

## CAT71C256L/71C256LI - Low Power

### 32K x 8-BIT CMOS STATIC RAM

#### DESCRIPTION

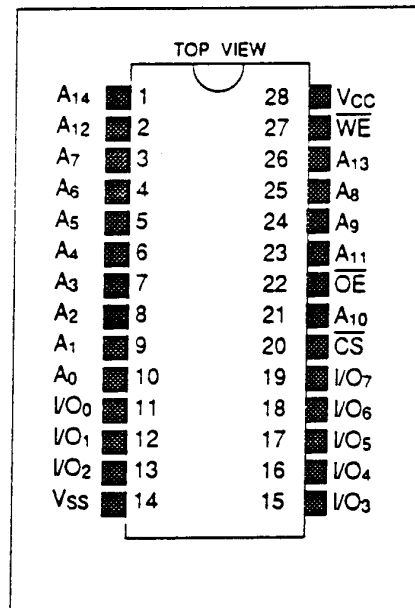
The CAT71C256L/71C256LI is a low power, high performance 262,144 bit CMOS static RAM organized as a 32,768 X 8 bit array. It features 5V single power supply operation and direct TTL input/output compatibility. Since the circuitry is completely static, external clock and refreshing operations are unnecessary. The CAT71C256L/71C256LI is a CMOS device requiring extremely low power during standby (100 $\mu$ A). The  $\overline{\text{CS}}$  and  $\overline{\text{OE}}$  control signals facilitate OR-tying of the output lines, simplifying memory expansion.

#### FEATURES

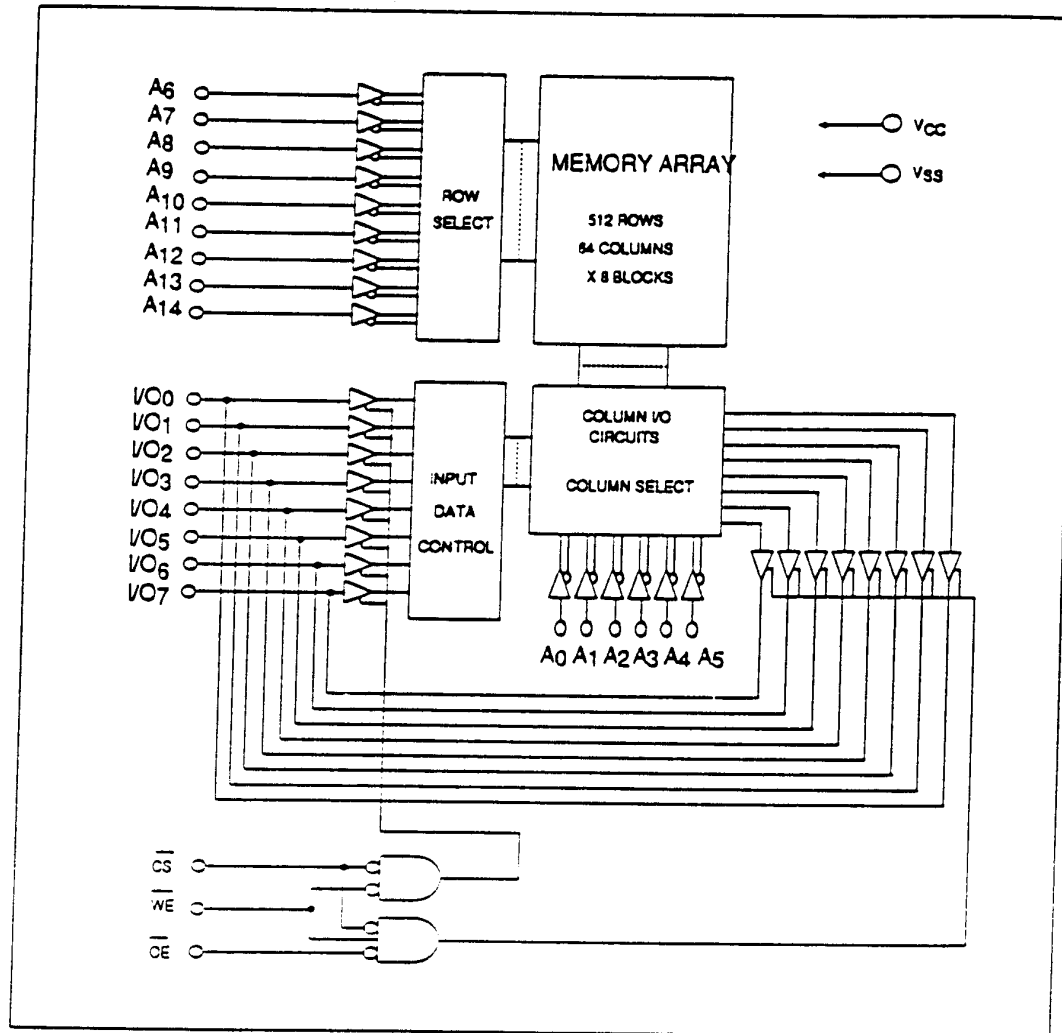
- Single 5V supply (  $\pm 10\%$  )
- Low power consumption:
  - Active: 80mA max
  - Standby: 100 $\mu$ A max
- 32,768 X 8 configuration
- Static operation
- Access / Cycle time: 85ns max
- TTL compatible INPUT/OUTPUT
- Three state outputs
- 28-pin DIP and 28-pin SO packages
- Temperature Range:
  - CAT71C256L (0° to +70°C)
  - CAT71C256LI (-40° to +85°C)

#### PIN CONFIGURATION

28-Pin DIP and SO



**BLOCK DIAGRAM**



**Pin Assignment**

|                                     |                    |
|-------------------------------------|--------------------|
| A <sub>0</sub> - A <sub>14</sub>    | :ADDRESS INPUTS    |
| I/O <sub>0</sub> - I/O <sub>7</sub> | :DATA INPUT/OUTPUT |
| $\overline{\text{CS}}$              | :CHIP SELECT       |
| $\overline{\text{WE}}$              | :WRITE ENABLE      |
| $\overline{\text{OE}}$              | :OUTPUT ENABLE     |

## MODES OF OPERATION

| Mode    | $\overline{CS}$ | $\overline{WE}$ | $\overline{OE}$ | I/O Operation |
|---------|-----------------|-----------------|-----------------|---------------|
| Standby | H               | X               | X               | High-Z        |
| Read    | L               | H               | H               | High-Z        |
|         | L               | H               | L               | DOUT          |
| Write   | L               | L               | X               | DIN           |

Note: X = H or L

## ABSOLUTE MAXIMUM RATINGS

| Symbol           | Rating              | Conditions                                             | Value                        | Unit |
|------------------|---------------------|--------------------------------------------------------|------------------------------|------|
| V <sub>CC</sub>  | Supply voltage      | T <sub>A</sub> = 25°C, with respect to V <sub>SS</sub> | -0.3 to 7.0                  | V    |
| V <sub>IN</sub>  | Input voltage       |                                                        | -0.3 to V <sub>CC</sub> +0.3 | V    |
| P <sub>D</sub>   | Power dissipation   | T <sub>A</sub> = 25°C                                  | 1.0                          | W    |
| T <sub>STG</sub> | Storage temperature | -                                                      | -55 to +150                  | °C   |

\* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Symbol           | Parameter              | Conditions                 | Limits |      |                      | Unit |
|------------------|------------------------|----------------------------|--------|------|----------------------|------|
|                  |                        |                            | Min.   | Typ. | Max.                 |      |
| V <sub>CC</sub>  | Supply voltage         | V <sub>CC</sub> = 5V ± 10% | 4.5    | 5    | 5.5                  | V    |
| V <sub>SS</sub>  |                        |                            |        | 0    |                      | V    |
| V <sub>CCH</sub> | Data retention voltage |                            | 2      | 5    | 5.5                  | V    |
| V <sub>IH</sub>  | "H" Input voltage      | 5V ± 10%                   | 2.2    | -    | V <sub>CC</sub> +0.3 | V    |
| V <sub>IL</sub>  | "L" Input voltage      |                            | -0.3   | -    | 0.8                  | V    |
| T <sub>OPR</sub> | Operating temperature  | CAT71C256L                 | 0      | -    | +70                  | °C   |
|                  |                        | CAT71C256LI                | -40    | -    | +85                  | °C   |
| CL               | Output load            |                            | -      | -    | 100                  | pF   |
| TTL              |                        |                            | -      | -    | 1                    | -    |

## DC CHARACTERISTICS

(V<sub>CC</sub> = +5V ±10%), T<sub>A</sub> (71C256L = 0°C to +70°C, 71C256LI = -40°C to 85°C)

| Symbol            | Parameter                     | Conditions                                                                                     | Limits |      |      | Unit |
|-------------------|-------------------------------|------------------------------------------------------------------------------------------------|--------|------|------|------|
|                   |                               |                                                                                                | Min.   | Typ. | Max. |      |
| I <sub>LI</sub>   | Input leakage current         | V <sub>IN</sub> = 0 to V <sub>CC</sub>                                                         | -1     |      | 1    | μA   |
| I <sub>LO</sub>   | Output leakage current        | $\overline{CS}$ or $\overline{OE}$ = V <sub>IH</sub><br>V <sub>IO</sub> = 0 to V <sub>CC</sub> | -1     |      | 1    | μA   |
| V <sub>OH</sub>   | "H" output voltage            | I <sub>OH</sub> = -1mA                                                                         | 2.4    |      | -    | V    |
| V <sub>OL</sub>   | "L" output voltage            | I <sub>OL</sub> = 2.1mA                                                                        |        |      | 0.4  | V    |
| I <sub>CCS</sub>  | Standby supply current (CMOS) | $\overline{CS} \geq V_{CC} - 0.2V$<br>V <sub>IN</sub> = 0 to V <sub>CC</sub>                   |        | 0.2  | 100  | μA   |
| I <sub>CCS1</sub> | Standby supply current (TTL)  | $\overline{CS} = V_{IH}$<br>T <sub>cyc</sub> = min. cycle                                      |        |      | 3    | mA   |
| I <sub>CCA</sub>  | Operating supply current      | Min. cycle                                                                                     |        |      | 80   | mA   |

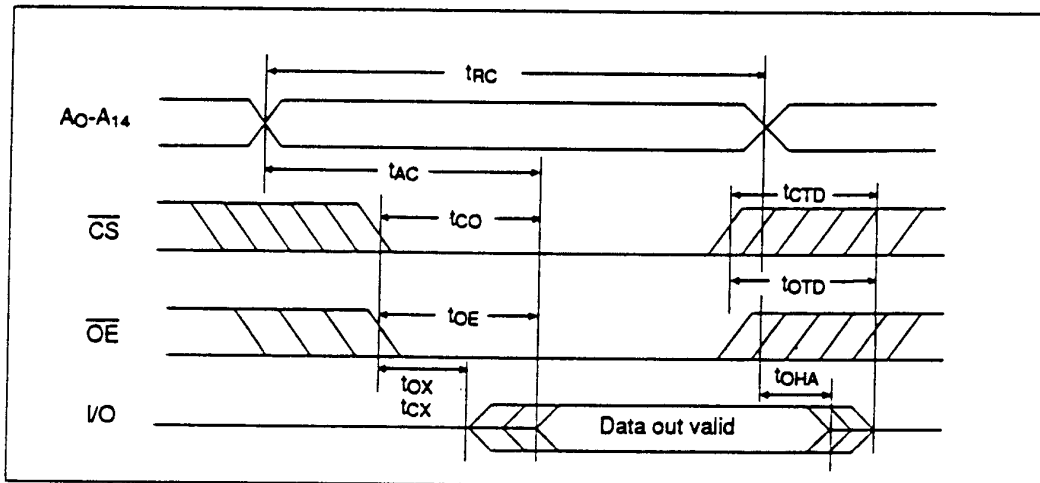
## AC CHARACTERISTICS - TEST CONDITIONS

| Parameter                           | Conditions                                     |
|-------------------------------------|------------------------------------------------|
| Input Pulse Level                   | V <sub>IH</sub> = 2.4V, V <sub>IL</sub> = 0.6V |
| Input Rise and Fall Times           | 5 ns                                           |
| Input/Output Timing Reference Level | 1.5V                                           |
| Output Load                         | C <sub>L</sub> = 100pF, 1 TTL gate             |

## READ CYCLE

(V<sub>CC</sub> = 5V ±10%), T<sub>A</sub> (71C256L = 0°C to +70°C, 71C256LI = -40°C to +85°C)

| Symbol           | Parameter                            | 71C256LI-85 |      | Units |
|------------------|--------------------------------------|-------------|------|-------|
|                  |                                      | Min.        | Max. |       |
| t <sub>RC</sub>  | Read Cycle Time                      | 85          |      | ns    |
| t <sub>AC</sub>  | Address Access Time                  |             | 85   | ns    |
| t <sub>CO</sub>  | Chip Select Access Time              |             | 85   | ns    |
| t <sub>OE</sub>  | Output Enable to Output Valid        |             | 45   | ns    |
| t <sub>CX</sub>  | Chip Selection to Output Active      | 10          |      | ns    |
| t <sub>OHA</sub> | Output Hold Time from Address Change | 5           |      | ns    |
| t <sub>OTD</sub> | Output 3-state from Output Disable   | 0           | 30   | ns    |
| t <sub>CTD</sub> | Output 3-state from Chip Deselection |             | 30   | ns    |
| t <sub>OX</sub>  | Output Enable to Output Active       | 5           |      | ns    |

**READ CYCLE TIMING****NOTES:**

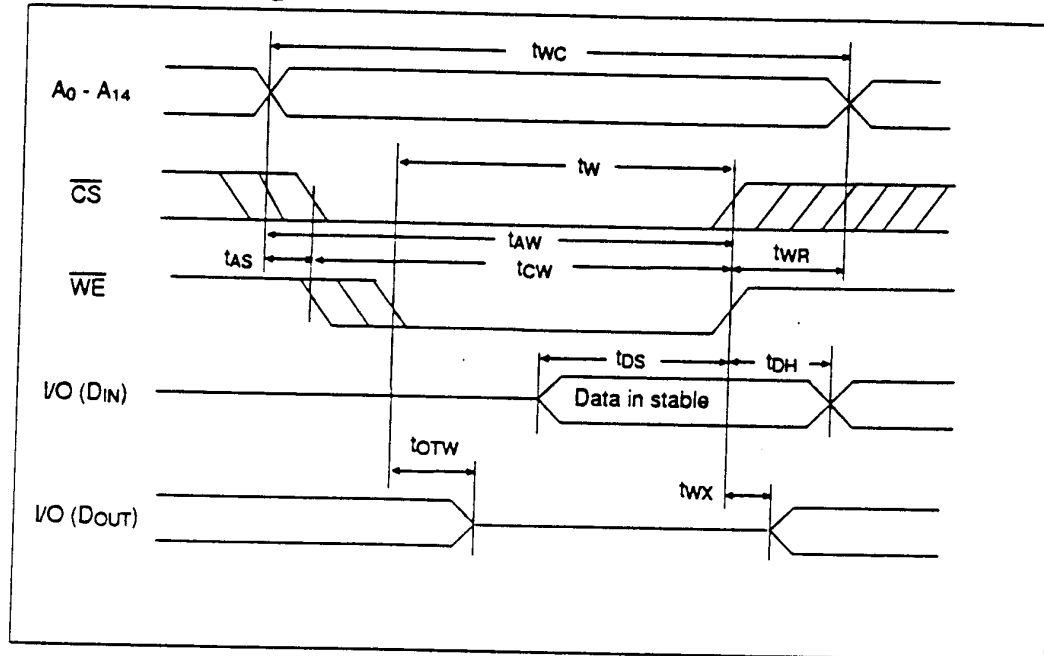
1. A READ occurs during the overlap of a low  $\overline{CS}$ , a low  $\overline{OE}$  and a high  $\overline{WE}$ .
2.  $t_{CTD}$  and  $t_{OTD}$  are specified by the time to DATA OUT high impedance.

**WRITE CYCLE**

( $V_{CC} = 5V \pm 10\%$ ),  $T_A$  (71C256L =  $0^\circ\text{C}$  to  $+70^\circ\text{C}$ , 71C256LI =  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ )

| Symbol    | Parameter                       | 71C256L/J-85 |      | Units |
|-----------|---------------------------------|--------------|------|-------|
|           |                                 | Min.         | Max. |       |
| $t_{WC}$  | Write Cycle Time                | 85           |      | ns    |
| $t_{CW}$  | Chip Selection to End of Write  | 75           |      | ns    |
| $t_{AW}$  | Address Valid to End of Write   | 75           |      | ns    |
| $t_{AS}$  | Address to Write Set-up Time    | 0            |      | ns    |
| $t_W$     | Write Time                      | 70           |      | ns    |
| $t_{WR}$  | Write Recovery Time             | 5            |      | ns    |
| $t_{DS}$  | Data Set-up Time                | 40           |      | ns    |
| $t_{DH}$  | Data Hold from Write Time       | 0            |      | ns    |
| $t_{OTW}$ | Output 3-state from Write       | 0            | 30   | ns    |
| $t_{WX}$  | Output Active from End of Write | 5            |      | ns    |

## WRITE CYCLE TIMING



## NOTES:

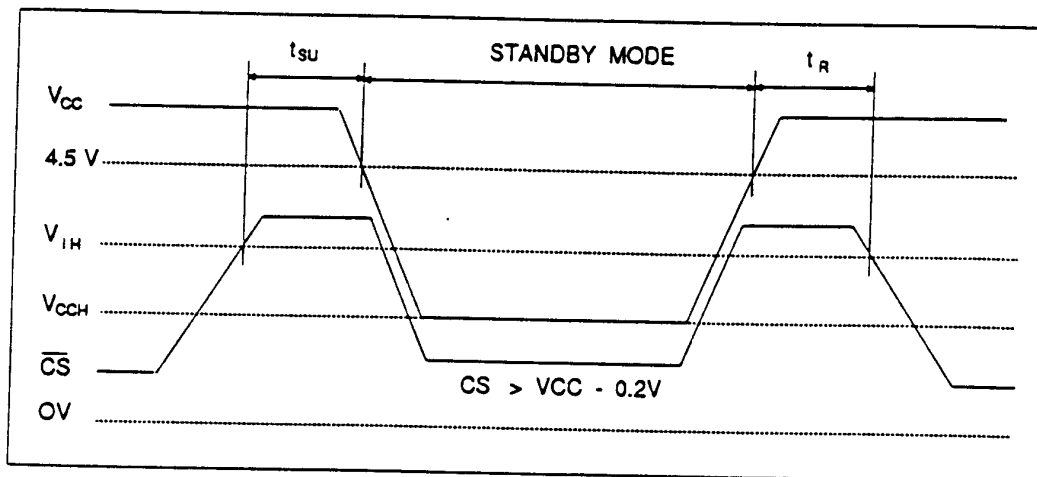
1. Write condition: during the overlap of a low  $\overline{CS}$  and a low  $\overline{WE}$ .
2.  $\overline{OE}$  can be both high and low during a Write cycle.
3.  $t_{AS}$  is specified from a low  $\overline{CS}$  or a low  $\overline{WE}$ , whichever occurs last after the address is set.
4.  $t_w$  is the overlap time of a low  $\overline{CS}$  and a low  $\overline{WE}$ .
5.  $t_{WR}$ ,  $t_{DS}$  and  $t_{DH}$  are specified from a high  $\overline{CS}$  or a high  $\overline{WE}$ , whichever occurs first.
6.  $t_{OTW}$  is specified by the time to DATA OUT high impedance, not by output level.
7. When I/O pins are in data output mode, do not force inverse input signals to those pins.

## CAPACITANCE

( $T_A = 25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ ,  $V_{CC} = 5\text{V}$ )

| Symbol   | Parameter                | Conditions           | Limits<br>Typ. max. | Unit |
|----------|--------------------------|----------------------|---------------------|------|
| $C_{VO}$ | Input/Output capacitance | $V_{IO} = 0\text{V}$ | 10                  | pF   |
| $C_{IN}$ | Input capacitance        | $V_{IN} = 0\text{V}$ | 10                  | pF   |

Note: These parameters are periodically sampled and are not 100% tested.

**$\overline{CS}$  CONTROL TIMING****LOW  $V_{CC}$  DATA RETENTION CHARACTERISTICS**

$T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , unless otherwise noted.

| Symbol    | Parameter                              | Conditions                                            | Limits   |      |      | Unit    |
|-----------|----------------------------------------|-------------------------------------------------------|----------|------|------|---------|
|           |                                        |                                                       | Min.     | Typ. | Max. |         |
| $V_{CCH}$ | $V_{CC}$ for data retention            | $\overline{CS} \geq V_{CC} - 0.2V$                    | 2        |      |      | V       |
| $I_{CCH}$ | Data retention current                 | $\overline{CS} \geq V_{CC} - 0.2V$ ,<br>$V_{CC} = 3V$ |          | 1    | 50   | $\mu A$ |
| $t_{SU}$  | $\overline{CS}$ to Data retention time |                                                       | 0        |      |      | ns      |
| $t_R$     | Operation recovery time                |                                                       | $t_{RC}$ |      |      | ns      |