PRELIMINARY

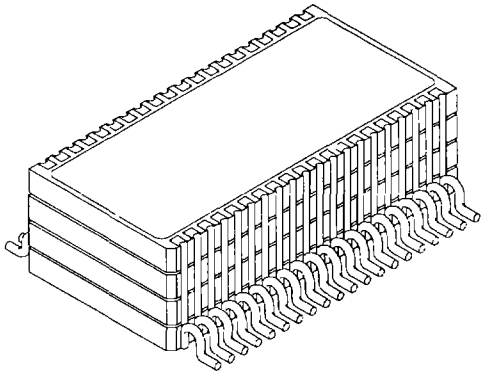
DESCRIPTION:

The DPD1MX16M2H3 "STACK" module is a revolutionary new memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC) stacked and leaded for surface mount applications. The module is configured as a four-high stack with dual sided Gullwing leads and packs 16-Megabits of CMOS DRAM in an area just over one-half square inch (0.539 in^2), while maintaining a height of only 0.356 inches.

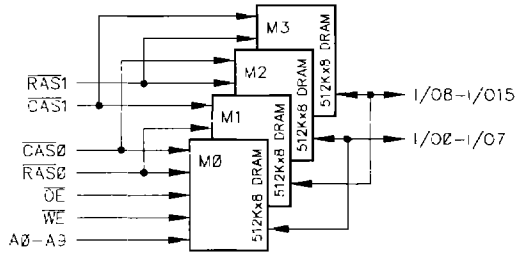
The DPD1MX16M2H3 contains four individual 512K x 8 DRAMs, packaged in their own hermetically sealed SLCC making the module suitable for commercial, industrial and military applications.

The module can be organized as 1Meg x 16 or 2Meg x 8 and has a Fast Page Mode as a high speed access mode.

By using SLCCs, the "Stack" family of modules offers a higher board density of memory than available with conventional through-hole, surface mount or hybrid techniques.



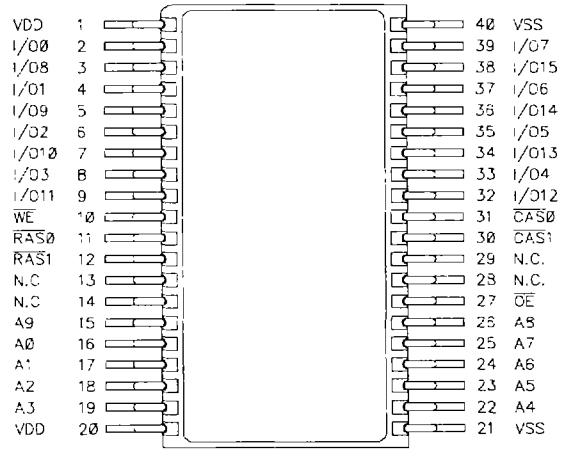
FUNCTIONAL BLOCK DIAGRAM



FEATURES:

- Organizations Available: 1Meg x 16, 2Meg x 8
- Access Times: 70, 80, 100ns
- 1,024 Refresh Cycles (16ms)
- Single +5V Power Supply, ±10% Tolerance
- 3 Variations of Refresh:
  - RAS Only Refresh
  - CAS before RAS Refresh
  - Hidden Refresh
- Common Data Inputs and Outputs
- 40-Pin Dual Sided Gullwing STACK Package

PIN-OUT DIAGRAM



PIN NAMES	
A0 - A9	Address Inputs
I/O0 - I/O15	Data Input/Output
RAS0, RAS1	Row Address Strobes
CAS0, CAS1	Column Address Strobes
WE	Write Enable
OE	Output Enable
V_{DD}	Power (+ 5V)
V_{SS}	Ground
N.C.	No Connect

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS			
Symbol	**Parameter**	**Value**	**Units**
T_{STC}	Storage Temperature	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +80	°C
$V_{I/O}$	Voltage on Any Pin	-2.0 to +7.0	V
V_{DD}	V_{DD} Supply Voltage	-1.0 to +7.0	V
I_{OUT}	Output Current	50	mA

CAPACITANCE: t_A = 25°C, f = 1MHz				
Symbol	**Parameter**	**Max**	**Unit**	**Condition**
C_{ADR}	Address Input	30	pF	V_{IN} = 0V
C_{I2}	CAS Input	15		
C_{I3}	RAS Input	15		
C_{WE}	Write Enable	30		
C_{OE}	Output Enable	30		
$C_{I/O}$	Data Input/Output	25		

RECOMMENDED OPERATING CONDITIONS						
Symbol	**Parameter**		**Min.**	**Typ.**	**Max.**	**Units**
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IL}	Input Low Voltage		-1.0		0.8	V
V_{IH}	Input High Voltage		2.4		V_{DD}+1.0	V
T_A	Operating Temperature	C	0	+25	+70	°C
		I	-40	+25	+85	
		M/B	-55	+25	+110	

NOTE: All voltages referenced to V_{SS}.

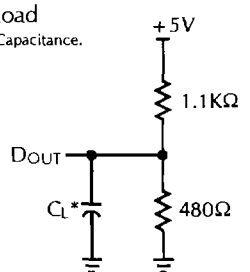
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns *
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V

* Transition measured between 0.8V and 2.2V.

OUTPUT LOAD		
Load	**CL**	**Parameters Measured**
1	100pF	except t_{CLZ}
2	5pF	t_{CLZ}

Figure 1. Output Load

** Including Scope and Jig Capacitance.



DC OPERATING CHARACTERISTICS						
Symbol	**Characteristic**	**Conditions**		**Limits**		**Units**
				Min.	**Max.**	
I_{CC1}	Standby Current: TTL	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}			8	mA
I_{CC2}	Standby Current: CMOS [25]	$\overline{RAS}$ = $\overline{CAS}$ = V_{DD} -2.0V			4	mA
I_{CC3}	Operating Current: [3,4,29] Random READ/WRITE	$\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min.	x8		245	mA
			x16		480	
I_{CC4}	Operating Supply Current: [3,4,29] FAST-PAGE-MODE	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min.; t_{CP}, t_{ASC} = 10ns	x8		225	mA
			x16		440	
I_{CC5}	Refresh Current: $\overline{RAS}$ ONLY [3,29]	One $\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min.			245	mA
I_{CC5}	Refresh Current: $\overline{RAS}$ ONLY [3,29]	Two $\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min.			480	mA
I_{CC6}	Refresh Current: CBR [3]	One $\overline{RAS}$ Cycling, One $\overline{CAS}$ Cycling, Address Cycling: t_{RC} = t_{RC} min.			235	mA
I_{CC6}	Refresh Current: CBR [3]	Two $\overline{RAS}$ Cycling, Two $\overline{CAS}$ Cycling, Address Cycling: t_{RC} = t_{RC} min.			440	mA
V_{OL}	Output Low Voltage	I_{OL} = 4.2mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -5mA		2.4		V

TRUTH TABLE								
OPERATING MODE		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESS		DATA OUTPUT
						t_R	t_C	
Standby		H	H→X	X	X	X	X	HIGH-Z
Read Cycle		L	L	H	L	ROW	COL	Data-Out
Early Write Cycle *		L	L	L	X	ROW	COL	Data-In
Read - Write Cycle *		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
Fast - Page - Mode Read Cycle	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd Cycle	L	H→L	H	L	N/A	COL	Data-Out
Fast - Page - Mode Write Cycle	1st Cycle *	L	H→L	L	X	ROW	COL	Data-In
	2nd Cycle *	L	H→L	L	X	N/A	COL	Data-In
Fast - Page - Mode Read Write Cycle	1st Cycle *	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd Cycle *	L	H→L	H→L	L→H	N/A	COL	Data-Out, Data-In
Hidden Refresh Cycle	READ	L→H→L	L	L	L	ROW	COL	Data-Out
	WRITE *	L→H→L	L	L	X	ROW	COL	Data-In
$\overline{RAS}$ - Only Refresh Cycle		L	H	X	X	ROW	N/A	HIGH-Z
CBR Refresh Cycle		H→L	L	X	X	X	X	HIGH-Z

H = HIGH, L = LOW, X = Don't Care.
* EARLY WRITE only.

FUNCTIONAL DESCRIPTION

Each bit is uniquely addressed through the 19 address bits during READ or WRITE cycles. First, $\overline{RAS}$ is used to latch 10 bits (A0 - A9) then, $\overline{CAS}$ latches 9 bits (A0 - A8).

The $\overline{CAS}$ control also determines whether the cycle will be a refresh cycle ($\overline{RAS}$ - ONLY) or an active cycle (READ, WRITE or READ - WRITE) once $\overline{RAS}$ goes LOW.

READ or WRITE cycles are selected by $\overline{WE}$. A logic HIGH on $\overline{WE}$ dictates READ mode while a logic LOW on $\overline{WE}$ dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. Taking $\overline{WE}$ LOW will initiate a WRITE cycle, selecting I/O0 through I/O7. If $\overline{WE}$ goes LOW prior to $\overline{CAS}$ going LOW, the output pin(s) remain open (HIGH-Z) until the next $\overline{CAS}$ cycle. If $\overline{WE}$ goes LOW after $\overline{CAS}$ goes LOW and data reaches the output pins, data-out (Q) is activated and retains the selected cell data as long as $\overline{CAS}$ and $\overline{OE}$ remain LOW (regardless of $\overline{WE}$ or $\overline{RAS}$). This late $\overline{WE}$ pulse results in a READ - WRITE cycle.

The eight data inputs and eight data outputs are routed through eight pins using common I/O and pin direction is controlled by $\overline{OE}$ and $\overline{WE}$.

FAST - PAGE - MODE operations allow faster data operations (READ, WRITE or READ - MODIFY - WRITE) within a row-address-defined (A0 - A9) page boundary. The FAST - PAGE - MODE cycle is always initiated with a row-address strobed-in by $\overline{RAS}$ followed by a common - address strobed - in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ LOW and strobing-in different column-address, thus executing faster memory cycles. Returning $\overline{RAS}$ HIGH terminated the FAST - PAGE - MODE operation.

Returning $\overline{RAS}$ and $\overline{CAS}$ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is also preconditioned for the next cycle during the $\overline{RAS}$ HIGH time. Memory cell data is retained in its correct state by maintaining power and excluding any RAS cycle (READ - WRITE) or $\overline{RAS}$ REFRESH cycle ($\overline{RAS}$ - ONLY, CBR, or HIDDEN) so that all 1,024 combinations of $\overline{RAS}$ addresses (A0 - A9) are included at least every 16ms. regardless of sequence. The CBR REFRESH cycle will also invoke the refresh counter and controller for row - address control.

A.C. OPERATING AND CHARACTERISTICS

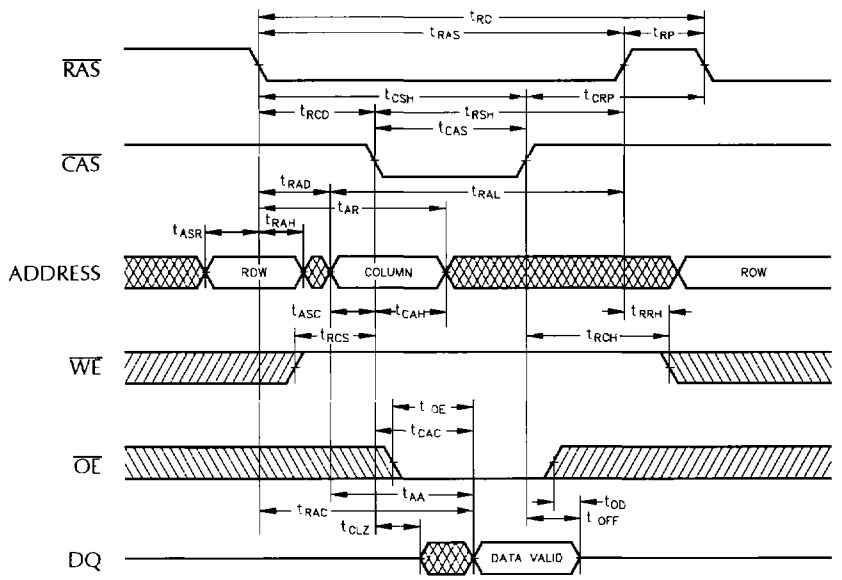
No.	Symbol	Parameter	70ns		80ns		100ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Random Read or Write Cycle Time	130		150		170		ns
2	t_{RWC}	Read - Write Cycle Time	175		195		215		ns
3	t_{PC}	FAST - PAGE - MODE Read or Write Cycle Time	40		45		55		ns
4	t_{PRWC}	FAST - PAGE - MODE Read - Write Cycle Time	95		100		110		ns
5	t_{RAC}	Access Time from $\overline{RAS}$ [14]		70		80		100	ns
6	t_{CAC}	Access Time from $\overline{CAS}$ [15]		20		20		20	ns
7	t_{OE}	Output Enable Time		20		20		20	ns
8	t_{AA}	Access Time from Column - Address		35		40		45	ns
9	t_{CPA}	Access Time from $\overline{CAS}$ precharge		40		45		50	ns
10	t_{RAS}	$\overline{RAS}$ Pulse Width	70	100,000	80	100,000	100	100,000	ns
11	t_{RASP}	$\overline{RAS}$ Pulse Width (FAST - PAGE - MODE)	70	100,000	80	100,000	100	100,000	ns
12	t_{RSH}	$\overline{RAS}$ Hold Time	20		20		20		ns
13	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		80		ns
14	t_{CAS}	$\overline{CAS}$ Pulse Width	20	100,000	20	100,000	20	100,000	ns
15	t_{CSH}	$\overline{CAS}$ Hold Time	70		80		100		ns
16	t_{CPN}	$\overline{CAS}$ Precharge Time [16]	10		10		10		ns
17	t_{CP}	$\overline{CAS}$ Precharge Time (FAST - PAGE - MODE)	10		10		10		ns
18	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time [17]	20	50	20	60	20	70	ns
19	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		10		ns
20	t_{ASR}	Row Address Setup Time	0		0		0		ns
21	t_{RAH}	Row Address Hold Time	10		10		10		ns
22	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time [18]	15	35	15	40	15	45	ns
23	t_{ASC}	Column Address Setup Time	0		0		0		ns
24	t_{CAH}	Column Address Hold Time	15		15		15		ns
25	t_{AR}	Column Address Hold Time to $\overline{RAS}$	55		60		65		ns
26	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35		40		45		ns
27	t_{RCS}	Read Command Setup Time [26]	0		0		0		ns
28	t_{RCH}	Read Command Hold Time to $\overline{CAS}$ [19, 26]	0		0		0		ns
29	t_{RRH}	Read Command Hold Time to $\overline{RAS}$ [19]	0		0		0		ns
30	t_{CLZ}	$\overline{CAS}$ to Output In LOW-Z [30]	3		3		3		ns
31	t_{OFF}	Output Buffer Turn-Off Delay Time [20, 28, 30]	3	15	3	15	3	15	ns
32	t_{OD}	Output Disable Time [28, 30]	3	15	3	15	3	15	ns
33	t_{WCS}	Write Command Setup Time [21, 26]	0		0		0		ns
34	t_{WCH}	Write Command Hold Time [26]	10		10		10		ns
35	t_{WCR}	Write Command hold Time to $\overline{RAS}$ [26]	55		60		70		ns
36	t_{WP}	Write Command Pulse Width [26]	10		10		10		ns
37	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time [26]	20		20		20		ns
38	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time [26]	20		20		20		ns
39	t_{DS}	Data-In Setup Time [22]	0		0		0		ns
40	t_{DH}	Data-In Hold Time [22]	15		15		15		ns
41	t_{DHR}	Data-In Hold Time to $\overline{RAS}$	55		60		70		ns
42	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time [21]	95		105		120		ns
43	t_{AWD}	Column Address to $\overline{WE}$ Delay Time [21]	60		65		70		ns

A.C. OPERATING AND CHARACTERISTICS (Continued)									
No.	Symbol	Parameter	70ns		80ns		100ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
44	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time [21]	45		45		45		ns
45	t_T	Transition Time (Rise or Fall) [9, 10]	3	50	3	50	3	50	ns
46	t_{REF}	Refresh Period (1,024 cycles)		10		10		10	ms
47	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Percharge Time	0		0		0		ns
48	t_{CSR}	$\overline{CAS}$ Setup Time (CBR Refresh Cycle) [5]	10		10		10		ns
49	t_{CHR}	$\overline{CAS}$ Hold Time (CBR Refresh Cycle) [5]	10		10		10		ns
50	t_{WRS}	MASKED WRITE Command to $\overline{RAS}$ Setup Time [26]	0		0		0		ns
51	t_{WRH}	$\overline{WE}$ Hold Time to $\overline{RAS}$ (MASKED WRITE) [26]	15		15		15		ns
52	t_{OEH}	$\overline{OE}$ Hold Time from WE During [27] READ - MODIFY - WRITE Cycle	20		20		20		ns
53	t_{ORD}	$\overline{OE}$ Setup prior to RAS during HIDDEN REFRESH Cycle	0		0		0		ns

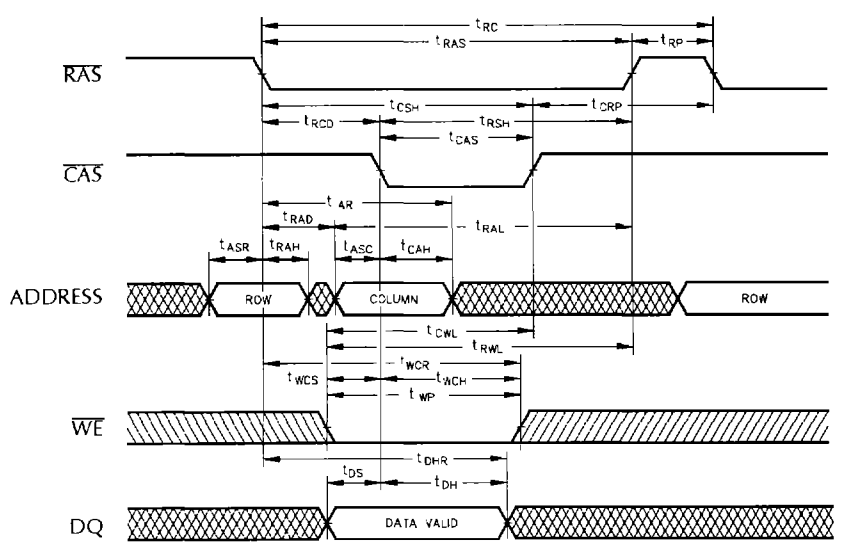
NOTES:

1. All voltages are referenced to V_{SS}.
2. This parameter is sample. V_{DD} - 5V ± 10%; f = 1MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on - chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is assured.
7. An initial pause of 100µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$ - ONLY or CBR) before proper operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
8. AC Characteristics assume t_T = 5ns.
9. V_{IH} (min) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monatomic manner.
11. If $\overline{CAS}$ = V_{IH}, data output is high impedance.
12. If $\overline{CAS}$ = V_{IL}, data output may contain data from the last valid READ cycle.
13. Measured with the load equivalent of two TTL gates and 100pF, V_{OH} = 2.0V and V_{OL} = 0.8V.
14. Assumes that t_{RCD} < t_{RCD} (max.). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
15. Assumes that t_{RCD} ≥ t_{RCD} (max.).
16. If $\overline{CAS}$ is LOW at the falling edge of $\overline{RAS}$, Q will be maintained from the previous cycle. To initiate a new cycle and clear the Q buffer, $\overline{CAS}$ must be pulsed HIGH for t_{CPN}.
17. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RCD} is greater than the specified t_{RCD} (max.) limit, access time is controlled exclusively by t_{CAC}.
18. Operation within the t_{RAD} limit ensures that t_{RCD} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, access time is controlled exclusively by t_{AA}.
19. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
20. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}.
21. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are restrictive operating parameters in LATE - WRITE and READ - MODIFY - WRITE cycles only. If t_{WCS} ≥ t_{WCS} (min.), the cycle is an EARLY - WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If t_{RWD} ≥ t_{RWD} (min.), t_{AWD} ≥ t_{AWD} (min.) and t_{CWD} ≥ t_{CWD} (min.), the cycle is a READ - WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data - out is indeterminate. $\overline{OE}$ held HIGH and $\overline{WE}$ taken LOW after $\overline{CAS}$ goes LOW results in a LATE - WRITE ($\overline{OE}$ = controlled) cycle.
22. These parameters are referenced to $\overline{CAS}$ leading edge in EARLY - WRITE cycles and $\overline{WE}$ leading edge in LATE - WRITE or READ- MODIFY - WRITE cycles.
23. During a READ cycle, if $\overline{OE}$ is LOW then taken HIGH before $\overline{CAS}$ goes HIGH, Q goes open. If $\overline{OE}$ is tied permanently LOW, LATE - WRITE or READ - MODIFY WRITE operations are not possible.
24. A HIDDEN - REFRESH may also be performed after a WRITE cycle. In this case $\overline{WE}$ = LOW and $\overline{OE}$ = HIGH.
25. All other inputs at V_{DD} -0.2V.
26. Write command is defined as $\overline{WE}$ going LOW.
27. LATE - WRITE and READ - MODIFY - WRITE cycles must have both t_{OD} and t_{OEH} met ($\overline{OE}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously written data if $\overline{CAS}$ remains LOW and $\overline{OE}$ is taken back LOW after t_{OEH} is met. If $\overline{CAS}$ goes HIGH prior to $\overline{OE}$ going back LOW, the DQs will remain open.
28. The DQs open during READ cycles once t_{OD} or t_{OFF} occur. If $\overline{CAS}$ goes HIGH before $\overline{OE}$, the DQs will open regardless of the state of $\overline{OE}$. If $\overline{CAS}$ stays LOW while $\overline{OE}$ is brought HIGH, the DQs will open. If $\overline{OE}$ is brought back LOW ($\overline{CAS}$ still LOW), the DQs will provide the previously read data.
29. Column - Address changed once while $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
30. The 3ns minimum is a parameter guaranteed by design.

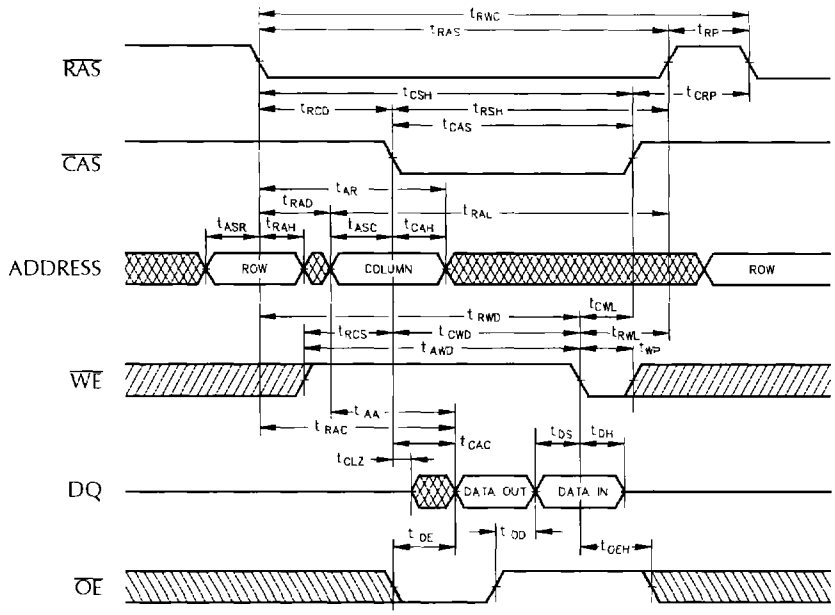
READ CYCLE



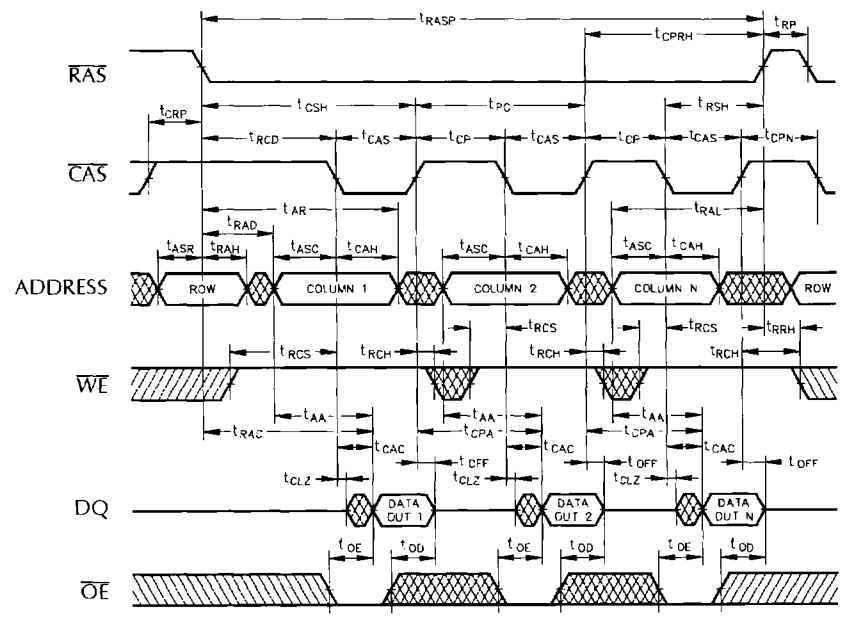
EARLY - WRITE CYCLE; ($\overline{OE}$ = Don't Care)



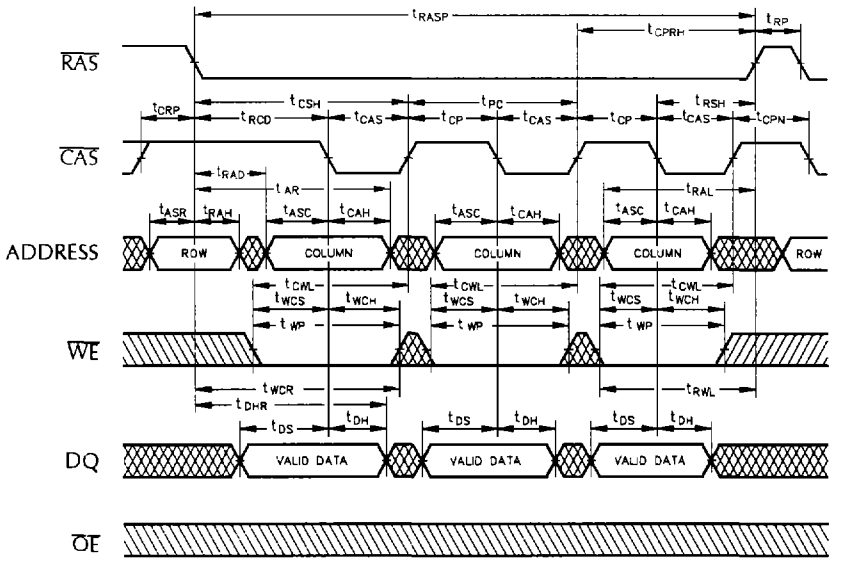
READ - WRITE CYCLE (LATE - WRITE and READ - MODIFY - WRITE CYCLES)



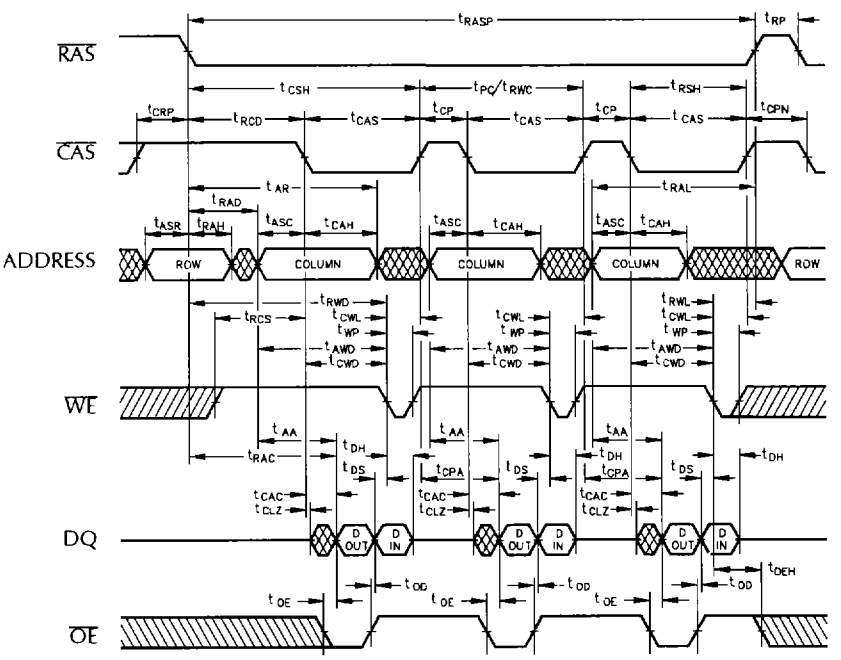
FAST - PAGE MODE READ CYCLE



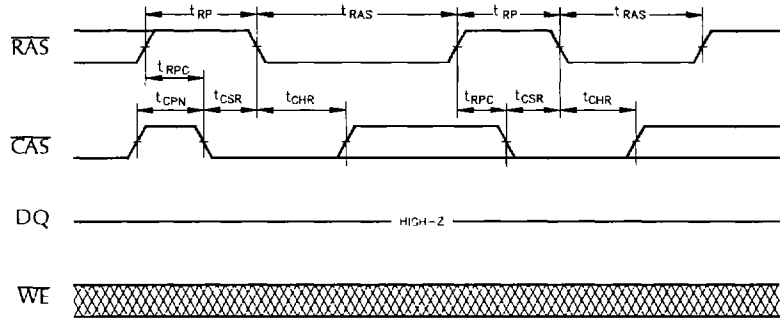
FAST - PAGE - MODE EARLY - WRITE CYCLE



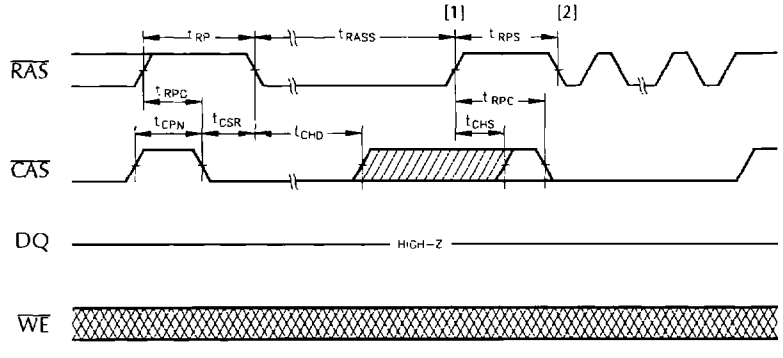
FAST - PAGE - MODE READ - WRITE CYCLE (LATE - WRITE and READ - MODIFY - WRITE CYCLES)



CBR REFRESH CYCLE (A0 - A9; $\overline{OE}$ = Don't Care)

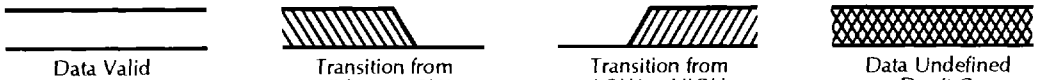


SELF REFRESH CYCLE - "SLEEP - MODE" (A0 - A9; $\overline{OE}$ = Don't Care)



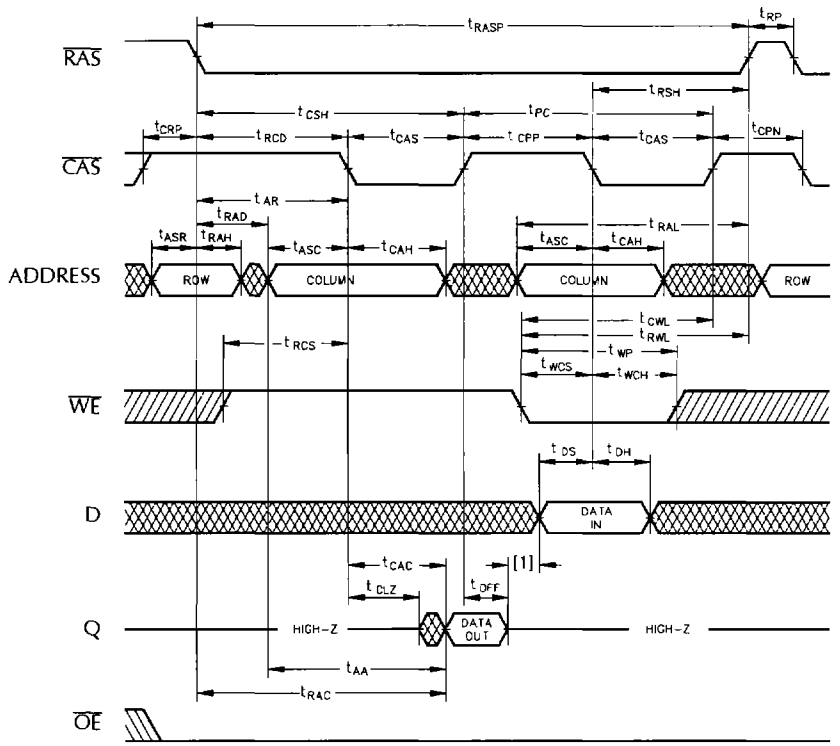
NOTES:
[1] Once tRASS (min.) is met, and $\overline{RAS}$ remains LOW, the DRAM will enter SELF REFRESH mode.
[2] Once tRPS is satisfied, a complete burst of all rows should be executed.

WAVEFORM KEY



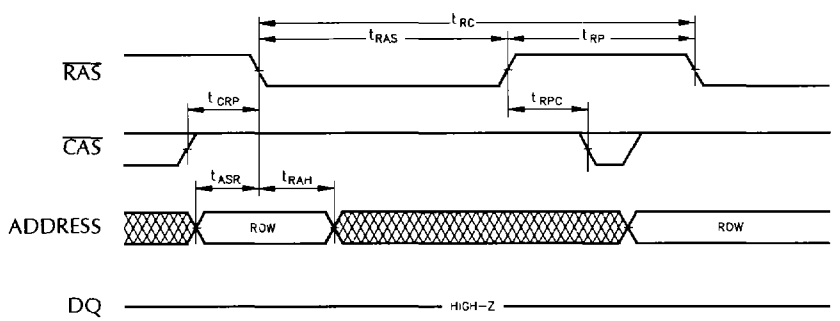
Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

FAST - PAGE - MODE READ - EARLY - WRITE CYCLE (Pseudo READ - MODIFY - WRITE CYCLES)

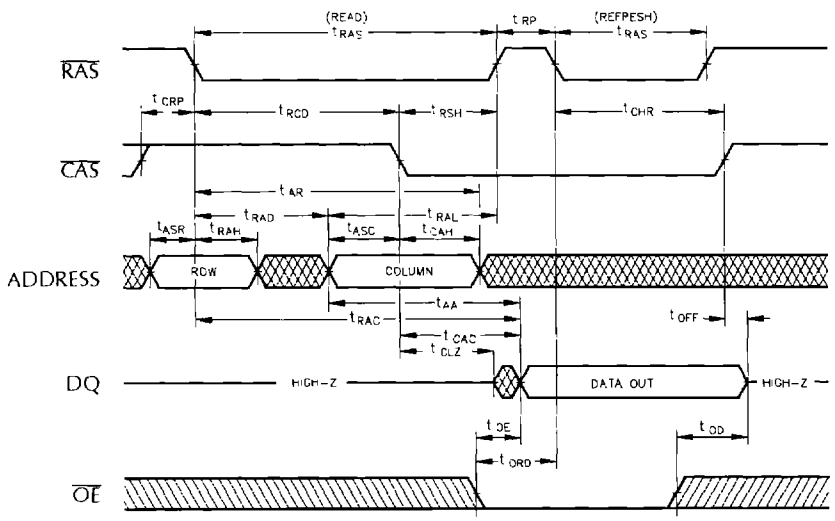


NOTE:
[1] Do not drive data prior to HIGH-Z; that is completion of tOFF. tCPP is equal of tOFF + tDS (min.) + guardband between data-out and driving new data-in

RAS - ONLY REFRESH CYCLE (OE and WE Don't Care)



HIDDEN REFRESH CYCLE [24] ($\overline{WE}$ = HIGH; $\overline{OE}$ = LOW)



PRELIMINARY

ORDERING INFORMATION

DP	D	1M	X	16	M	2	H3	–	XX	X
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	DESIG	DESIG	PACKAGE		SPEED	GRADE

C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	−40°C to +85°C
M	MILITARY	−55°C to +110°C
B	MIL−PROCESSED	−55°C to +110°C

70	70ns
80	80ns
10	100ns

40−PIN GULLWING SURFACE MOUNT/(3−D) STACK

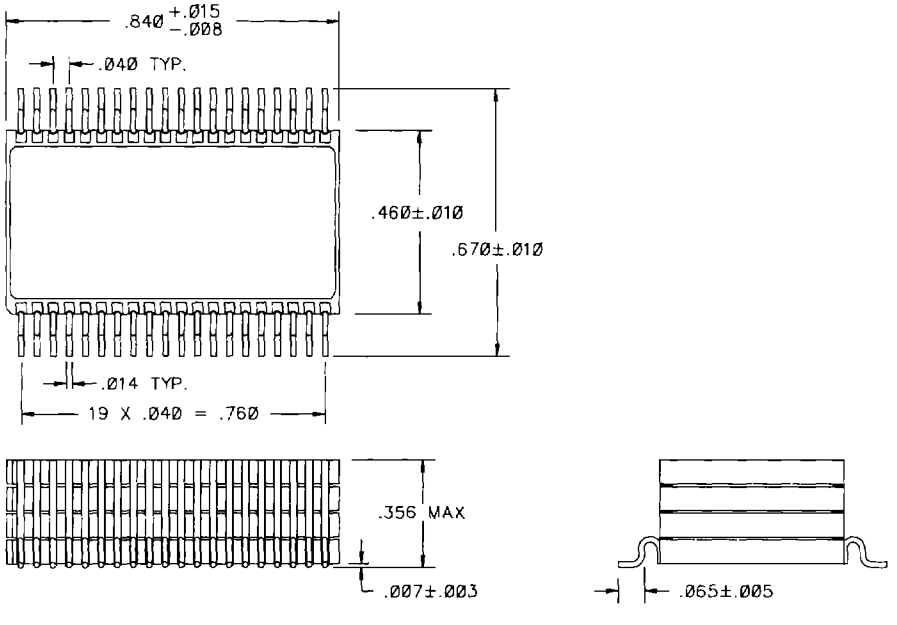
2 DUAL SIDED

M 4 MEG BASED DIE

MODULE WITHOUT SUPPORT LOGIC

DRAM DEVICES

MECHANICAL DRAWING



Dense-Pac Microsystems, Inc.
7321 Lincoln Way ◆ Garden Grove, California 92641-1428
(714) 898-0007 ◆ (800) 642-4477 (Outside CA) ◆ FAX: (714) 897-1772