Integrated Device Technology, Inc.

8K x 9 & 16K x 9 CMOS PARALLEL IN-OUT FIFO MODULE

IDT7MP2005
IDT7MP2011

FEATURES:

- First-In/First-Out memory module
- 8K x 9 organization (IDT7MP2005)
- 16K x 9 organization (IDT7MP2011)
- High speed: 20ns (max.) access time
- Asynchronous and simultaneous read and write
- Fully expandable by both word depth and/or bit width
- MASTER/SLAVE multiprocessing applications
- Bidirectional and rate buffer applications
- Empty and Full warning-flags
- High-performance CEMOS™ technology
- Single 5V (±10%) power supply

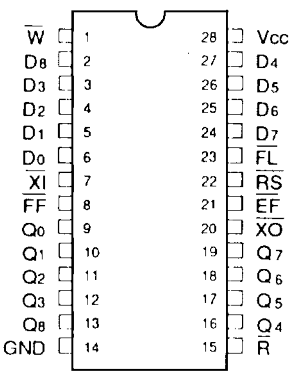
DESCRIPTION:

IDT7MP2005/7MP2011 are FIFO memory modules constructed on multi-layered epoxy laminate (FR-4) substrate by mounting two IDT7204 (4K x 9) or IDT7205 (8K x 9) FIFOs in plastic leaded chip carriers. Extremely high speeds are achieved in this fashion due to the use of IDT7203s and IDT7204s fabricated in IDT's high performance CEMOS technology. These devices utilize an algorithm that loads and empties data on a first-In/first-out basis. The device uses Full and Empty flags to prevent data overflow and underflow and expansion logic to allow for unlimited expansion capability in both word size and depth.

The reads and writes are internally sequential through the use of ring pointers, with no address information required to load and unload data. Data is toggled in and out of the device through the use of the WRITE (W) and READ (R) pins. The devices have a read/write cycle time of 30ns (min.) for commercial temperature ranges.

The devices utilize a 9-bit wide data array to allow for control and parity bits at the user's option. This feature is especially useful in data communications applications where it is necessary to use a parity bit for transmission/reception error checking.

PIN CONFIGURATION[1]



DSIP
TOP VIEW

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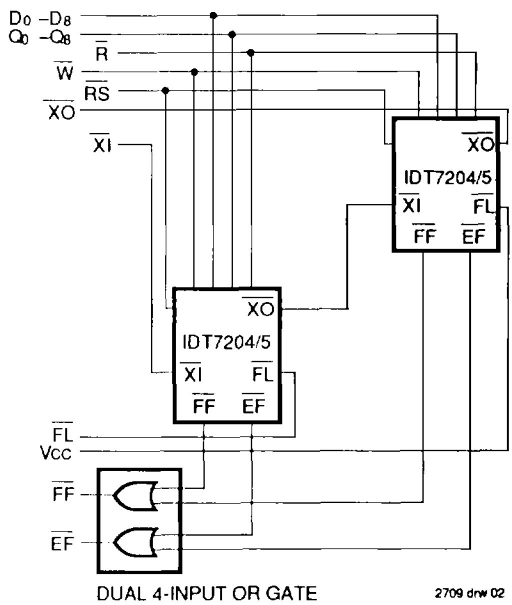
NOTE:
1. For module dimensions, please refer to drawing M34 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



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PIN NAMES

W = WRITE	FL = FIRST LOAD	XI = EXPANSION IN	EF = EMPTY FLAG
R = READ	D = DATAIN	XO = EXPANSION OUT	Vcc = POWER
RS = RESET	Q = DATAOUT	FF = FULL FLAG	GND = GROUND

DSC-7052/-

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Com'l.	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–55 to +125	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2709 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliabilty.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCCC	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH[1]	Input High Voltage Commercial	2.0	—	—	V
VIL[1]	Input Low Voltage Commercial	—	—	0.8	V

NOTE: 2709 tbl 03

1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (TA = +25°C, f = 1.0 MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
CIN	Input Capacitance	VIN = 0V	20	pF
COUT	Output Capacitance	VOUT = 0V	25	pF

NOTE: 2709 tbl 04

1. This parameter is guaranteed by design but not tested.

DC ELECTRICAL CHARACTERISTICS

(VCC = 5.0V ±10%, TA = 0°C to +70°C)

Symbol	Parameter	IDT7MP2005[4] Min.	IDT7MP2005[4] Max.	IDT7MP2011[5] Min.	IDT7MP2011[5] Max.	IDT7MP2005[6] Min.	IDT7MP2005[6] Max.	Unit
|ILI|[1]	Input Leakage Current (Any Input)	—	20	—	20	—	20	µA
|IOL|[2]	Output Leakage Current	—	20	—	20	—	20	µA
VOH	Output Logic "1" Voltage IOUT = –2mA	2.4	—	2.4	—	2.4	—	V
VOL	Output Logic "0" Voltage IOUT = 8mA	—	0.4	—	0.4	—	0.4	V
ICC1[3]	Operating Current	—	320	—	300	—	132	mA
ICC2[3]	Average Standby Current ($\overline{R}$ = $\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = VIH)	—	30	—	24	—	24	mA
ICC3[3]	Power Down Current (All Input = VCC – 0.2V)	—	16	—	16	—	16	mA

NOTES: 2709 tbl 04

1. Measurements with 0.4 ≤ VIN ≤ VOUT.
2. R ≥ VIH, 0.4 ≤ VOUT ≤ VCC.
3. ICC measurements are made with outputs open.
4. tAA = 20, 25, 30, 35ns.
5. tAA = 30, 35, 40, 50, 60, 70, 85, 120ns.
6. tAA = 40, 50, 60, 70, 85, 120ns.

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AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1, 2 & 3

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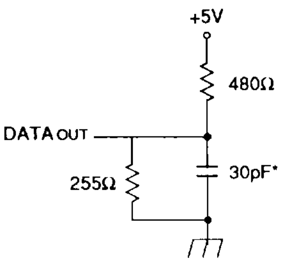

Figure 1. Output Load

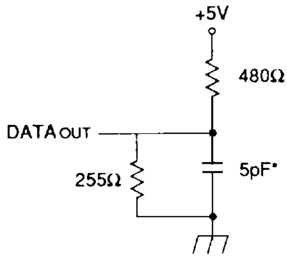

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Figure 2. Output Load
(for t_{RLZ}, t_{WLZ}, and t_{RHZ})

* Includes scope and jig capacitances.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V±10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP2005S20 Min.	7MP2005S20 Max.	7MP2005S25 Min.	7MP2005S25 Max.	7MP2005S30 7MP2011S30 Min.	7MP2005S30 7MP2011S30 Max.	7M205SS35 7M2011S35 Min.	7M205SS35 7M2011S35 Max.	Unit
t_{RC}	Read Cycle Time	30	—	35	—	40	—	45	—	ns
t_A	Access Time	—	20	—	25	—	30	—	35	ns
t_{RR}	Read Recovery Time	10	—	10	—	10	—	10	—	ns
t_{RPW}(1)	Read Pulse Width	20	—	25	—	30	—	35	—	ns
t_{RLZ}(2)	Read Pulse Low to Data Bus at Low Z	5	—	5	—	5	—	5	—	ns
t_{WLZ}(2)	Write Pulse High to Data Bus at Low Z	5	—	5	—	10	—	10	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	ns
t_{RHZ}(2)	Read Pulse High to Data Bus at High Z	—	13	—	20	—	20	—	20	ns
t_{WC}	Write Cycle Time	30	—	35	—	40	—	45	—	ns
t_{WPW}(1)	Write Pulse Width	20	—	25	—	30	—	35	—	ns
t_{WR}	Write Recovery Time	10	—	10	—	10	—	10	—	ns
t_{DS}	Data Set-up Time	15	—	18	—	18	—	20	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	0	—	ns
t_{RSC}	Reset Cycle Time	30	—	35	—	40	—	45	—	ns
t_{RS}(1)	Reset Pulse Width	20	—	25	—	30	—	35	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	10	—	10	—	ns
t_{EFL}	Reset to Emtpy Flag Low	—	30	—	35	—	40	—	45	ns
t_{REF}	Read Low to Emtpy Flag Low	—	20	—	25	—	30	—	35	ns
t_{RFF}	Read High to Full Flag High	—	23	—	25	—	30	—	35	ns
t_{WEF}	Write High to Empty Flag High	—	23	—	25	—	30	—	35	ns
t_{WFF}	Write Low to Full Flag Low	—	20	—	25	—	30	—	35	ns

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NOTES:
1. Pulse widths less than minimum value are not allowed.
2. This parameter is guaranteed by design but not tested.

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V±10%, T_A = 0°C to +70°C)

Symbol	Parameter	7MP2005S40 7MP2011S40 Min.	Max.	7MP2005S50 7MP2011S50 Min.	Max.	7MP2005S60 7MP2011S60 Min.	Max.	7MP2005S70 7MP2011S70 Min.	Max.	7MP2005S85 7MP2011S85 Min.	Max.	7MP2005S120 7MP2011S120 Min.	Max.	Unit
t_{RC}	Read Cycle Time	50	—	65	—	75	—	85	—	105	—	140	—	ns
t_A	Access Time	—	40	—	50	—	60	—	70	—	85	—	120	ns
t_{RR}	Read Recovery Time	10	—	15	—	15	—	15	—	20	—	20	—	ns
t_{RPW}(1)	Read Pulse Width	40	—	50	—	60	—	70	—	85	—	120	—	ns
t_{RLZ}(2)	Read Pulse Low to Data Bus at Low Z	5	—	10	—	10	—	10	—	10	—	10	—	ns
t_{WLZ}(2)	Write Pulse High to Data Bus at Low Z	10	—	15	—	15	—	15	—	20	—	20	—	ns
t_{DV}	Data Valid from Read Pulse High	5	—	5	—	5	—	5	—	5	—	5	—	ns
t_{RHZ}(2)	Read Pulse High to Data Bus at High Z	—	25	—	30	—	30	—	30	—	30	—	35	ns
t_{WC}	Write Cycle Time	50	—	65	—	75	—	85	—	105	—	140	—	ns
t_{WPW}(1)	Write Pulse Width	40	—	50	—	60	—	70	—	85	—	120	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	15	—	15	—	20	—	20	—	ns
t_{DS}	Data Set-up Time	20	—	30	—	30	—	30	—	40	—	40	—	ns
t_{DH}	Data Hold Time	0	—	5	—	5	—	10	—	10	—	10	—	ns
t_{RSC}	Reset Cycle Time	50	—	65	—	75	—	85	—	105	—	140	—	ns
t_{RS}(1)	Reset Pulse Width	40	—	50	—	60	—	70	—	85	—	120	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	15	—	15	—	20	—	20	—	ns
t_{EFL}	Reset to Emtpy Flag Low	—	50	—	65	—	75	—	85	—	105	—	140	ns
t_{REF}	Read Low to Emtpy Flag Low	—	40	—	50	—	60	—	70	—	85	—	120	ns
t_{RFF}	Read High to Full Flag High	—	40	—	50	—	60	—	70	—	85	—	120	ns
t_{WEF}	Write High to Empty Flag High	—	40	—	50	—	60	—	70	—	85	—	120	ns
t_{WFF}	Write Low to Full Flag Low	—	40	—	50	—	60	—	70	—	85	—	120	ns

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NOTES:
1. Pulse widths less than minimum value are not allowed.
2. This parameter is guaranteed by design but not tested.

8

SIGNAL DESCRIPTIONS:

INPUTS:

DATA IN (D_0-D_8)

Data Inputs for 9-bit wide data path.

CONTROLS:

RESET ($\overline{RS}$)

Reset is accomplished whenever the RESET ($\overline{RS}$) input is taken to a low state. During RESET, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. Both the READ ENABLE ($\overline{R}$) and WRITE ENABLE ($\overline{W}$) inputs must be in the high state during reset.

WRITE ENABLE ($\overline{W}$)

A write cycle is initiated on the falling edge of this input if the FULL FLAG ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect the the rising edge of the WRITE ENABLE ($\overline{W}$). Data is stored in the RAM array sequentially and independently of any ongoing read operation.

To prevent data overflow, the FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operations. Upon the completion of a valid read operation, the FULL FLAG ($\overline{FF}$) will go high after t_{RFF}, allowing a valid write to begin.

READ ENABLE ($\overline{R}$)

A read cycle is initiated on the falling edge of the READ ENABLE ($\overline{R}$) provided the EMPTY FLAG ($\overline{EF}$) is not set. The data is accessed on a first-in/first-out basis independent of any ongoing write operations. After READ ENABLE ($\overline{R}$) goes high, the Data Outputs (Q_0 through Q_8) will return to a high impedance condition until the next READ operation. When all the data has been read from the FIFO, the EMPTY FLAG ($\overline{EF}$) will go low, inhibiting further read operations with the data outputs remaining in a high impedance state. Once a valid write operation has been accomplished, the EMPTY FLAG ($\overline{EF}$) will go high after t_{WEF} and a valid READ can then begin.

FIRST LOAD ($\overline{FL}$)

This pin is grounded to indicate that it is the first device. In the multiple module (depth expansion mode) application, this pin on the rest of devices should connect to Vcc for proper operation.

EXPANSION IN ($\overline{XI}$)

EXPANSION IN ($\overline{XI}$) is connected to EXPANSION OUT ($\overline{XO}$) of the previous (in depth expansion) or same device for proper applications.

OUTPUTS:

FULL FLAG ($\overline{FF}$)

The FULL FLAG ($\overline{FF}$) will go low, inhibiting further write operation, when the write pointer is one location from the read pointer, indicating that the device is full. If the read pointer is not moved after RESET ($\overline{RS}$), the FULL FLAG ($\overline{FF}$) will go low after 8,192 writes for the IDT7MP2005 and 16,384 writes for the IDT7MP2011.

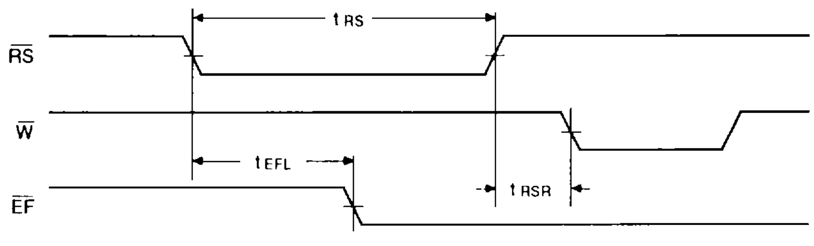
EXPANSION OUT ($\overline{XO}$)

EXPANSION OUT ($\overline{XO}$) is connected to the EXPANSION IN ($\overline{XI}$) of the same device (single device mode) or the EXPANSION IN ($\overline{XI}$) of the next device (multiple device, depth expansion mode) for proper operation. This output acts as a signal to the next device by providing a pulse to the next device when the current device reaches the last location of memory.

DATA OUTPUTS (Q_0-Q_8)

Data outputs for a 9-bit wide data path. This output is in a high impedance condition whenever READ ($\overline{R}$) is in a high state.

TIMING WAVEFORM OF RESET CYCLE[1,2]



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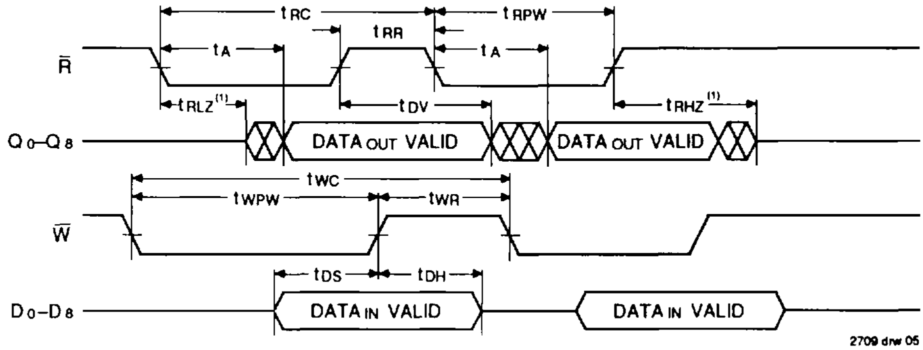
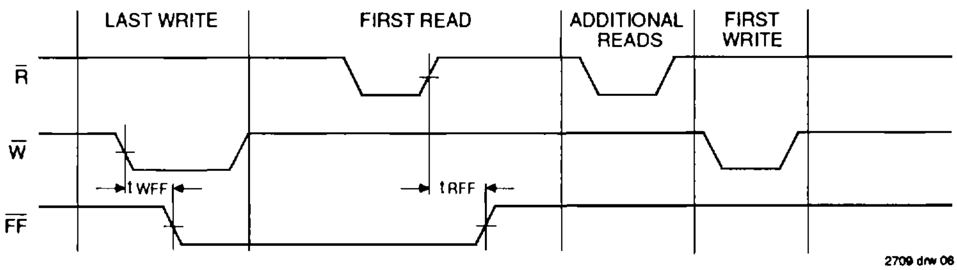
NOTES:
1. $t_{RSC} = t_{RS} + t_{RSR}$
2. $\overline{W}$ and $\overline{R}$ = V_{IH} during RESET.

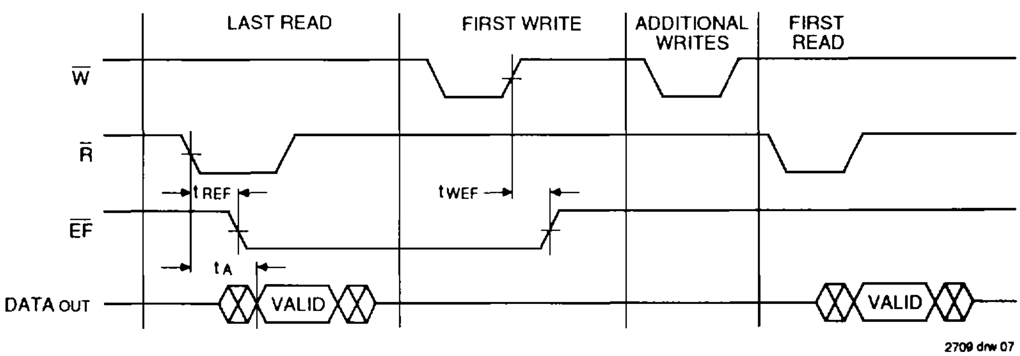
TIMING WAVEFORM OF ASYNCHRONOUS WRITE AND READ OPERATION



TIMING WAVEFORM FOR THE FULL FLAG FROM LAST WRITE TO FIRST READ



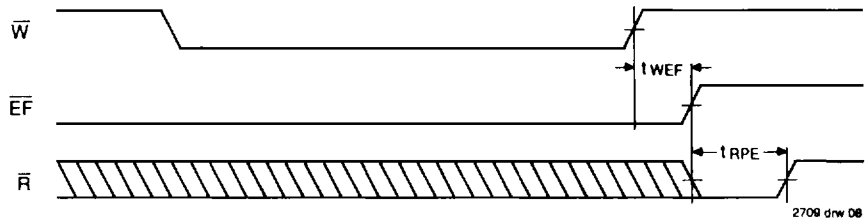
TIMING WAVEFORM FOR THE EMPTY FLAG FROM LAST READ TO FIRST WRITE



NOTE:
1. This parameter is guaranteed by design but not tested.

TIMING WAVEFORM OF THE EMPTY FLAG CYCLE

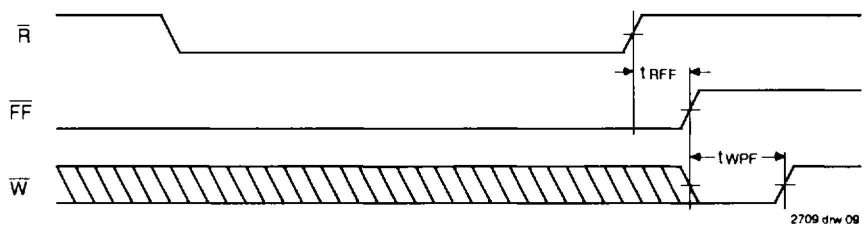
t_{RPE} EFFECTIVE READ PULSE WIDTH AFTER FULL FLAG HIGH [1]



NOTE:
1. ($t_{RPE} = t_{RPW}$)

TIMING WAVEFORM OF THE FULL FLAG CYCLE

t_{RPE} EFFECTIVE READ PULSE WIDTH AFTER FULL FLAG HIGH [1]



NOTE:
1. ($t_{WPF} = t_{WPW}$)

OPERATING MODES

SINGLE DEVICE MODE

A single IDT7MP2005/2011 may be used when the application requirements are for 8,192/16,384 words or less. The IDT7MP2005/2011 is in a Single Device Configuration when the EXPANSION IN ($\overline{XI}$) control input is connected to the EXPANSION OUT ($\overline{XO}$) of the device and the FIRST LOAD ($\overline{FL}$) control pin is grounded (see Figure 8).

WIDTH EXPANSION MODE

Word width may be increased simply by connecting the corresponding input control signals of multiple devices. Status flags ($\overline{EF}$ and $\overline{FF}$) can be detected from any one device. Figure 9 demonstrates an 18-bit word width by using two IDT7MP2005/2011. Any word width can be attained by adding additional IDT7MP2005/2011s.

DEPTH EXPANSION (DAISY CHAIN) MODE

The IDT7MP2005/2011 can easily be adapted to applications when the requirements are for greater than 8,192/16,384 words. Figure 10 demonstrates Depth Expansion using three IDT7MP2005/2011. Any depth can be attained by adding additional IDT7MP2005/2011s. The IDT7MP2005/2011 operate in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the FIRST LOAD ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the high state.
3. The EXPANSION OUT ($\overline{XO}$) pin of each device must be tied to the EXPANSION IN ($\overline{XI}$) pin of the next device. (See Figure 10.)
4. External logic is needed to generate a composite FULL FLAG ($\overline{FF}$) and EMPTY FLAG ($\overline{EF}$). This requires the logical ANDing of all $\overline{EF}$s and logical ANDing of all $\overline{FF}$s (i.e. all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$). (See Figure 10.)

COMPOUND EXPANSION MODE

The two expansion techniques described above can be applied together in a straight forward manner to achieve large FIFO arrays. (See Figure 11.)

BIDIRECTIONAL MODE

Applications which require data buffering between two systems (each system capable of READ and WRITE operations) can be achieved by pairing IDT7MP2005/2011s as shown in Figure 12. Care must be taken to assure that the appropriate flag is monitored by each system (i.e. $\overline{FF}$ is monitored on the device where $\overline{W}$ is used; $\overline{EF}$ is monitored on the device where $\overline{R}$ is used). Both Depth Expansion and Width Expansion may be used in this mode.

DATA FLOW-THROUGH MODES

Two types of flow-through modes are permitted with the IDT7MP2005/2011: a read flow-through mode and write flow-through mode. For the read flow-through mode (Figure 13), the FIFO permits a reading of a single word of data immediately after writing one word of data into the completely empty FIFO.

In the write flow-through mode (Figure 14), the FIFO permits a writing of a single word of data immediately after reading one word of data from a completely full FIFO.

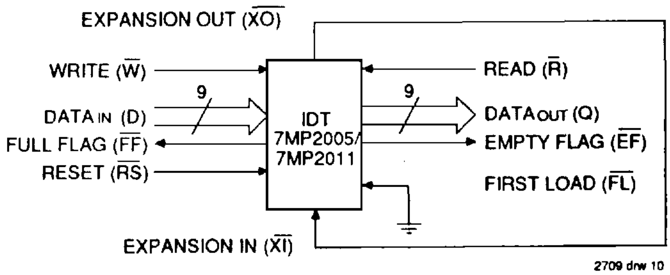
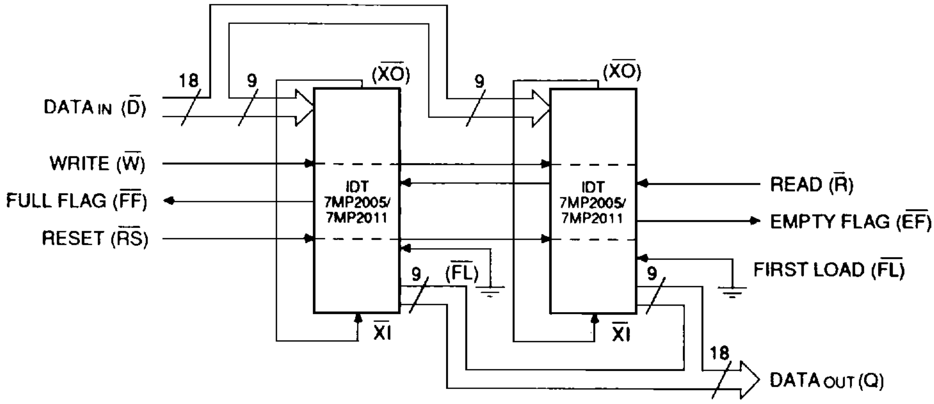


Figure 8. Block Diagram of Single IDT7MP2005/7MP2011 FIFO



NOTE:
1. Flag detection is accomplished by monitoring the FF and EF signals on either (any) device used in the width expansion configuration. Do not connect any output control signals together.

Figure 9. Block Diagram of 8,192 x 18/16,384 x 18 FIFO Memory Used In Width Expansion Mode

TRUTH TABLES
TABLE I—RESET

Single Device Configuration/Width Expansion Mode

Mode	Inputs		Internal Status		Outputs	
	RS	XI	Read Pointer	Write Pointer	EF	FF
Reset	0	0	Location Zero	Location Zero	0	1
Read/Write	1	0	Increment(1)	Increment(1)	X	X

NOTE:
1. Pointer will increment if flag is High.

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TABLE II—RESET AND FIRST LOAD TRUTH TABLE

Depth Expansion/Compound Expansion Mode

Mode	Inputs			Internal Status		Outputs	
	RS	FL	XI	Read Pointer	Write Pointer	EF	FF
Reset First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

NOTE:
1. XI is connected to XO of previous device. See Figure 10.
2. RS = Reset Input, FL = First Load, EF = Empty Flag Output, FF = Flag Full Output, XI = Expansion Input.

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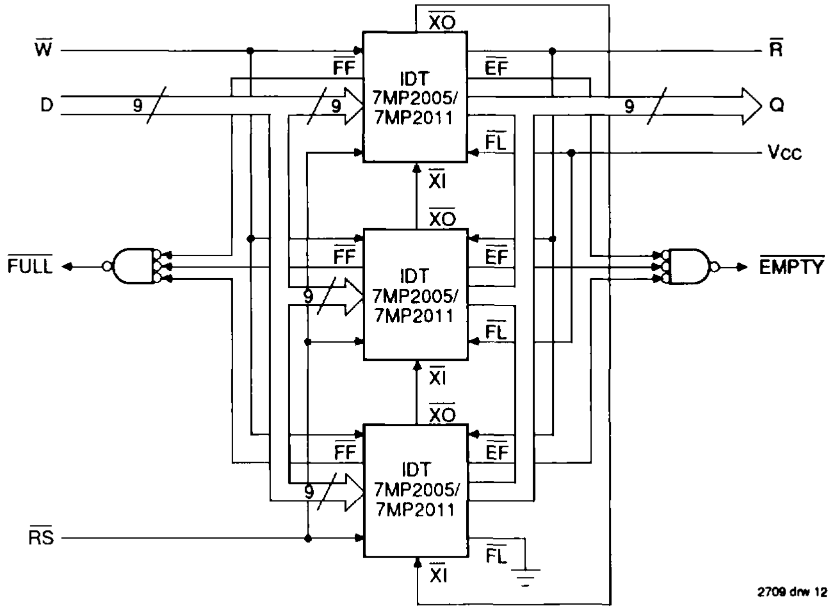

Figure 10. Block Diagram of 24,576 x 9/49,152 x 9 FIFO Memory (Depth Expansion)

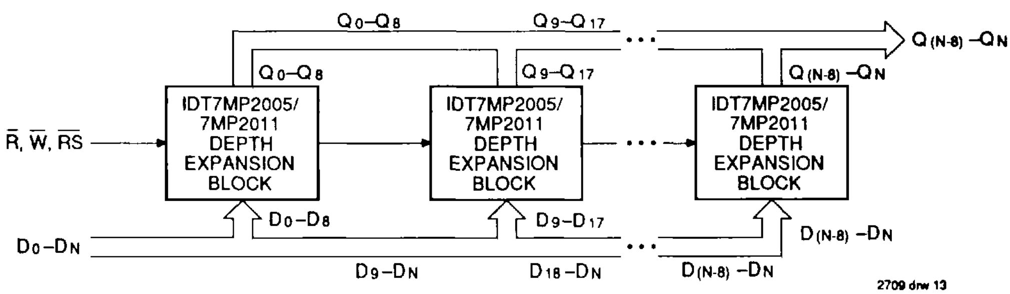

Figure 11. Compound FIFO Expansion

NOTES:
1. For depth expansion block see DEPTH EXPANSION Section and Figure 10.
2. For Flag detection see WIDTH EXPANSION Section and Figure 9.

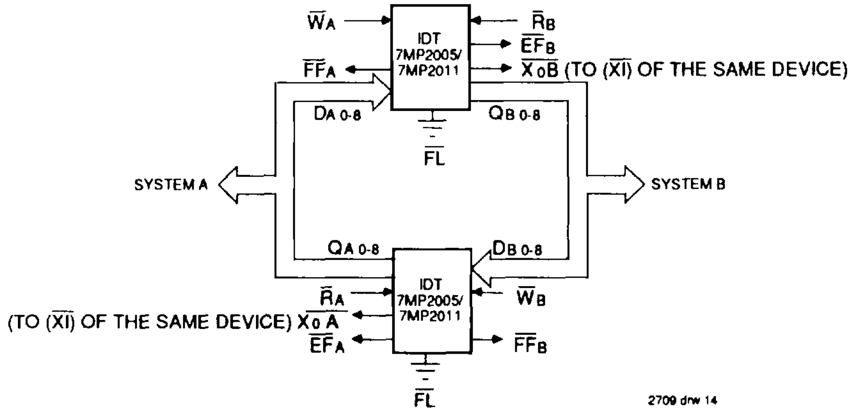

Figure 12. Bidirectional FIFO Mode

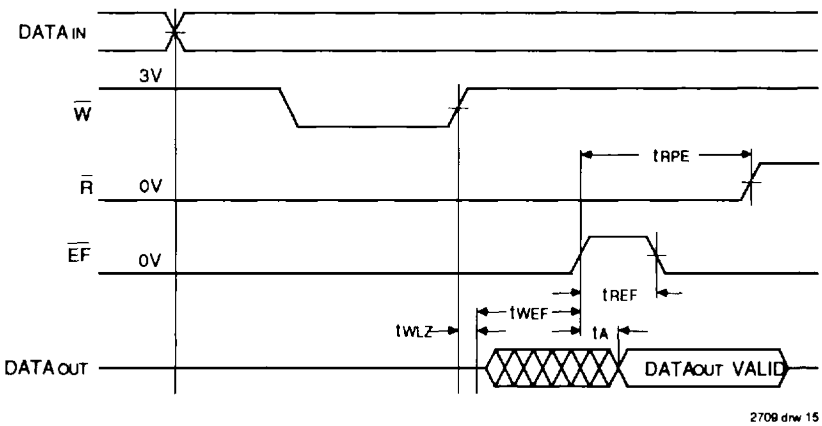

Figure 13. Read Data Flow-Through Mode

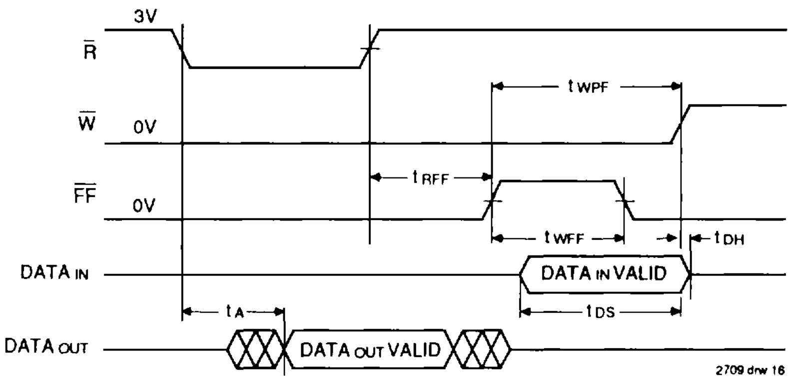

Figure 14. Write Data Flow-Through Mode

ORDERING INFORMATION

IDT XXXX A 999 A A

IDT	XXXX	A	999	A	A
	Device Type	Power	Speed	Package	Process/ Temperature Range

Code	Description
Blank	Commercial (0°C to+70°C)
V	FR-4 DSIP (Dual Single In-line Package)
20, 25, 30, 35, 40, 50, 60, 70, 85, 120	Speed in Nanoseconds
S	Standard Power
7MP2005	8K x 9 FIFO Module
7MP2011	16K x 9 FIFO Module

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