PS9402

R08DS0014EJ0001
Rev.0.01
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2.5 A OUTPUT CURRENT, HIGH CMR, IGBT, POWER MOS FET GATE DRIVE, 16-PIN SSOP PHOTOCOUPLER

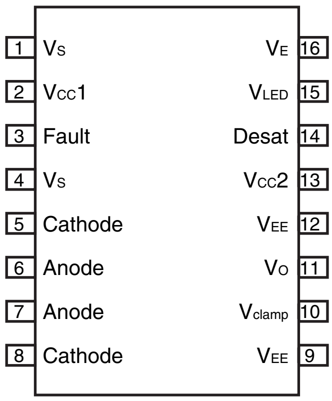
DESCRIPTION

The PS9402 is an optically coupled isolator containing a GaAlAs LED on the input side and a photo diode, a signal processing circuit and a power output transistor on the output side on one chip.
The PS9402 is designed specifically for high common mode transient immunity (CMR), high output current and high switching speed.
The PS9402 includes desaturation detection and active miller clamping functions.
The PS9402 is suitable for driving IGBTs and Power MOS FETs.
The PS9402 is in a 16-pin plastic SSOP (Shrink Small Outline Package). And the PS9402 is able to high-density (surface) mounting.

FEATURES

- Long creepage distance (8 mm MIN.)
- Large peak output current (2.5 A MAX., 2.0 A MIN.)
- High speed switching (t_{PLH}, t_{PHL} = 200 ns MAX.)
- UVLO (Under Voltage Lock Out) protection with hysteresis
- Desaturation detection
- Miller clamping
- High common mode transient immunity (CM_H, CM_L = ±25 kV/μs MIN.)
- Embossed tape product: PS9402-E3: 850 pcs/reel
- Pb-Free product
- Safety standards
  - UL awaiting approval
  - CSA awaiting approval
  - DIN EN60747-5-2 (VDE0884 Part2) awaiting approval

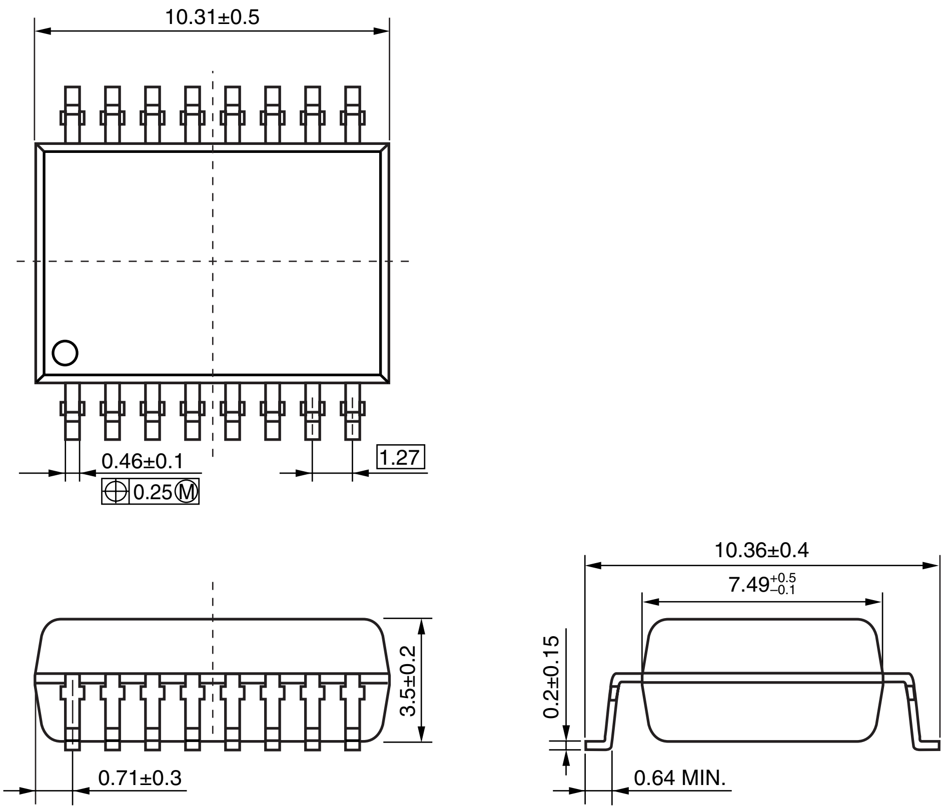
PIN CONNECTION
(Top View)



APPLICATIONS

- IGBT, Power MOS FET Gate Driver
- Industrial inverter
- Uninterruptible Power Supply (UPS)

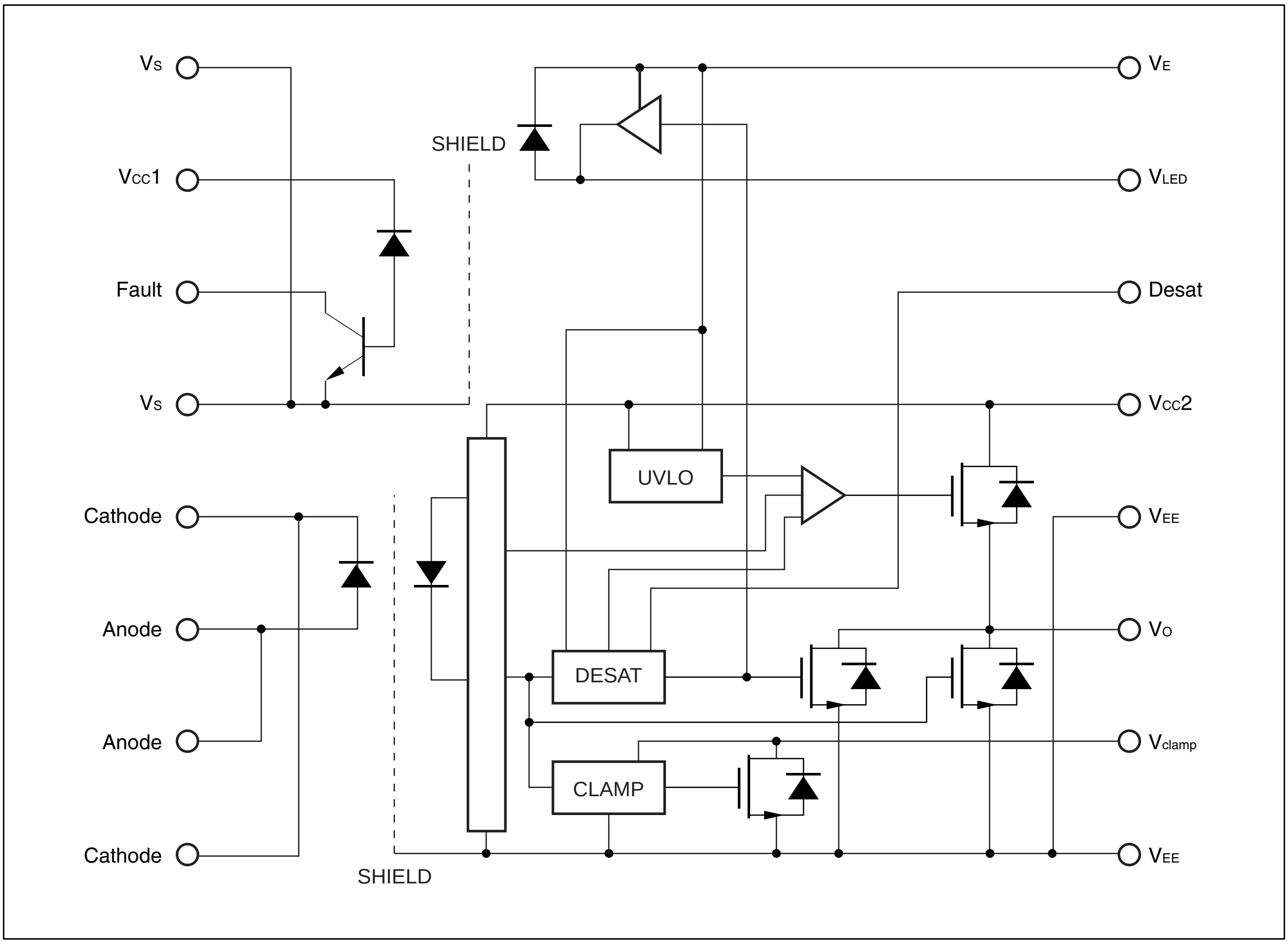
PACKAGE DIMENSIONS (UNIT: mm)



PHOTOCOUPLER CONSTRUCTION

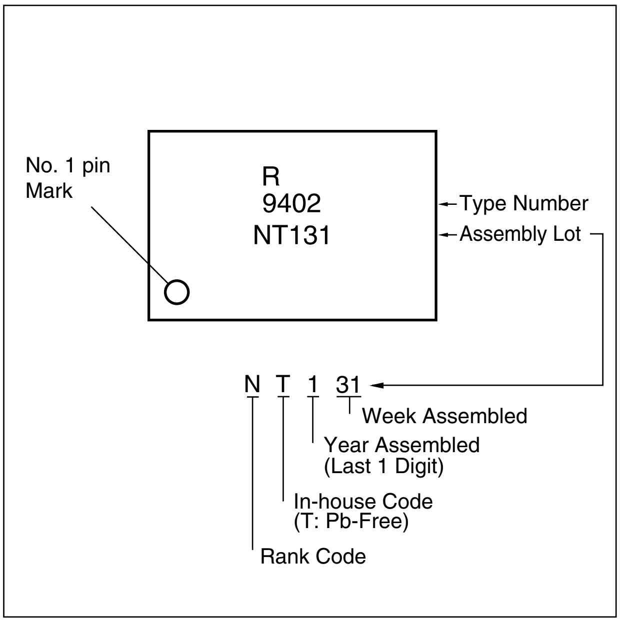
Parameter	Unit (MIN.)
Air Distance	8 mm
Outer Creepage Distance	8 mm
Isolation Distance	0.4 mm

BLOCK DIAGRAM(UNIT: mm)



IF	UVLO (V_{CC2}–V_{EE})	DESAT	FAULT	V_O
Don't care	Active (<V_{UVLO-})	Don't care	Undefined	Low
Don't care	Don't care	High (>V_{DESAT})	Low	Low
OFF	Don't care	Don't care	Undefined	Low
ON	Not Active (>V_{UVLO+})	Low (<V_{DESAT})	High	High

MARKING EXAMPLE



ORDERING INFORMATION

Part Number	Order Number	Solder Plating Specification	Packing Style	Safety Standard Approval	Application Part Number*1
PS9402	PS9402-AX	Pb-Free (Ni/Pd/Au)	10 pcs (Tape 10 pcs cut)	Standard products (UL and CSA awaiting approval)	PS9402
PS9402-E3	PS9402-E3-AX		Embossed Tape 850 pcs/reel		
PS9402-V	PS9402-V-AX		10 pcs (Tape 10 pcs cut)	DIN EN60747-5-2 (VDE0884 Part2) awaiting approval (Option)	
PS9402-V-E3	PS9402-V-E3-AX		Embossed Tape 850 pcs/reel		

Note: *1. For the application of the Safety Standard, following part number should be used.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Forward Current	I_F	25	mA
Peak Transient Forward Current (Pulse Width < 1 μs)	$I_{F\ (TRAN)}$	1.0	A
Reverse Voltage	V_R	5	V
Input Supply Voltage	$V_{CC}1$	0 to 5.5	V
Input IC Power Dissipation *1	P_I	80	mW
High Level Peak Output Current *2	$I_{OH\ (PEAK)}$	2.5	A
Low Level Peak Output Current *2	$I_{OL\ (PEAK)}$	2.5	A
FAULT Output Current	I_{FAULT}	8	mA
FAULT Pin Voltage	V_{FAULT}	0 to $V_{CC}1$	V
Total Output Supply Voltage	$(V_{CC}2–V_{EE})$	0 to 33	V
Negative Output Supply Voltage	$(V_E–V_{EE})$	0 to 15	V
Output Voltage	V_O	0 to $V_{CC}2$	V
Peak Clamping Sinking Current	I_{Clamp}	1.7	A
Miller Clamping Pin Voltage	V_{Clamp}	0 to $V_{CC}2$	V
DESAT Voltage	V_{DESAT}	V_E to V_E+10	V
Output IC Power Dissipation *3	P_O	300	mW
Isolation Voltage *4	BV	5 000	Vr.m.s.
Operating Ambient Temperature	T_A	–40 to +110	°C
Storage Temperature	T_{stg}	–55 to +125	°C

Notes: *1. Reduced to 1.6 mW/°C at T_A = 75°C or more.
*2. Maximum pulse width = 10 μs, Maximum duty cycle = 0.5%
*3. Reduced to 5.5 mW/°C at T_A = 70°C or more.
*4. AC voltage for 1 minute at T_A = 25°C, RH = 60% between input and output. Pins 1-8 shorted together, 9-16 shorted together.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	MAX.	Unit
Total Output Supply Voltage	$(V_{CC}2–V_{EE})$	15	30	V
Negative Output Supply Voltage	$(V_E–V_{EE})$	0	15	V
Positive Output Supply Voltage	$(V_{CC}2–V_E)$	15	30– (V_E – V_{EE})	V
Forward Current (ON)	$I_{F\ (ON)}$	8	12	mA
Forward Voltage (OFF)	$V_{F\ (OFF)}$	–2	0.8	V
Operating Ambient Temperature	T_A	–40	110	°C

ELECTRICAL CHARACTERISTICS (DC) (at RECOMMENDED OPERATING CONDITIONS, $V_{EE} = V_E$ = GND, unless otherwise specified)

Parameter	Symbol	Conditions	MIN.	TYP.[*1]	MAX.	Unit
FAULT Logic Low Output Voltage	V_{FAULTL}	I_{FAULT} = 1.1 mA		0.1		V
FAULT Logic High Output Current	I_{FAULTH}	V_{FAULT} = 5.5 V, $V_{CC}1$ = 5.5 V, T_A = 25°C			0.5	μA
High Level Output Current	I_{OH}	$V_O = (V_{CC}–4\ V)$ [*2]	0.5	1.5		A
		$V_O = (V_{CC}–15\ V)$ [*3]	2.0			
Low Level Output Current	I_{OL}	$V_O = (V_{EE}+2.5\ V)$ [*2]	0.5	1.5		A
		$V_O = (V_{EE}+15\ V)$ [*3]	2.0			
Low Level Output Current During Fault Condition	I_{OLF}	$V_O–V_{EE}$ = 14 V	90	140	230	mA
High Level Output Voltage	V_{OH}	I_O = 100 mA [*4]	V_{CC} – 2.0	V_{CC} – 1.3		V
		I_O = –650 μA [*4]	V_{CC} – 1.5	V_{CC} – 0.8		
Low Level Output Voltage	V_{OL}	I_O = 100 mA		0.15	0.5	V
Clamp Pin Threshold Voltage	V_{tClamp}			2.0		V
Clamp Low Level Sinking Current	I_{CL}	$V_{tClamp} = V_{EE}$ + 2.5V	0.35	1.5		A
High Level Supply Current	$I_{CC}2_H$	I_O = 0 mA		2	3	mA
Low Level Supply Current	$I_{CC}2_L$	I_O = 0 mA		2	3	mA
Blanking Capacitor Charging Current	I_{CHG}	V_{DESAT} = 2 V	0.13	0.24	0.33	mA
Blanking Capacitor Discharging Current	I_{DSCHG}	V_{DESAT} = 7 V	10	30		mA
DESAT Threshold	V_{DESAT}	$V_{CC}1–V_E > V_{UVLO–}$, V_O < 5V	6.0	6.9	7.5	V
UVLO Threshold [*5]	V_{UVLO+}	V_O > 5 V	11.0	12.3	13.5	V
	$V_{UVLO–}$	V_O < 5 V	9.8	11.0	12.3	
UVLO Hysteresis	$V_{UVLO+}–V_{UVLO–}$		0.4	1.3		V
Threshold Input Current (L → H)	I_{FLH}	I_O = 0 mA, V_O > 5 V		1.5	5	mA
Threshold Input Voltage (H → L)	V_{FHL}	I_O = 0 mA, V_O < 5 V	0.8			V
Input Forward Voltage	V_F	I_F = 10 mA, T_A = 25°C	1.2	1.56	1.8	V
Input Reverse Current	I_R	V_R = 3V, T_A = 25°C			10	μA
Input Capacitance	C_{IN}	f = 1 MHz, V_F = 0 V		30		pF

Notes: *1. Typical values at T_A = 25°C.
*2. Maximum pulse width = 50 μs, Maximum duty cycle = 0.2%
*3. Maximum pulse width = 10 μs, Maximum duty cycle = 0.5%
*4. V_{OH} is measured with the DC load current in this testing (Maximum pulse width = 1 ms, Maximum duty cycle = 20%).
*5. For High Level Output Voltage testing, V_{OH} is measured with the DC load current. When driving capacitive loads, V_{OH} will approach V_{CC} as I_{OH} approaches zero units.

SWITCHING CHARACTERISTICS (AC) (at RECOMMENDED OPERATING CONDITIONS, $V_{EE} = V_E$ = GND, unless otherwise specified)

Parameter	Symbol	Conditions	MIN.	TYP.[*1]	MAX.	Unit
Propagation Delay Time (L → H)	t_{PLH}	R_g = 10 Ω, C_g = 10 nF, f = 10 kHz, Duty Cycle = 50%[*2], I_F = 10 mA, $V_{CC}2$ = 30 V	50	100	200	ns
Propagation Delay Time (H → L)	t_{PHL}		50	100	200	ns
Pulse Width Distortion (PWD)	$\|t_{PHL}-t_{PLH}\|$			20	100	ns
Rise Time	t_r			50		ns
Fall Time	t_f			50		ns
Common Mode Transient Immunity at High Level Output[*3]	CM_H1	T_A = 25°C, I_F = 10 mA, $V_{CC}2$ = 30 V, V_{CM} = 1.5 kV, C_{DESAT} = 100 pF, R_F = 2.1 kΩ, $V_{CC}1$ = 5 V	25			kV/μs
Common Mode Transient Immunity at Low Level Output[*4]	CM_L1	T_A = 25°C, V_F = 0 V, $V_{CC}2$ = 30 V, V_{CM} = 1.5 kV, R_F = 2.1 kΩ, $V_{CC}1$ = 5 V			–25	kV/μs
DESAT Sense to 90% V_O Delay[*5]	$t_{DESAT (90\%)}$	C_{DESAT} = 100 pF, R_F = 2.1 kΩ, R_g = 10 Ω, C_g = 10 nF $V_{CC}2$ = 30 V		250	500	ns
DESAT Sense to 10% V_O Delay	$t_{DESAT (10\%)}$			2	3	μs
DESAT Sense to Low Level FAULT Signal Delay[*6]	$t_{DESAT (FAULT)}$			400	800	ns
DESAT Sense to DESAT Low Propagation Delay[*5]	$t_{DESAT (LOW)}$			250		ns
DESAT Input Mute[*7]	$t_{DESAT (MUTE)}$		5			μs
RESET to High Level FAULT Signal Delay	$t_{RESET (FAULT)}$	$V_{CC}1$ = 5.5 V	0.3	1.2	3.0	μs
		$V_{CC}1$ = 3.3 V	0.5	1.5	4.0	μs

Notes: *1. Typical values at T_A = 25°C.

*2. This load condition is equivalent to the IGBT load at 1 200 V/150 A.

*3. Common mode transient immunity in the high state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in the high state (i.e., V_O > 15 V or FAULT > 2 V). A 100 pF and a 2.1kΩ pull-up resistor is needed in fault detection mode.

*4. Common mode transient immunity in the low state is the maximum tolerable dV_{CM}/dt of the common mode pulse, V_{CM}, to assure that the output will remain in a low state (i.e., V_O < 1.0 V or FAULT < 0.8 V).

*5. This is the amount of time the DESAT threshold must be exceeded before V_{OUT} begins to go low, and the FAULT output to go low. This is supply voltage dependent.

*6. This is the amount of time from when the DESAT threshold is exceeded, until the FAULT output goes low.

*7. Auto Reset: This is the amount of time when V_{OUT} will be asserted low after DESAT threshold is exceeded. See the Description of Operation (Auto Reset) topic in the application information section.

TEST CIRCUIT

Fig. 1 V_{FAULTL} Test Circuit

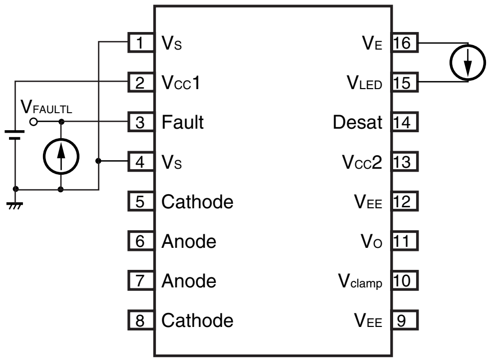


Fig. 2 I_{FAULTH} Test Circuit

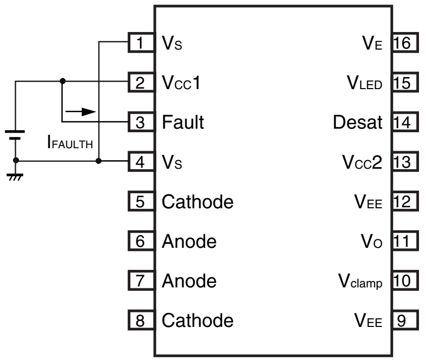


Fig. 3 I_{OH} Test Circuit

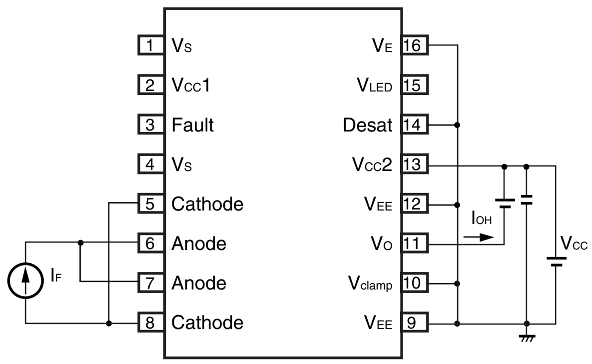


Fig. 4 I_{OL} Test Circuit

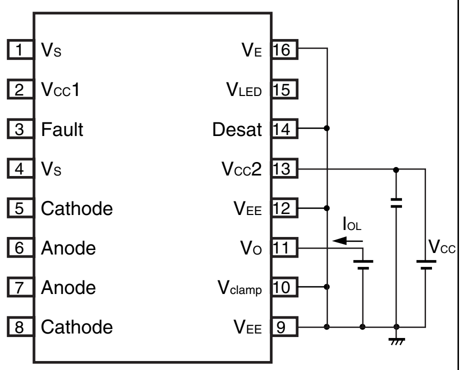


Fig. 5 V_{OH} Test Circuit

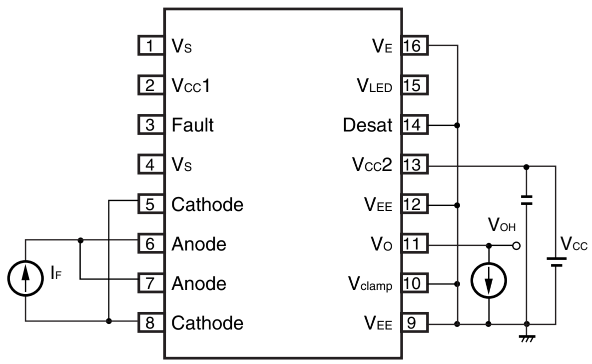
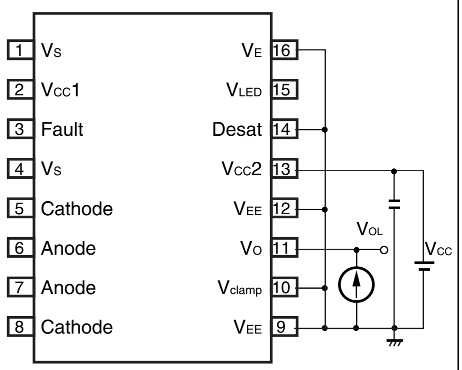


Fig. 6 V_{OL} Test Circuit



TEST CIRCUIT 2

Fig. 7 I_{CC2H} Test Circuit

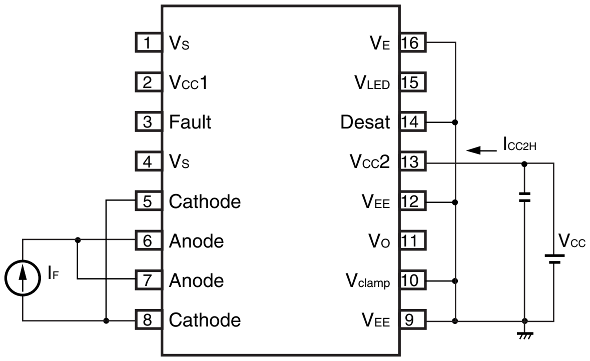


Fig. 8 I_{CC2L} Test Circuit

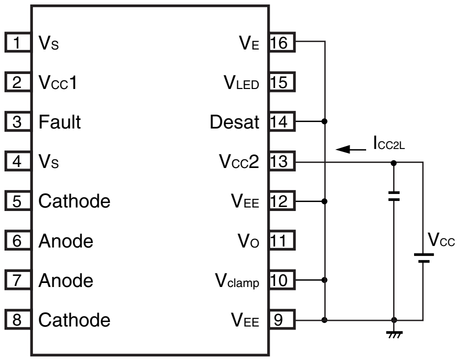


Fig. 9 I_{CHG} Test Circuit

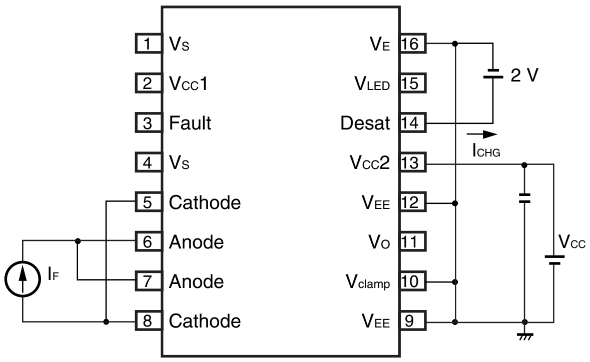


Fig. 10 I_{DSCHG} Test Circuit

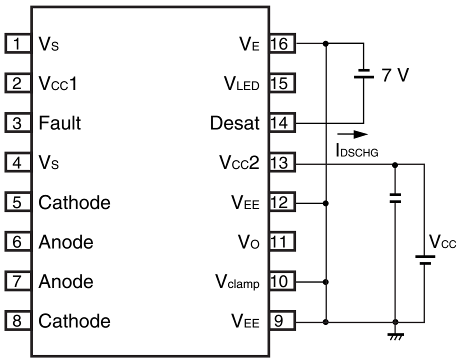


Fig. 11 I_{CL} Test Circuit

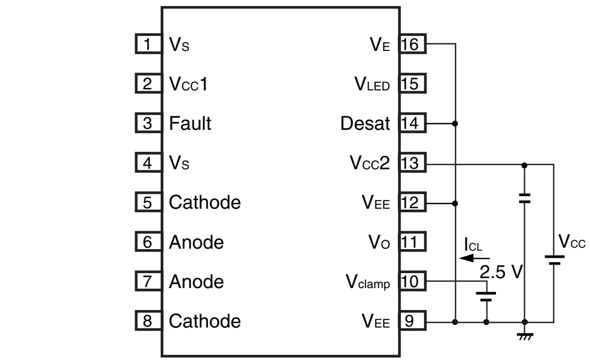
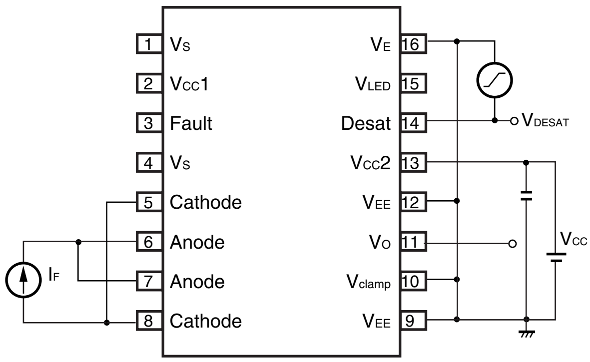


Fig. 12 V_{DESAT} Test Circuit



TEST CIRCUIT 3

Fig. 13 VUVLO Test Circuit

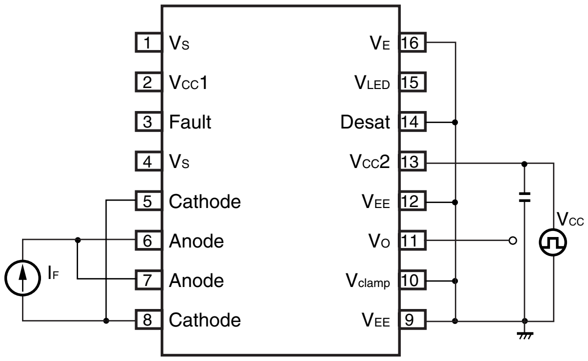


Fig. 14 IFLH Test Circuit

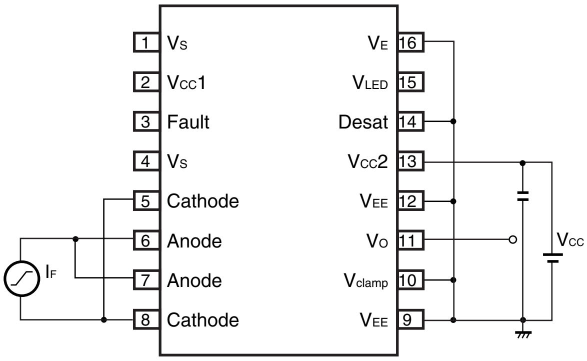


Fig. 15 tPLH/tPHL Test Circuit

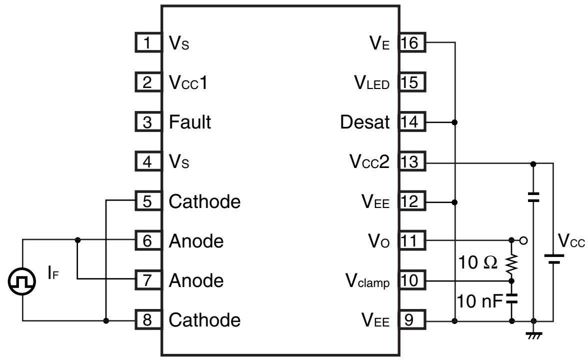


Fig. 17 tPLH/tPHL Test Wave Forms

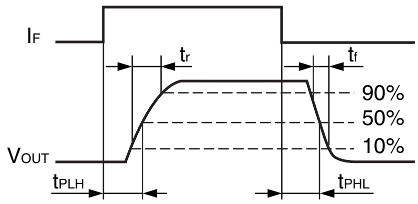


Fig. 17 tDESAT Test Circuit

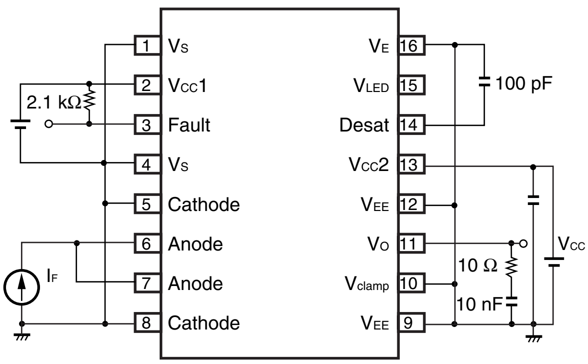
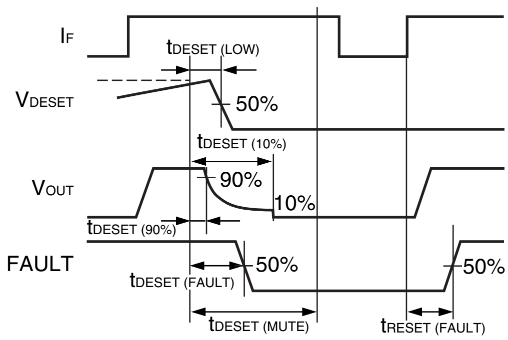


Fig. 18 tDESAT Test Wave Forms



TEST CIRCUIT 4

Fig. 19 CMH Test Circuit (LED1 ON)

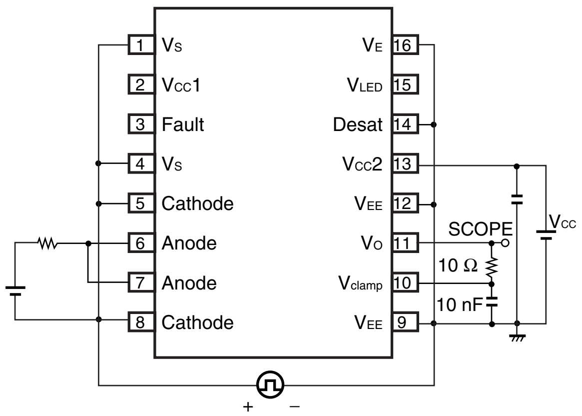


Fig. 20 CML Test Circuit (LED1 OFF)

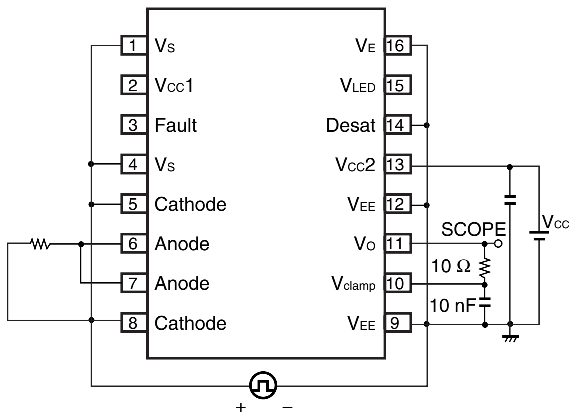


Fig. 21 CMH Test Circuit (LED2 ON)

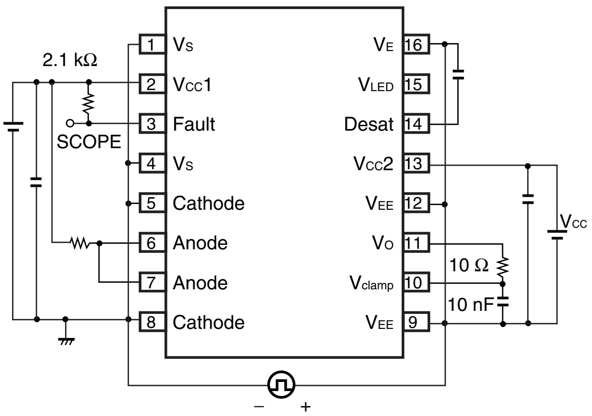


Fig. 22 CML Test Circuit (LED2 OFF)

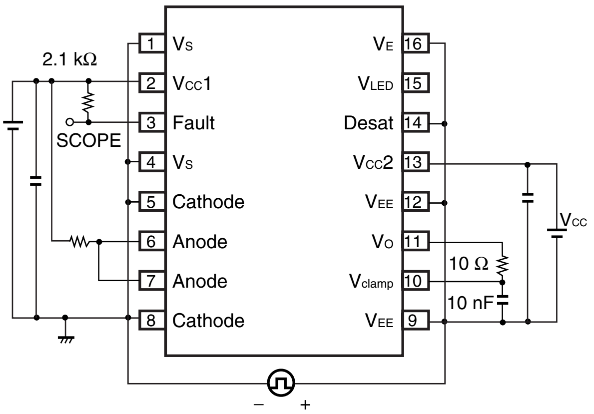


Fig. 23 CMH, CML Test Wave Forms (LED1 ON, OFF)

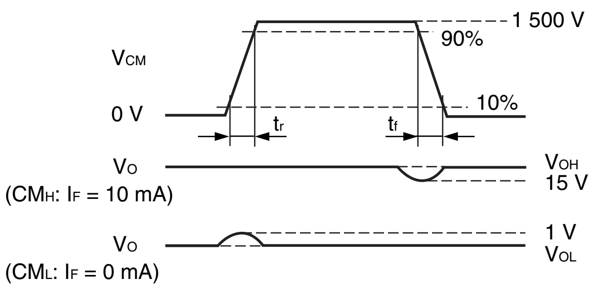
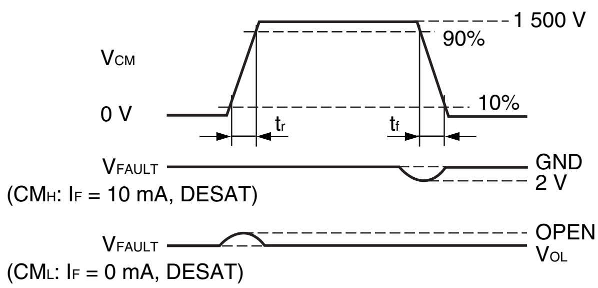
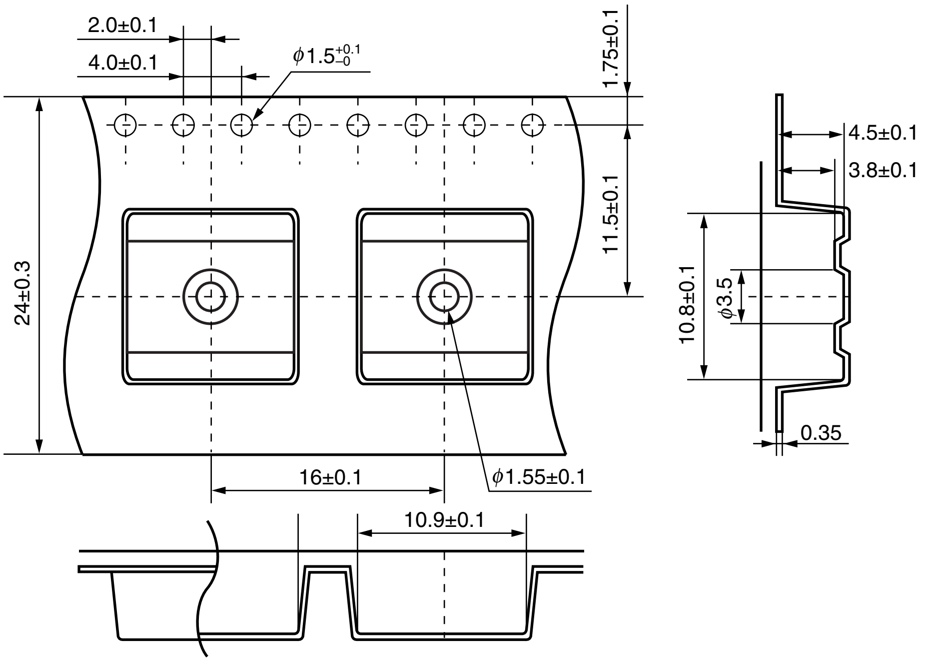


Fig. 24 CMH, CML Test Wave Forms (LED2 ON, OFF)

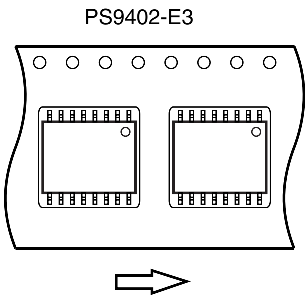


TAPING SPECIFICATIONS (UNIT: mm)

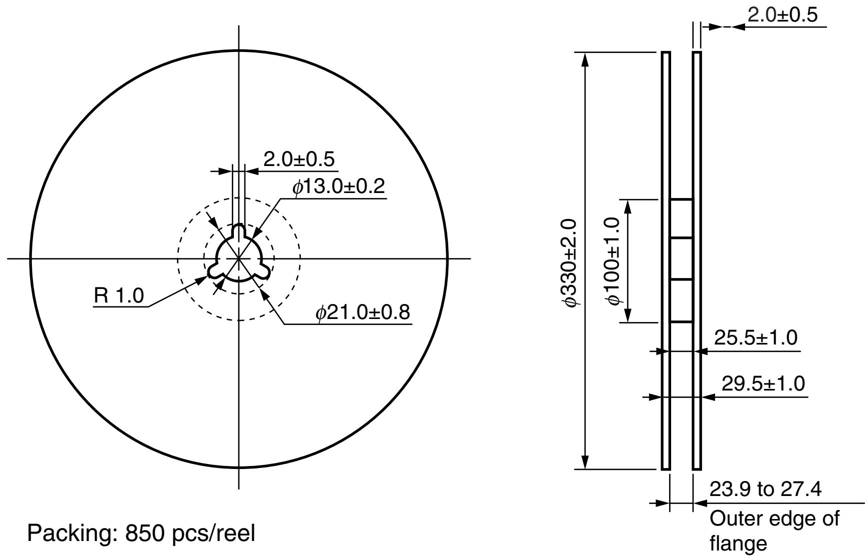
Outline and Dimensions (Tape)



Tape Direction



Outline and Dimensions (Reel)



Packing: 850 pcs/reel

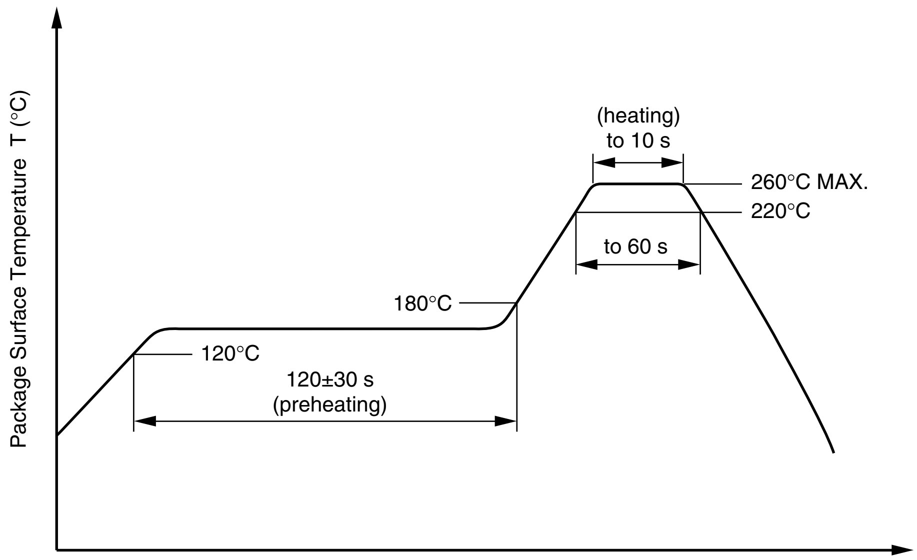
NOTES ON HANDLING

1. Recommended soldering conditions

(1) Infrared reflow soldering

- Peak reflow temperature — 260°C or below (package surface temperature)
- Time of peak reflow temperature — 10 seconds or less
- Time of temperature higher than 220°C — 60 seconds or less
- Time to preheat temperature from 120 to 180°C — 120±30 s
- Number of reflows — Three
- Flux — Rosin flux containing small amount of chlorine (The flux with a maximum chlorine content of 0.2 Wt% is recommended.)

Recommended Temperature Profile of Infrared Reflow



(2) Wave soldering

- Temperature — 260°C or below (molten solder temperature)
- Time — 10 seconds or less
- Preheating conditions — 120°C or below (package surface temperature)
- Number of times — One (Allowed to be dipped in solder including plastic mold portion.)
- Flux — Rosin flux containing small amount of chlorine (The flux with a maximum chlorine content of 0.2 Wt% is recommended.)

(3) Soldering by Soldering Iron

- Peak Temperature (lead part temperature) — 350°C or below
- Time (each pins) — 3 seconds or less
- Flux — Rosin flux containing small amount of chlorine (The flux with a maximum chlorine content of 0.2 Wt% is recommended.)

(a) Soldering of leads should be made at the point 1.5 to 2.0 mm from the root of the lead

(4) Cautions

- Fluxes — Avoid removing the residual flux with freon-based and chlorine-based cleaning solvent.

2. Cautions regarding noise
Be aware that when voltage is applied suddenly between the photocoupler's input and output at startup, the output transistor may enter the on state, even if the voltage is within the absolute maximum ratings.

USAGE CAUTIONS

1. This product is weak for static electricity by designed with high-speed integrated circuit so protect against static electricity when handling.

2. Board designing

(1) By-pass capacitor of more than 0.1 μF is used between V_{CC} and GND near device. Also, ensure that the distance between the leads of the photocoupler and capacitor is no more than 10 mm.

(2) In older to avoid malfunctions and characteristics degradation, IGBT collector or emitter traces should not be closed to the LED input.

3. Make sure the rise/fall time of the forward current is 0.5 μs or less.

4. In order to avoid malfunctions, make sure the rise/fall slope of the supply voltage is 3 V/μs or less.

5. Avoid storage at a high temperature and high humidity.

Caution GaAs Products	This product uses gallium arsenide (GaAs). GaAs vapor and powder are hazardous to human health if inhaled or ingested, so please observe the following points. • Follow related laws and ordinances when disposing of the product. If there are no applicable laws and/or ordinances, dispose of the product as recommended below. 1. Commission a disposal company able to (with a license to) collect, transport and dispose of materials that contain arsenic and other such industrial waste materials. 2. Exclude the product from general industrial waste and household garbage, and ensure that the product is controlled (as industrial waste subject to special control) up until final disposal. • Do not burn, destroy, cut, crush, or chemically dissolve the product. • Do not lick the product or in any way allow it to enter the mouth.

Revision History	PS9402 Preliminary Data Sheet

Rev.	Date	Description	
		Page	Summary
0.01	May 09, 2011	–	First edition issued

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141