QuickLogic PolarPro™ Data Sheet

Combining Low Power, Performance, Density, and Embedded RAM

Device Highlights

Low Power Programmable Logic

- As low as 2.2 µA
- 0.18 µm, six layer metal CMOS process
- 1.8 V core voltage, 1.8/2.5/3.3 V drive capable I/Os
- Up to 221 kilobits of SRAM
- Up to 292 I/Os available
- Up to one million system gates
- Nonvolatile, instant-on
- IEEE 1149.1 boundary scan testing compliant

Embedded Dual-Port SRAM

- Up to twelve dual-port 4-kilobit high performance SRAM blocks (QL1P075, QL1P100, QL1P200, and QL1P300 devices)
- Up to twenty-four dual-port 8-kilobit high performance SRAM blocks (QL1P600 and QL1P1000 devices)
- Embedded synchronous/asynchronous FIFO controller
- Configurable and cascadable aspect ratio

Programmable I/O

- Bank programmable drive strength
- Bank programmable slew rate control
- Independent I/O banks capable of supporting multiple I/O standards in one device
- Native support for DDR I/Os
- Bank programmable I/O standards: LVTTL, LVCMOS, and LVCMOS18

Advanced Clock Network

- Multiple low skew clock networks
  - 1 dedicated global clock network
  - 4 programmable global clock networks
- Quadrant-based segmentable clock networks
  - 20 quad clock networks per device
  - 4 quad clock networks per quadrant
  - 1 dedicated clock network per quadrant
- Two user Configurable Clock Managers (CCMs)

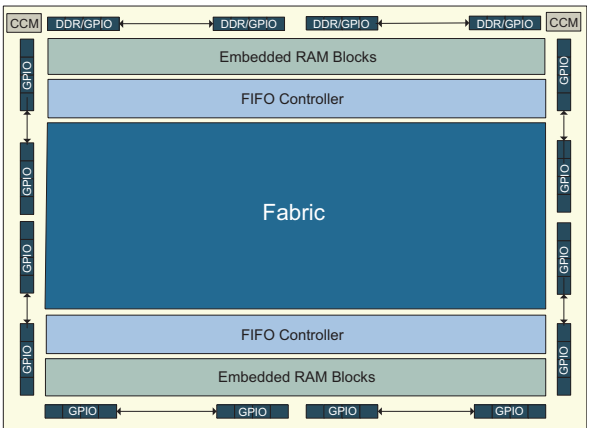
Very Low Power (VLP) Mode

- QuickLogic PolarPro has a special VLP pin which can enable a low power sleep mode that significantly reduces the overall power consumption of the device by placing the device in standby.
- Enter VLP mode from normal operation in less than 250 µs (typical)
- Exit from VLP mode to normal operation in less than 250 µs (typical)

Security Links

There are several security links to disable JTAG access to the device. Programming these optional links completely disables access to the device from the outside world and provides an extra level of design security not possible in SRAM-based FPGAs.

Figure 1: QuickLogic PolarPro Block Diagram



Ultra-Low Power FPGA Combining Performance, Density, and Embedded RAM

Table 1: PolarPro Product Family Members

Features		QL1P075	QL1P100	QL1P200	QL1P300	QL1P600	QL1P1000
Max Gates		75,000	100,000	200,000	300,000	600,000	1,000,000
Logic Cells		512	640	1,536	1,920	4,224	7,680
Max I/O		172	188	292	302	508	652
RAM Modules		8	8	12	12	24	24
FIFO Controllers		8	8	12	12	24	24
RAM bits		36,864	36,864	55,296	55,296	221,184	221,184
CCMs		2[a]	2[a]	2	2	2	2
Packages	TFBGA (0.5 mm)	132	132	132	132	-	-
	TQFP (0.5 mm)	144	144	-	-	-	-
	TFBGA (0.8 mm)	196	196	-	-	-	-
	LBGA (1.0 mm)	256	256	256, 324	256, 324	256, 324	256, 324

a. The PolarPro 144-pin TQFP and 132-pin TFBGA devices have one CCM. The PolarPro 196-pin TFBGA, 256-pin LBGA and 324-pin LBGA devices have two CCMs.

Table 2: Maximum Usable I/Os

Device	132 TFBGA (8 mm x 8 mm)	144 TQFP	196 TFBGA (12 mm x 12 mm)	256 LBGA	324 LBGA
QL1P075	77	97	136	168	-
QL1P100	77	97	136	184	-
QL1P200	74	-	-	184	238[a]
QL1P300	74	-	-	184	238[a]
QL1P600	-	-	-	184[a]	238[a]
QL1P1000	-	-	-	184[a]	238[a]

a. Preliminary.

Process Data

QuickLogic PolarPro is fabricated on a 0.18 µ, six layer metal CMOS process. The core voltage is 1.8 V. The I/O voltage input tolerance and output drive can be set as 1.8 V, 2.5 V, and 3.3 V.

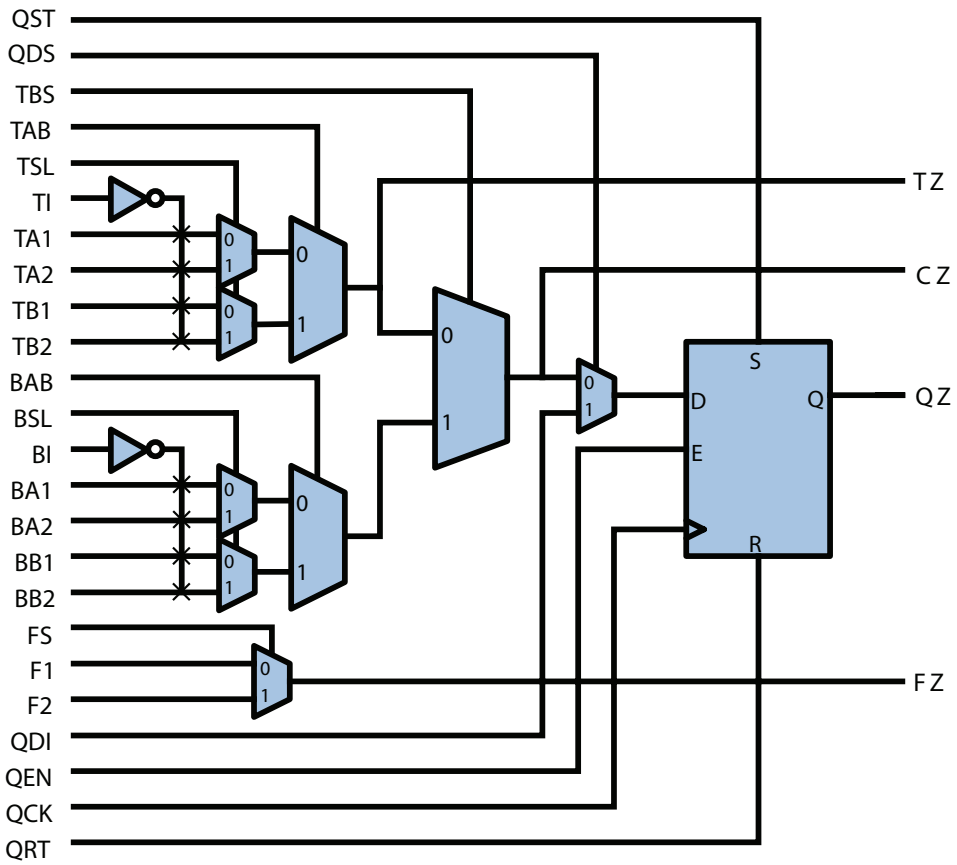
Programmable Logic Architectural Overview

The QuickLogic PolarPro logic cell structure presented in **Figure 2** is a single register, multiplexer-based logic cell. It is designed for wide fan-in and multiple, simultaneous output functions. The cell has a high fan-in, fits a wide range of functions with up to 24 simultaneous inputs (including register control lines), and four outputs (three combinatorial and one registered). The high logic capacity and fan-in of the logic cell accommodates many user functions with a single level of logic delay.

The QuickLogic PolarPro logic cell can implement:

- Two independent 3-input functions
- Any 4-input function
- 8 to 1 mux function
- Independent 2 to 1 mux function
- Single dedicated register with clock enable, active high set and reset signals
- Direct input selection to the register, which allows combinatorial and register logic to be used separately
- Combinatorial logic that can also be configured as an edge-triggered master-slave D flip-flop

Figure 2: PolarPro Logic Cell



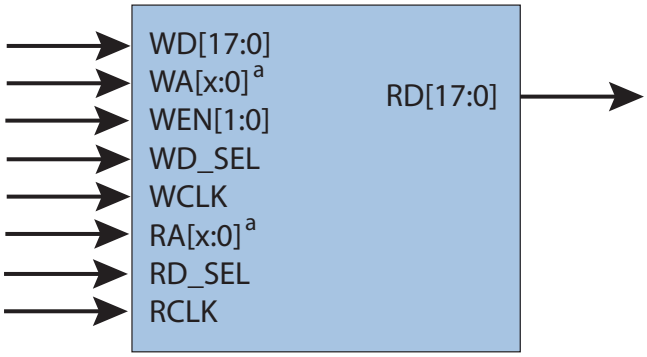
RAM Modules

The PolarPro family of devices include two different RAM block sizes. The QL1P075, QL1P100, QL1P200, and QL1P300 have 4-kilobit (4,608 bits) RAM blocks, while the QL1P600 and QL1P1000 devices have 8-kilobit (9,216 bits) RAM blocks.

The RAM features include:

- Independently configurable read and write data bus widths
- Independent read and write clocks
- Horizontal and vertical concatenation
- Write byte enables
- Selectable pipelined or non-pipelined read data

Figure 3: 4-Kilobit Dual-Port RAM Block



a. x=8 for 4-kilobit RAM blocks, x=9 for 8-kilobit RAM blocks.

Table 3: RAM Interface Signals

Signal Name	Function
Inputs	
WD [17:0]	Write Data
WA [x:0][a]	Write Address
WEN [1:0]	Write Enable (two 9-bit enables)
WD_SEL	Write Chip Select
WCLK	Write Clock
RA [x:0][a]	Read Address
RD_SEL	Read Chip Select
RCLK	Read Clock
Output	
RD [17:0]	Read Data

a. x=8 for 4-kilobit RAM blocks, x=9 for 8-kilobit RAM blocks.

The read and write data buses of a RAM block can be arranged to variable bus widths. The bus widths can be configured using the RAM Wizard available in QuickWorks, QuickLogic's development software. The selection of the RAM depth and width determines how the data is addressed.

The RAM blocks also support data concatenation. Designers can cascade multiple RAM modules to increase the depth or width by connecting corresponding address lines together and dividing the words between modules. Generally, this requires the use of additional programmable logic resources. However, when concatenating only two 4-kilobit RAM blocks or two 8-kilobit RAM blocks, they can be concatenated horizontally or vertically without using any additional programmable fabric resources.

For example, two internal 4-kilobit dual-port RAM blocks concatenated vertically to create a 512x18 RAM block or horizontally to create a 256x36 RAM block. A block diagram of horizontal and vertical concatenation is displayed in **Figure 4**.

Figure 4: Horizontal and Vertical Concatenation Examples

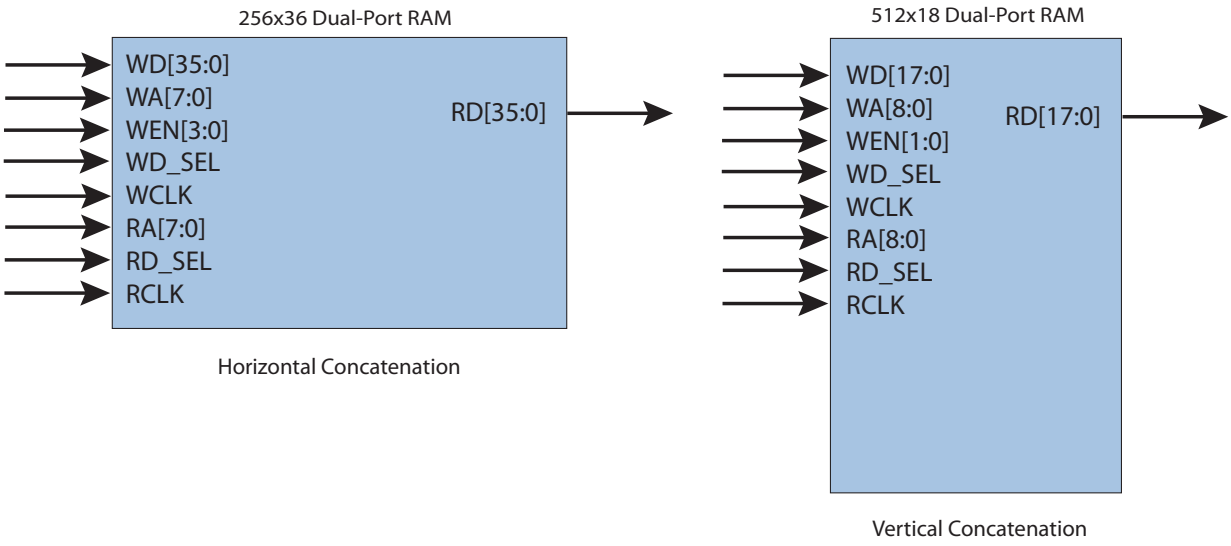


Table 4 shows the various RAM configurations supported by the PolarPro RAM modules.

Table 4: Available Dual-Port RAM Configurations

Device	Number of RAM Blocks	Depth	Width
QL1P075 QL1P100 QL1P200 QL1P300	1	256	1-18
	1	512	1-9
	2	256	1-36
	2	512	1-18
	2	1024	1-9
QL1P600 QL1P1000	1	512	1-18
	1	1024	1-9
	2	512	1-36
	2	1024	1-18
	2	2048	1-9

True Dual-Port RAM

PolarPro dual-port RAM modules can also be concatenated to generate true dual-port RAMs. The true dual-port RAM module's Port1 and Port2 have completely independent read and write ports, and separate read and write clocks. This allows Port1 and Port2 to have different data widths and clock domains. It is important to note that there is no circuitry preventing a write and read operation to the same address space at the same time. Therefore, it is up to the designer to ensure that the same address is not read from and written to simultaneously, otherwise the data is considered invalid. Likewise, the same address must not be written to from both ports at the same time. However, it is possible to read from the same address. **Figure 5** shows an example of a 512x18 true dual-port RAM.

Figure 5: 512x18 True Dual-Port RAM Block

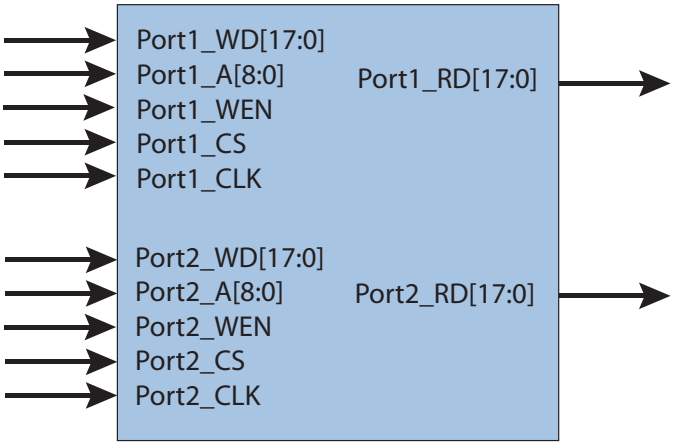


Table 5: True Dual-Port RAM Interface Signals

Port	Signal Name	Function
Port1	**Inputs**	
	Port1_WD[17:0]	Write Data
	Port1_A[8:0]	Write Address
	Port1_WEN[1:0]	Write Enable
	Port1_CS	Chip Select
	Port1_CLK	Clock
	Output	
	Port1_RD[17:0]	Read Data
Port2	**Inputs**	
	Port2_WD[17:0]	Write Data
	Port2_A[8:0]	Write Address
	Port2_WEN[1:0]	Write Enable
	Port2_CS	Chip Select
	Port2_CLK	Clock
	Output	
	Port2_RD[17:0]	Read Data

Table 6: Available True Dual-Port RAM Configurations

Device	Depth	Width
QL1P075 QL1P100 QL1P200 QL1P300	512	1-18
	1024	1-9
QL1P600 QL1P1000	512	1-36
	1024	1-18
	2048	1-9

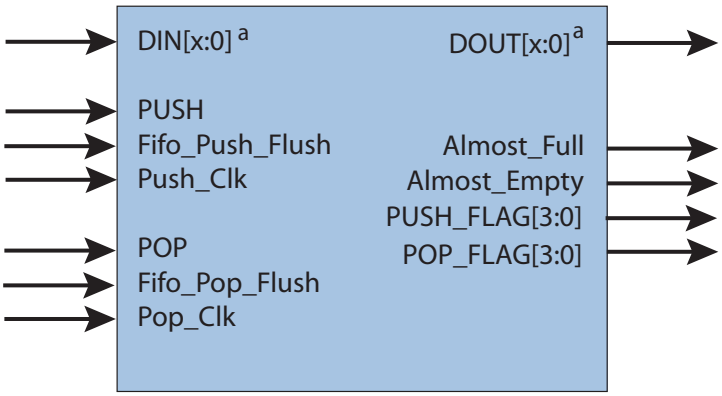
Embedded FIFO Controllers

Every RAM block can be implemented as a synchronous or asynchronous FIFO. There are built-in FIFO controllers that allow for varying depths and widths without requiring programmable fabric resources.

The PolarPro FIFO controller features include:

- x9, x18 and x36 data bus widths
- Independent PUSH and POP clocks
- Independent programmable data width on PUSH and POP sides
- Configurable synchronous or asynchronous FIFO operation
- 4-bit PUSH and POP level indicators to provide FIFO status outputs for each port
- Pipelined read data to improve timing

Figure 6: FIFO Module



a. x = {1,2,3,....35}.

Table 7: Available FIFO Configurations

Device	Number of RAM Blocks	Depth	Supported Widths
QL1P075 QL1P100 QL1P200 QL1P300	1	256	1-18 bits
	1	512	1-9 bits
	2	256	1-36 bits
	2	512	1-18 bits
	2	1024	1-9 bits
QL1P600 QL1P1000	1	512	1-18 bits
	1	1024	1-9 bits
	2	512	1-36 bits
	2	1024	1-18 bits
	2	2048	1-9 bits

Table 8 lists the FIFO controller interface signals.

Table 8: FIFO Interface Signals

Signal Name	Width (bits)	Direction	Function
PUSH Signals			
DIN	1 to 36	I	Data bus input
PUSH	1	I	Initiates a data push
Fifo_Push_Flush	1	I	Empties the FIFO
Push_Clk	1	I	Push data clock
POP Signals			
DOUT	1 to 36	O	Data bus output
POP	1	I	Initiates a data pop
Fifo_Pop_Flush	1	I	Empties the FIFO
Pop_Clk	1	I	Pop data clock
Status Flags			
Almost_Full	1	O	Asserted when FIFO has one location available
Almost_Empty	1	O	Asserted when FIFO has one location used
PUSH_FLAG[3:0]	4	O	FIFO PUSH level indicator
POP_FLAG[3:0]	4	O	FIFO POP level indicator

Table 9 and **Table 10** highlight the corresponding FIFO level indicator for each 4-bit value of the PUSH_FLAG and POP_FLAG outputs.

Table 9: FIFO PUSH Level Indicator Values

Value	Status
0000	Full
0001	Empty
0010	Room for more than one-half
0011	Room for more than one-forth
1000	Room for 8 or more
1001	Room for 7
1010	Room for 6
1011	Room for 5
1100	Room for 4
1101	Room for 3
1110	Room for 2
1111	Room for 1
Others	Reserved

Table 10: FIFO POP Level Interface Signals

Value	Status
0000	Empty
0001	1 entry in FIFO
0010	2 entries in FIFO
0011	3 entries in FIFO
1000	4 entries in FIFO
1010	5 entries in FIFO
1100	6 entries in FIFO
1110	7 entries in FIFO
1000	8 or more entries in FIFO
1101	One-forth or more full
1110	One-half or more full
1111	Full
Others	Reserved

FIFO Flush Procedure

Both PUSH and POP domains are provided with a flush input signal synchronized to their respective clocks. When a flush is triggered from one side of the FIFO, the signal propagates and re-synchronizes internally to the other clock domain. During a flush operation, the values of the FIFO flags are invalid for a specific number of cycles (see **Figure 7** and **Figure 8**).

As shown in **Figure 7**, when the **Fifo_Push_Flush** asserts, the **Almost_Full** and **PUSH_FLAG** signals become invalid until the FIFO can flush the data with regards to the Push clock domain as well as the Pop clock domain. After the **Fifo_Push_Flush** is asserted, the next rising edge of the Pop clock starts the Pop flush routine.

Figure 7 illustrates a FIFO Flush operation. After the **Fifo_Push_Flush** is asserted at 2 (**PUSH_Clk**), four POP clock cycles (12 through 15) are required to update the **POP_FLAG**, and **PUSH_FLAG** signals. The **Almost_Empty** signal is asserted to indicate that the push flush operation has been completed. On the following rising edge of the **PUSH_Clk** (8), the **PUSH_FLAG** is accordingly updated to reflect the successful flush operation.

Figure 7: FIFO Flush from PUSH Side

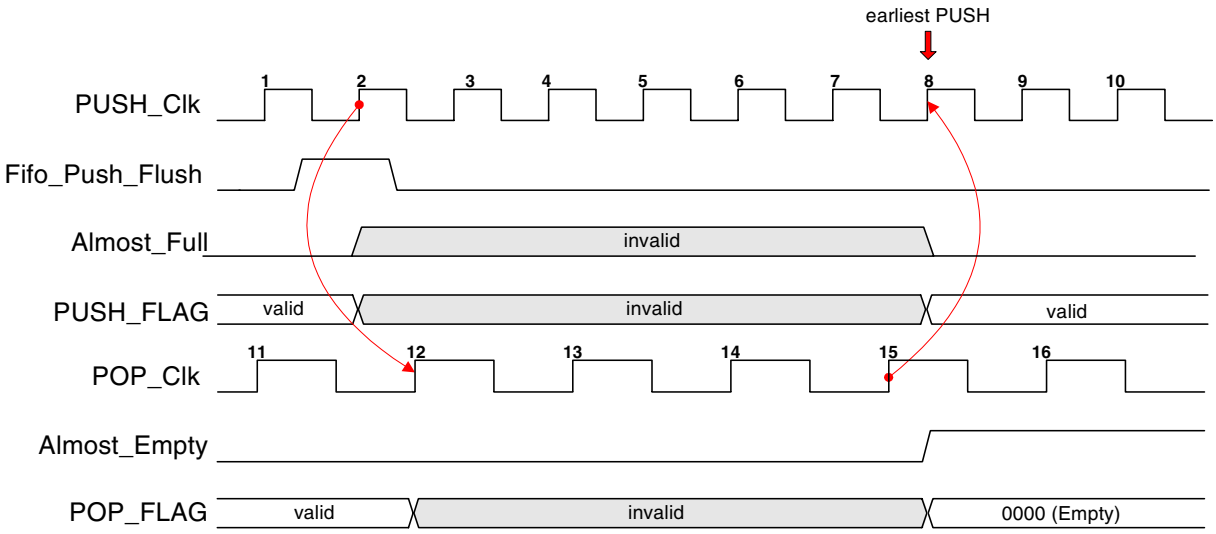


Figure 8 illustrates a POP flush operation. After the **Fifo_Pop_Flush** is asserted at 2 (**POP_Clk**), four PUSH clock cycles (12 through 15) are required to update the **POP_FLAG**, and **PUSH_FLAG** signals. The **Almost_Empty** signal is asserted to indicate that the pop flush operation has been completed. On the following rising edge of the **POP_Clk** (8), the **POP_FLAG** is updated accordingly to reflect the successful flush operation.

Figure 8: FIFO Flush from POP Side

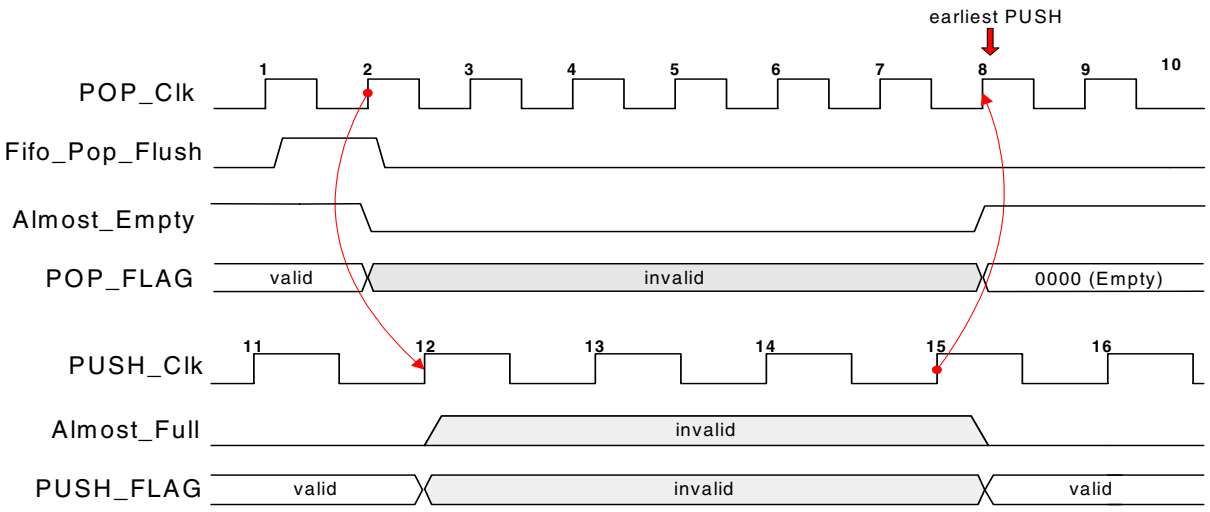


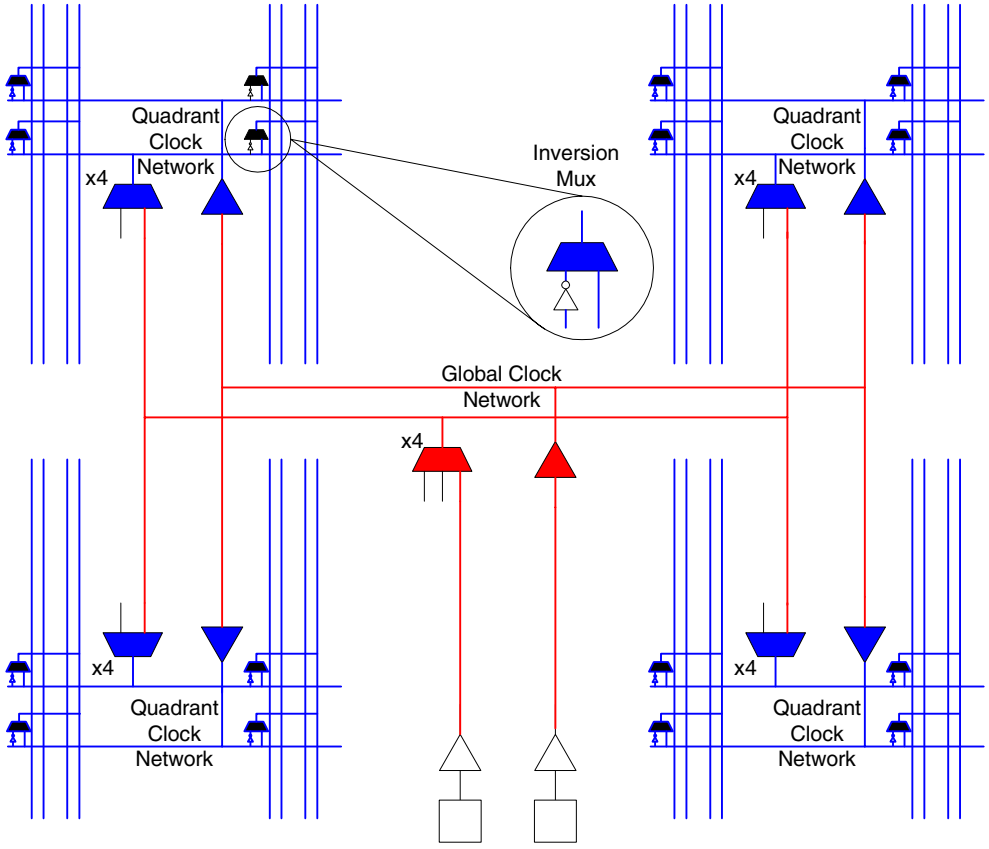
Figure 7 and **Figure 8** are only true for this particular PUSH-POP clock frequency combination. The clock frequency and phase difference between POP_Clk and PUSH_Clk can cause an additional flush delay of one clock cycle in either domain because of the asynchronous relationship between the two clocks.

Distributed Clock Networks

Global Clocks

The PolarPro clock network architecture consists of a 2-level H-tree network as shown in **Figure 9**. The first level of each clock tree (high-lighted in red) spans from the clock input pad to the global clock network and to the center of each quadrant of the chip. The second level (high-lighted in blue) spans from the quadrant clock network to every logic cell inside that quadrant. There are five global clocks in the global clock network, and five quadrant clocks in each quadrant clock network. All global clocks drive the quadrant clock network inputs. The quadrant clocks output to clock inversion muxes, which pass either the original input clock or an inverted version of the input clock to the logic cells in that quadrant. The clock networks can drive RAM block clock inputs and reset, set, enable, and clock inputs to I/O registers. Furthermore, the quadrant clock outputs can be routed to all logic cell inputs.

Figure 9: Global Clock Architecture



Of the five global clock networks, four can be either driven directly by clock pads, Configurable Clock Manager (CCM) outputs, or internally generated signals. These four clock nets go through 3-input global clock muxes located in the middle of the die. See **Figure 10** for a diagram of a 3-input global clock mux. The fifth is a dedicated global clock network that goes directly to the quadrant quad-net clock network and is used as a dedicated fast clock.

Figure 10: Global Clock Structure

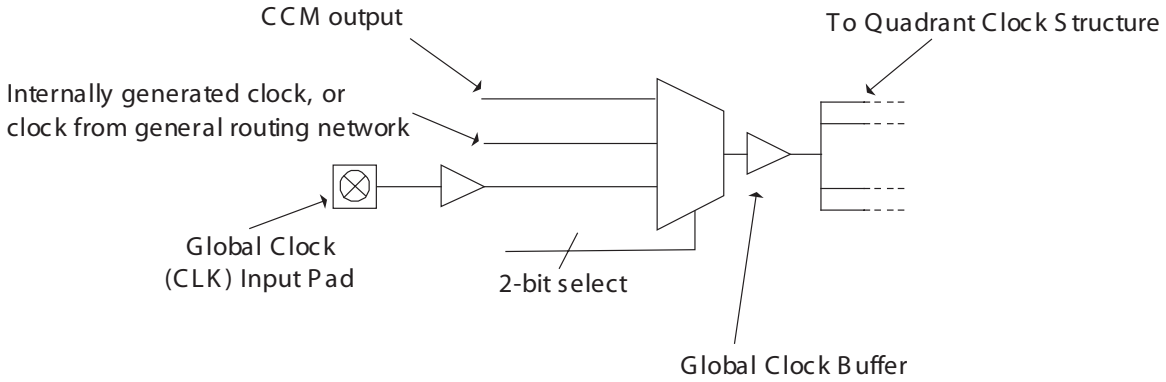
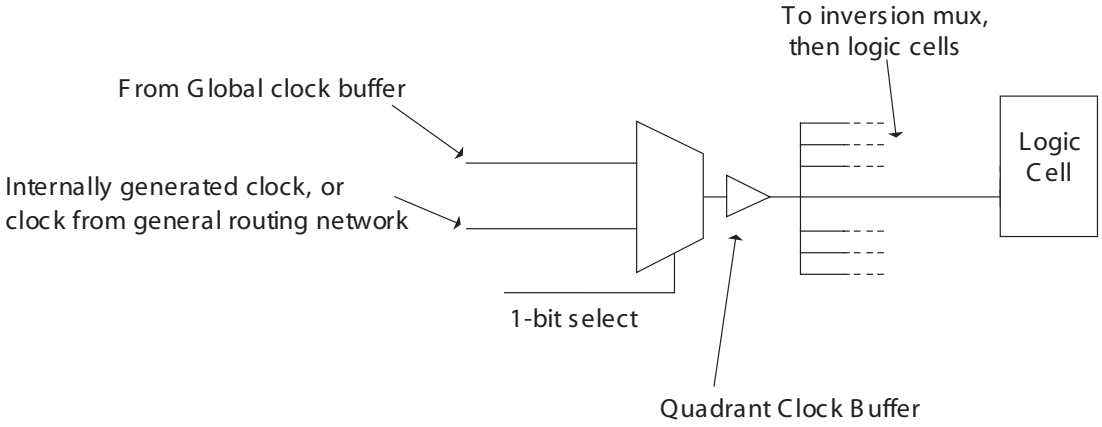


Figure 11 illustrates the quadrant clock 2-input mux.

Figure 11: Quadrant Clock Structure



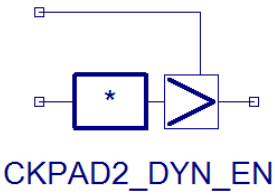
It is important to note that the select lines for the global clock and quad-net muxes are static signals and cannot be changed dynamically during device operation. For more information about global and quad-net clock networks and how to use them, refer to *Application Note 85 Clock Networks in PolarPro Devices* at http://www.quicklogic.com/images/appnote85.pdf.

Dynamic Clock Enable

Devices in the QuickLogic PolarPro family, QL1P200 and larger, provide a powerful dynamic clock enable feature that allows designers to dynamically enable and disable clocks routed into the QuickLogic device. Associated with each of the five clock inputs is a clock enable, which is an interface signal that can be either dynamically controlled via a routable signal or tied high or low. Once an incoming clock is disabled, the clock is driven low internally. All the logic that is driven by the clock is held at the state when the clock was disabled. If a reset signal is passed through the clock pad, the dynamic disable should not be used.

As an additional feature, PolarPro devices have built-in deglitching circuitry to prevent clock glitching during transitions so that clocks can be enabled or disabled asynchronously without the possibility of false edge detection within the internal logic. The dynamic clock disable feature can be implemented in Verilog, VHDL, and schematic designs by instantiating the dynamic clock enable macro, clock2_dyn_en. **Figure 12**, shows the schematic representation of the dynamic clock enable macro.

Figure 12: Clock Pad Macro for Dynamic Clock Enable

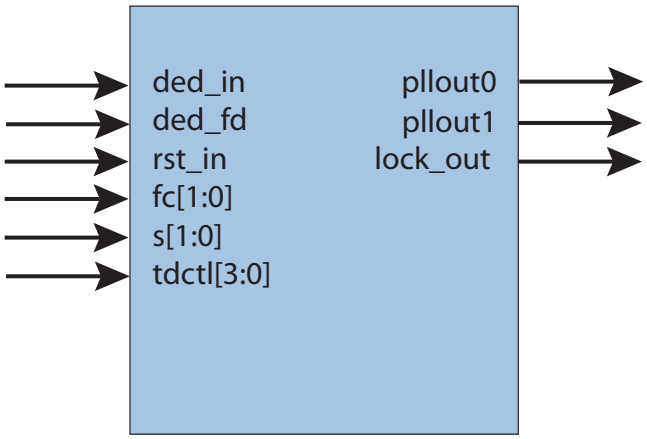


Configurable Clock Managers

The CCM features include:

- Input frequency range from 25 MHz to 200 MHz
- Output frequency range from 25 MHz to 200 MHz
- Output jitter is less than 200 ps peak-to-peak
- Two outputs: pullout0 (with 0° phase shift), and pullout1 (with an option of 0°, 90°, 180°, or 270° phase shift plus a programmable delay).
- Programmable delay allows delays up to 2.5 ns at 250 ps intervals
- Fixed feedback path
- Output frequency lock time in less than 10 µs

Figure 13: Configurable Clock Manager



The reset signal can be routed from a clock pad or generated using internal logic. The lock_out signal can be routed to internal logic and/or an output pad. Both CCM clock outputs can drive the global clock networks, as well as any general purpose I/O pin. Once the CCM has synchronized the output clock to the incoming clock, the lock_out signal will be asserted to indicate that the output clock is valid. Lock detection requires at least 10 µs after reset to assert lock_out. The PolarPro CCMs have three modes of operation, based on the input frequency and desired output frequency. **Table 11** indicates the features of each mode.

Table 11: CCM PLL Mode Frequencies

Output Frequency	Input Frequency Range	Output Frequency Range	PLL Mode
x1	25 MHz to 200 MHz	25 MHz to 200 MHz	PLL_MULT1
x2	25 MHz to 100 MHz	50 MHz to 200 MHz	PLL_MULT2
x4	25 MHz to 50 MHz	100 MHz to 200 MHz	PLL_MULT4

CCM Signals

Table 12 provides the name, direction, function and description of the CCM ports.

Table 12: CCM Signals

Signal Name	Direction	Function	Description
Routable Ports			
ded_in	I	Dedicated Input	Clock pad CCM input source.
ded_fd	I	Dedicated Feedback	Automatically calculated and routed by the software tools.
rst_in	I	Reset	Active high reset: If rst_in is asserted, pllout0 and pllout1 are reset to 0. This signal must be asserted and then released for lock_out to assert.
pllout0	O	0° Phase Clock	0° phase clock output.
pllout1	O	Configurable Phase Clock	0°, 90°,180°, or 270° phase clock output with programmable delay.
lock_out	O	Lock Detect	Active high lock detection signal. Active when the pllout signals correctly output the configured functionality.
Static Ports			
fc[1:0]	I	Phase Shift Control	Determines whether pllout1 is 0°, 90°, 180°, or 270° degrees out of phase with pllout0[a].
s[1:0]	I	Set Mode	Determines pllout1 and pllout0 frequency multiplier (x1, x2, or x4).
tdctl[3:0]	I	Time Delay Control	Pllout1 programmable delay, configurable in 250 ps increments up to a maximum of 2.5 ns. NOTE: 250 ps can vary depending on process variation.

a. The pllout1 output can vary up to -5% with respect to the pllout0 output. Therefore, QuickLogic recommends thorough post-layout simulation in order to verify satisfactory operation of the CCMs.

Table 13, **Table 14**, and **Table 15** give the values used to configure the Set Mode, Phase Shift Control and Time Delay Control bits.

Table 13: Set Mode Values

s[1:0]	Multiplier
00	x1
01	x2
10	x4
11	Reserved

Table 14: Phase Shift Control Values

fc[1:0]	Phase Shift (Deg.)
00	0
01	90
10	180
11	270

Table 15: Time Delay Control Values

tdctl[3:0]	Time Delay (ps)
0000	0
0001	250
0010	500
0011	750
0100	1000
0101	1250
0110	1500
0111	1750
1000	2000
1001	2250
1010	2500
1011	Reserved
1100	Reserved
1101	Reserved
1110	Reserved
1111	Reserved

CCM Configurations

The main purpose of the CCM is to align the clock arrival times of two separate clock destinations, whether it is within the FPGA or external to the chip. The difference between the two clock destinations is referred to as clock skew. To correct for clock skew the CCMs can be configured to shift the phase and/or delay of the pllout1 clock output.

In most cases the desired phase or added delay can be accomplished by configuring both the clock source input and feedback input as dedicated. In the case of a dedicated clock source and dedicated feedback, the QuickLogic development software calculates and generates all of the required routing delays to produce the requested configuration.

Table 16: Available Configurations

Clock	Feedback	Example Usage	Comments
Dedicated clock pad	Dedicated feedback	Standard PLL application. Reduce set-up or clock-to-out time.	If the clock pad and destination are in phase.

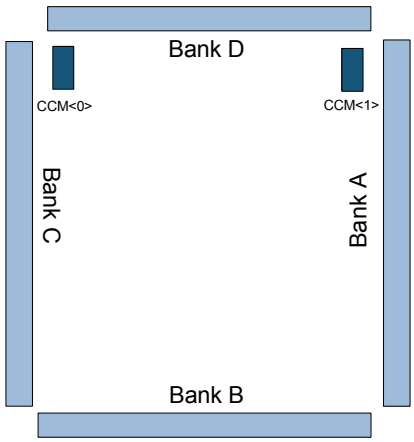
For more information on CCMs and how to use them in QuickWorks, refer to *Application Note 87 Configurable Clock Managers* at http://www.quicklogic.com/images/appnote87.pdf.

Simultaneously Switching Outputs (SSOs) While Using a CCM

SSOs are outputs that transition at the same time in the same direction (either from VCC to GND or GND to VCC). To ensure that the CCMs never lose lock over all possible frequencies of operation, designers must follow the guidelines specified in this section when using the FPGA outputs as SSOs. These guidelines include the number of SSOs placed adjacent to the CCMs and the quality of the power filtering circuit sourcing the CCM block.

Figure 14 shows a basic layout of the four I/O banks (Bank A, Bank B, Bank C and Bank D) available in PolarPro devices and the relative placement of the two CCMs (CCM<0> and CCM<1>).

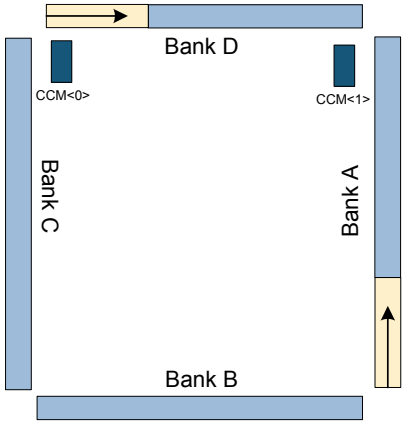
Figure 14: Basic Layout of I/O Banks and CCMs



SSOs placed in Bank C and Bank D in close proximity to CCM<0> may affect that CCM's functionality. Similarly, SSOs placed in Bank A and Bank D in close proximity to CCM<1> may affect that CCM's functionality.

NOTE: To define the boundary of operation when using SSOs in conjunction with CCMs, add SSOs starting from the far end of a bank relative to the CCMs location. For example, when using CCM<1>, add SSOs in Bank A starting from the far bottom right and in Bank D starting from the far top left (see **Figure 15**). The same applies for CCM<0> in reverse positioning.

Figure 15: Adding SSOs When Using CCM<1>



To ensure proper operation of the CCM(s) use the following guidelines:

1. Limit the number of SSOs in Bank A and Bank D that are synchronous to CCM<1> (i.e., clocked by CCM<1> outputs) and SSOs in Bank C and Bank D that are synchronous to CCM<0> (i.e., clocked by CCM<0> outputs) as shown in **Table 17**, **Table 18**, and **Table 19**.

NOTE: For example, refer to row 7 highlighted in **Table 17**. If 56 SSOs are placed with a slew rate setting of Wow, up to 24 SSOs can be placed in Bank A (CCM<1>) or Bank C (CCM<0>) and up to 48 SSOs can be placed in Bank D. Similarly, with a slew rate setting of Slow, up to 36 SSOs can be placed in Bank A (CCM<1>) or Bank C (CCM<0>) and up to 48 SSOs can be placed in Bank D. However, if 60 SSOs are placed on Bank A (CCM<1>) or Bank B (CCM<0>), a slew rate setting of Wow cannot be used, but slew rate settings such as Very Fast, Fast and Slow can be used.

Table 17: Usable Synchronous SSOs at VCCIO = 3.3 V

Total SSO in (Bank A and Bank D) or (Bank C and Bank D)	Slew Rate Setting							
	Wow		Very Fast		Fast		Slow	
	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D
QL1P075 and QL1P100								
8	8	8	8	8	8	8	8	8
16	16	16	16	16	16	16	16	16
24	24	24	24	24	24	24	24	24
32	24	32	32	32	32	32	32	32
40	24	40	36	40	36	40	36	40
48	24	48	36	48	36	48	36	48
56	24	48	36	48	36	48	36	48
60			36	40	36	48	36	48
64			36	40	36	48	36	48
72					36	48	36	48
76					36	40	36	48
84							36	48
QL1P200 and QL1P300								
8	8	8	8	8	8	8	8	8
16			16	16	16	16	16	16
24			24	24	24	24	24	16
32			24	32	32	32	32	16
40			24	40	36	32	36	16
48			24	40	36	32	36	16
56								
60								
64								
72								
76								
84								

Table 18: Usable Synchronous SSOs at VCCIO = 2.5 V

Total SSO in (Bank A and Bank D) or (Bank C and Bank D)	Slew Rate Setting							
	Wow		Very Fast		Fast		Slow	
	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D
QL1P075 and QL1P100								
8	8	8	8	8	8	8	8	8
16	16	16	16	16	16	16	16	16
24	24	24	24	24	24	24	24	24
32	32	32	32	32	32	32	32	32
40	36	40	36	40	36	40	36	40
48	36	48	36	48	36	48	36	48
56	36	48	36	48	36	48	36	48
60	36	48	36	48	36	48	36	48
64	36	48	36	48	36	48	36	48
72	36	48	36	48	36	48	36	48
76			36	48	36	48	36	48
84			36	48	36	48	36	48
QL1P200 and QL1P300								
8	8	8	8	8	8	8	8	8
16	16	16	16	16	16	16	16	16
24	0	24	24	24	24	24	24	24
32			32	24	32	24	32	32
40			36	24	36	24	36	40
48			36	24	36	24	36	48
56			36	24	36	24	36	48
60			36	24	36	24	36	48
64							36	48
72							36	48
76							36	40
84								

Table 19: Usable Synchronous SSOs at VCCIO = 1.8 V

Total SSO in (Bank A and Bank D) or (Bank C and Bank D)	Slew Rate Setting							
	Wow		Very Fast		Fast		Slow	
	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D
QL1P075 and QL1P100								
8	8	8	8	8	n/a	n/a	n/a	n/a
16	16	16	16	16	n/a	n/a	n/a	n/a
24	24	24	24	24	n/a	n/a	n/a	n/a
32	32	32	32	32	n/a	n/a	n/a	n/a
40	36	40	36	40	n/a	n/a	n/a	n/a
48	36	48	36	48	n/a	n/a	n/a	n/a
56	36	48	36	48	n/a	n/a	n/a	n/a
60	36	48	36	48	n/a	n/a	n/a	n/a
64	36	48	36	48	n/a	n/a	n/a	n/a
72	36	48	36	48	n/a	n/a	n/a	n/a
76	36	48	36	48	n/a	n/a	n/a	n/a
84	36	48	36	48	n/a	n/a	n/a	n/a
QL1P200 and QL1P300								
8	8	8	8	8	n/a	n/a	n/a	n/a
16	16	16	16	16	n/a	n/a	n/a	n/a
24	24	24	24	24	n/a	n/a	n/a	n/a
32	32	32	32	32	n/a	n/a	n/a	n/a
40	36	40	36	32	n/a	n/a	n/a	n/a
48	36	48	36	32	n/a	n/a	n/a	n/a
56	36	48	36	32	n/a	n/a	n/a	n/a
60	36	48	36	32	n/a	n/a	n/a	n/a
64	24	48	32	32	n/a	n/a	n/a	n/a
72					n/a	n/a	n/a	n/a
76					n/a	n/a	n/a	n/a
84					n/a	n/a	n/a	n/a

2. Limit the number of SSOs in Bank A and Bank D that are asynchronous to CCM<1> (i.e., not clocked by CCM<1> outputs) and SSOs in Bank C and Bank D that are asynchronous to CCM<0> (i.e., not clocked by CCM<0> outputs) as shown in **Table 20**, **Table 21**, and **Table 22**.

Table 20: Usable Asynchronous SSOs at VCCIO = 3.3V

Total SSO in (Bank A and Bank D) or (Bank C and Bank D)	Slew Rate Setting							
	Wow		Very Fast		Fast		Slow	
	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D
QL1P075 and QL1P100								
8	8	8	8	8	8	8	8	8
16					16	16	16	16
24					24	24	24	24
32					32	24	32	24
40					36	24	36	24
48					36	24	36	24
56							36	24
60							36	24
QL1P200 and QL1P300								
8	8	0	8	8	8	8	8	8
16			16	16	16	16	16	8
24			16	8	24	24	24	8
32					32	24	32	8
40					36	24	36	8
48								
56								
60								

Table 21: Usable Asynchronous SSOs at VCCIO = 2.5 V

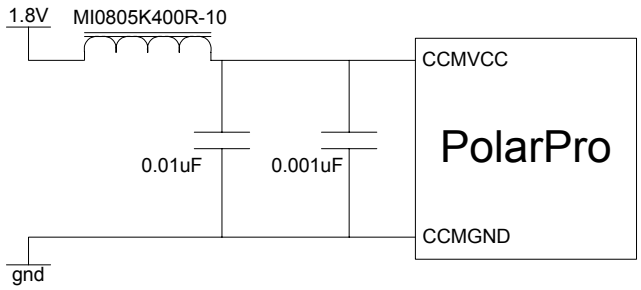
Total SSO in (Bank A and Bank D) or (Bank C and Bank D)	Slew Rate Setting							
	Wow		Very Fast		Fast		Slow	
	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D
QL1P075 and QL1P100								
8	8	8	8	8	8	8	8	8
16	16	16	16	16	16	16	16	16
24	16	24	24	24	24	24	24	24
32			32	32	32	32	32	32
40			36	32	36	32	36	40
44			36	32	36	32	36	40
48			36	32	36	32	36	40
56			32	32	36	32	36	40
60					36	24	36	40
64							36	40
68							36	32
QL1P200 and QL1P300								
8	8	8	8	8	8	8	8	8
16			16	16	16	16	16	16
24			24	24	24	24	24	16
32			32	24	32	32	32	16
40			36	24	36	32	36	16
44			36	24	36	32	36	16
48			32	24	36	32	36	16
56								
60								
64								
68								

Table 22: Usable Asynchronous SSOs at VCCIO = 1.8 V

Total SSO in (Bank A and Bank D) or (Bank C and Bank D)	Slew Rate Setting							
	Wow		Very Fast		Fast		Slow	
	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D	Max. SSO in Bank A/ Bank C	Max. SSO in Bank D
QL1P075 and QL1P100								
8	8	8	8	8	n/a	n/a	n/a	n/a
16	16	16	16	16	n/a	n/a	n/a	n/a
24	24	24	24	24	n/a	n/a	n/a	n/a
32	32	32	32	32	n/a	n/a	n/a	n/a
40	32	40	36	40	n/a	n/a	n/a	n/a
44	16	40	36	40	n/a	n/a	n/a	n/a
48	16	40	36	40	n/a	n/a	n/a	n/a
56	16	40	36	40	n/a	n/a	n/a	n/a
60			36	40	n/a	n/a	n/a	n/a
64			24	40	n/a	n/a	n/a	n/a
68					n/a	n/a	n/a	n/a
QL1P200 and QL1P300								
8	8	8	8	8	n/a	n/a	n/a	n/a
16	16	8	16	16	n/a	n/a	n/a	n/a
24	16	8	24	24	n/a	n/a	n/a	n/a
32			32	24	n/a	n/a	n/a	n/a
40			36	24	n/a	n/a	n/a	n/a
44			36	24	n/a	n/a	n/a	n/a
48			36	24	n/a	n/a	n/a	n/a
56			36	24	n/a	n/a	n/a	n/a
60			36	24	n/a	n/a	n/a	n/a
64					n/a	n/a	n/a	n/a
68					n/a	n/a	n/a	n/a

3. The power supply to the CCMs must have adequate noise filtering circuits. QuickLogic Reference Design boards use the noise filtering circuit shown in **Figure 16**.

Figure 16: Noise Filtering Circuit

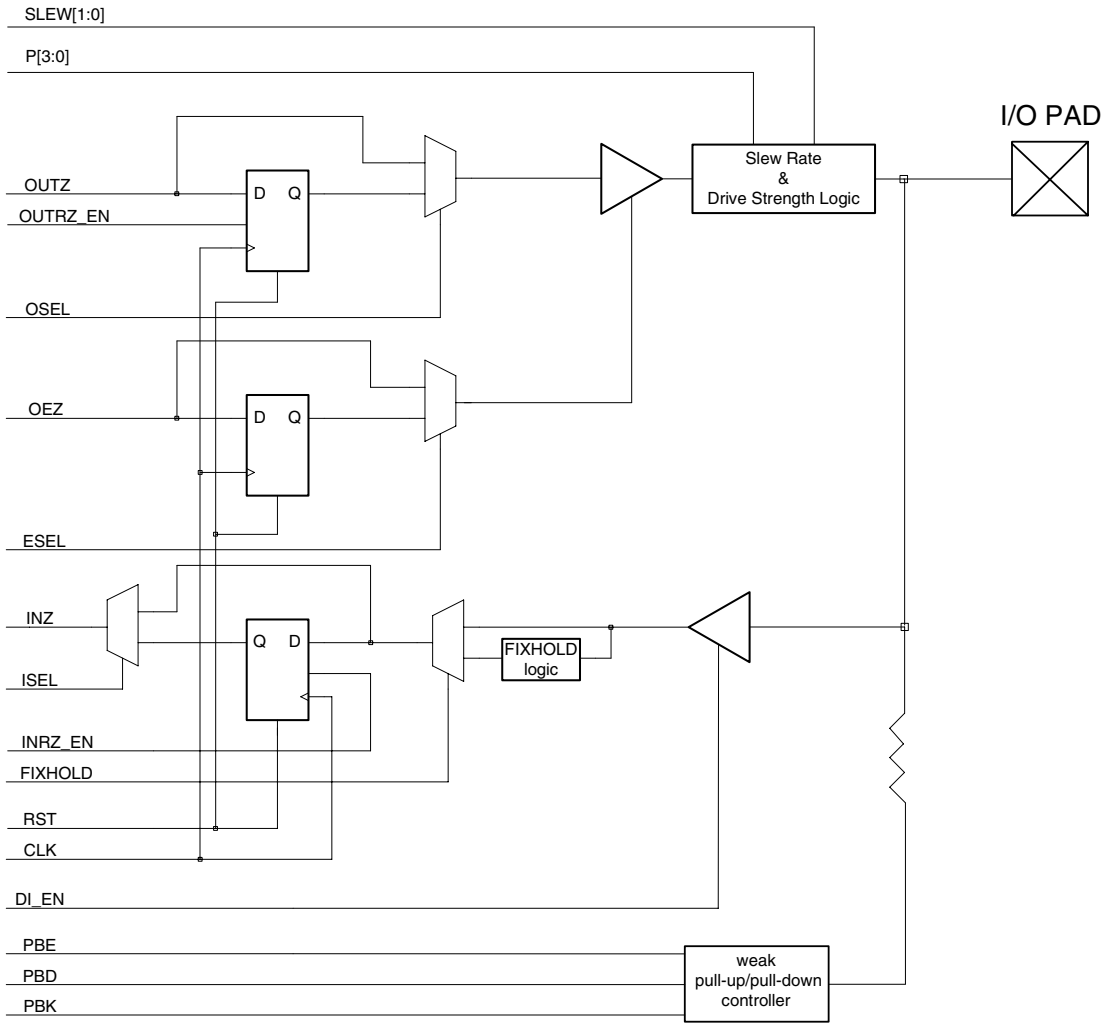


General Purpose Input Output (GPIO) Cell Structure

The GPIO features include:

- Direct or registered input with input path select
- Direct or registered output with output path select
- Direct or registered output enable with OE path select
- Input buffer enable to reduce power
- Programmable weak keeper, programmable pull-up/pull-down control
- Programmable drive strength
- Configurable slew rate
- Support for JTAG boundary scan

Figure 17: PolarPro GPIO Cell



With bi-directional I/O pins and global clock input pins, the PolarPro device maximizes I/O performance, functionality, and flexibility. All input and I/O pins are 1.8 V, 2.5 V, and 3.3 V tolerant and comply with the specific I/O standard selected. For single-ended I/O standards, the corresponding VCCIO bank input specifies the input tolerance and the output drive voltage. Drive strength and slew rate are configured for an entire bank. Weak keeper, pull-up, and pull-down functions can be configured for individual I/O. The default configuration for QuickLogic QuickWorks software has the drive strength set to 4 and the slew rate set to wow.

Table 23: GPIO Interface Signals

Signal Name	Direction	Function
Routable Signals		
OUTZ	I	Data out from internal logic
OUTRZ_EN	I	Enable for registered OUTZ
OEZ	I	Tristate enable for the output signal
INZ	O	Input signal to the internal logic
INRZ_EN	I	Enable for registered INZ
RST	I	Reset for optional registers
CLK	I	Clock signal for optional registers
DI_EN	I	Enable for I/O input signal. Drives a 1 to internal logic when disabled.
Static Signals		
SLEW[1:0]	I	2-bit slew rate control
P[3:0]	I	Programmable drive strength
OSEL	I	Select signal for registered or flow through OUTZ
ESEL	I	Select signal for registered or flow-through OEZ
ISEL	I	Select signal for registered or flow-through INZ
FIXHOLD	I	Enable control for I/O input delay for hold fixing
PBE	I	Input signals for the weak keeper, pull-up/pull-down controller, see **Table 24** for functional behavior
PBD	I	
PBK	I	

Programmable Weak Keeper, Pull-Up, and Pull-Down

A programmable Weak Keeper, Pull-Up or Pull-Down controller is also available on each General Purpose I/O bank. When implementing the Weak Keeper, Pull-Up, and Pull-Down functions, each I/O can be configured separately. The I/O Weak Pull-Up and Pull-Down eliminates the need for external resistors. When PBK=1 the keeper block is placed into keeper mode. In the keeper mode, the pad pin (if the driver is tristated), will be kept at whichever level it was last forced, either by the driver itself, or by an external driver.

Table 24: Weak Pull-Up, and Pull-Down Controller

PBK	PBD	PBE	Function
0	0	0	Tristate (floating)
0	0	1	Weak Pull-Down
0	1	1	Weak Pull-Up
1	X	X	Weak Keeper (retains state)
0	1	0	Reserved

Programmable Drive Strength

Every GPIO has independent drive strength control. Twelve different drive strength levels are available for designers to choose from. For additional information about corresponding drive strength see **DC Characteristics** on page 35.

Programmable Slew Rate

Each I/O has programmable slew rate capability. The PolarPro GPIOs allow up to four different slew rate speeds (slow, fast, vfast, and wow). Slower slew rates can be used to reduce noise caused by I/O switching.

I/O interface standards are programmable on a per bank basis. **Table 25** illustrates the I/O bank configurations available. Each I/O bank is independent of other I/O banks and each I/O bank has its own VCCIO supply inputs. A mixture of different I/O standards can be used on a PolarPro device. However, there is a limitation as to which I/O standards can be supported within a given bank. Only standards that share a common VCCIO can be shared within the same bank (e.g., PCI and LVTTL).

Table 25: I/O Standards and Applications

I/O Standard	VCCIO Voltage	Application
LVTTL	3.3 V	General Purpose
LVCMOS25	2.5 V	General Purpose
LVCMOS18	1.8 V	General Purpose
PCI	3.3 V	PCI Bus Applications

DDRIO Cell Structure

QuickLogic PolarPro devices support DDRIOs, which allows clocking data on both the positive and negative clock edges. All PolarPro devices have one I/O bank (Bank D) that can be configured in either a GPIO bank or a DDRIO mode. When bank D is configured to DDRIO mode, it is further divided into DDRIO sets. Each set contains 12 I/Os, which include 8 DQs, 1 DQM, 1 DQS, 1 DQCK_N and 1 DQCK_P (for the differential clocks, refer to **Table 26**).

Figure 18: PolarPro DDRIO Block Diagram

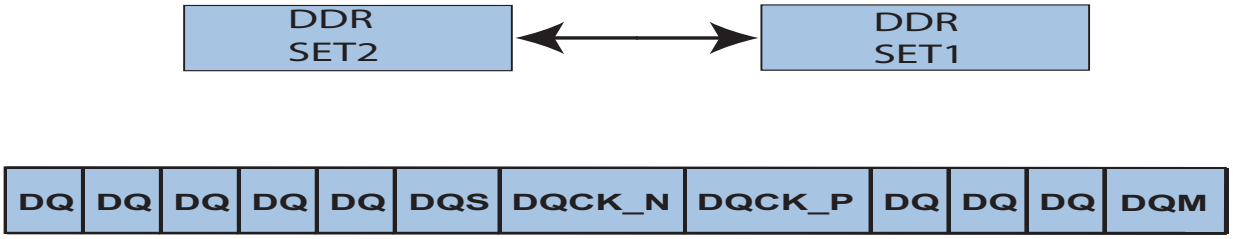


Table 26: Available DDR Sets

PolarPro Device	Package	Number of DDR Sets
QL1P075	PF144	2
	PT196	4
	PS256	4
QL1P100	PF144	2
	PT196	4
	PS256	4
QL1P200	PS256	4
	PS324	4
QL1P300	PS256	4
	PS324	4
QL1P600	PS256	4
	PS324	4
QL1P1000	PS256	4
	PS324	4

Double Data Rate (DDR) I/O

The DDR features include:

- Programmable slew rate
- Programmable drive strength
- Programmable pull-up

Figure 19: DDRIO DQ Configuration

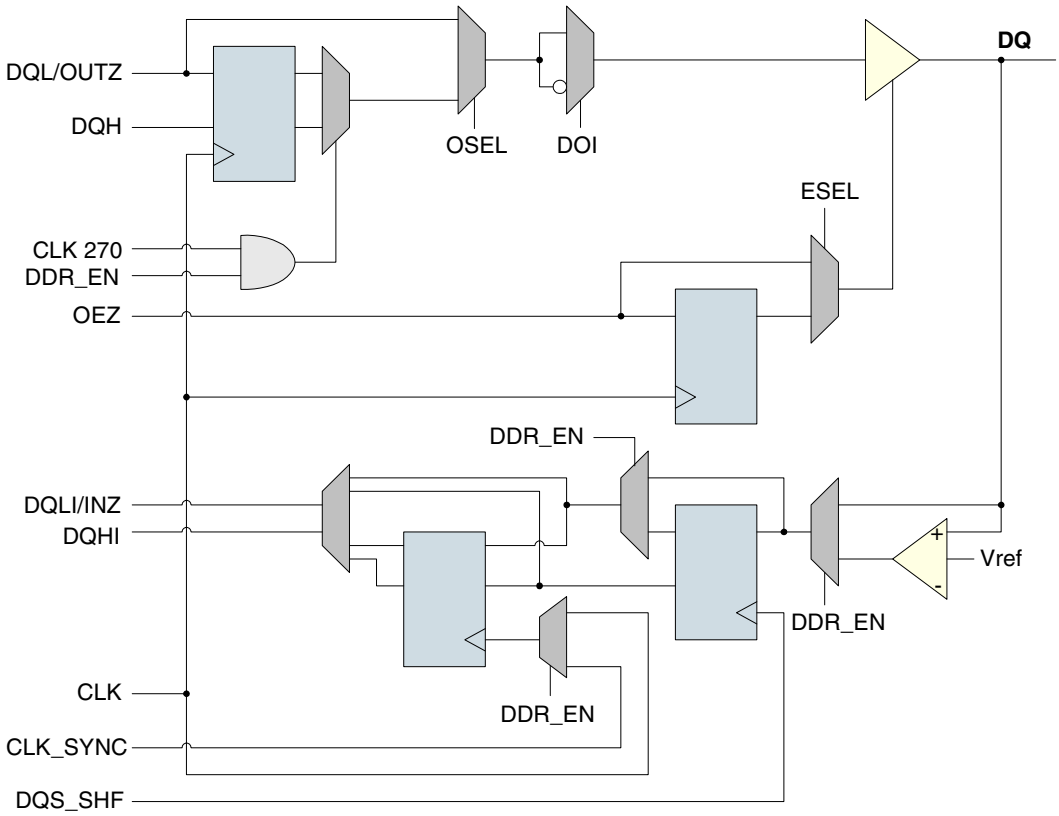


Figure 20: DDRIO DQS Configuration

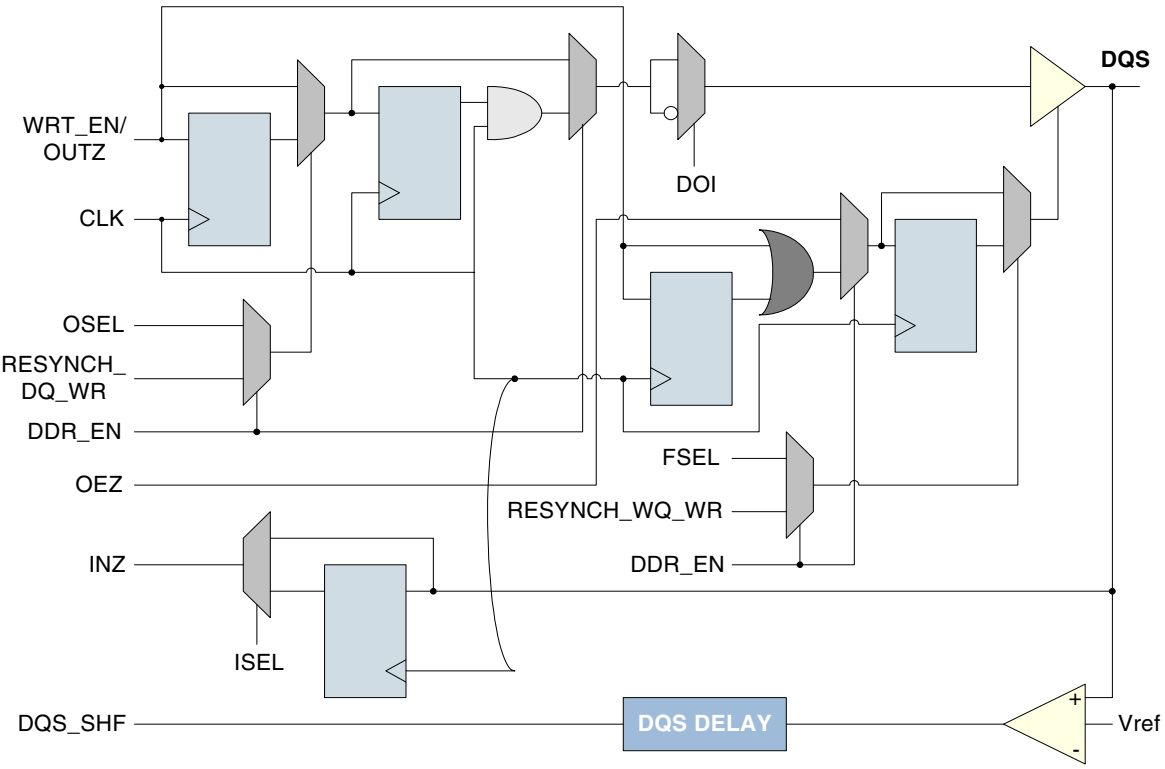


Table 27: DDR DQ Fabric Interface Signals

Signal Name	Direction	Function
Routable Signals		
DDR_EN	I	Enable DDR function, otherwise function will be that of GPIO.
CLK270	I	Shifted clock used in center-aligning data with DQS in writing out data.
PDB	I	Used as control for differential power-down.
CLK	I	System clock signal from the programmable fabric.
RST	I	Reset signal for registers inside the I/O.
INRZ_EN	I	Enable for registered DQLI / INZ.
DQH	I	Higher bit DQ signal output from core.
OUTRZ_EN	I	GPIO: enable for registered OUTZ signal.
DQL / OUTZ	I	DDR(DQL): lower bit DQ signal output from core. GPIO(OUTZ): data out from core with optional register.
OEZ	I	Tristate enable for the output signal with optional register.
DQHI	O	Higher bit DQ signal input to core with optional register for resynchronization.
DQLI / INZ	O	DDR(DQLI): lower bit DQ signal input to core with optional register for resynchronization. GPIO(INZ): data in signal to core with optional register.

Table 27: DDR DQ Fabric Interface Signals *(Continued)*

Signal Name	Direction	Function
Static Signals		
resync_DQ_rd	I	Signal to enable resynching of DQ being read to avoid setup violations inside the programmable fabric.
resync_DQ_wr	I	Signal to enable resynching of DQ being written to avoid setup violations inside the I/O.
SLEW[1:0]	I	2-bit slew rate control.
P[3:0]	I	Pull-up programmable drive strength.
N[3:0]	I	Pull-down programmable drive strength.
FIXHOLD	I	Enable control for I/O input delay for hold fixing.
PBE	I	Input signal for weak pull-up controller.
DOI	I	Used as control for data out inversion.
ISEL	I	Select signal for registered or flow through INZ.
OSEL	I	Select signal for registered or flow through OUTZ.
ESEL	I	Select signal for registered or flow through OEZ.

Table 28: DDR DQS Interface Signals

Signal Name	Direction	Function
Routable Signals		
CLK_SYNC	I	Optional resynchronization clock to sync incoming data with the programmable fabric system clock.
PDB	I	Control for differential power-down.
CLK	I	System clock signal from the programmable fabric.
RST	I	Reset signal for registers inside the I/O.
INRZ_EN	I	GPIO: enable for registered INZ.
INZ	O	GPIO: data in signal to core with optional register.
DQS_BR_REL	I	A read burst signal used to mask the end of DQS pulses to avoid unnecessary glitches that will result in clocking-in unwanted data.
OEZ	I	Tristate enable for the output signal with optional register.
OUTRZ_EN	I	Enable for registered or flow-through WRT_EN/OUTZ.
WRT_EN	I	DDR(WRT_EN): write enable signal. GPIO(OUTZ): data out from core with optional register.
Static Signals		
CLK_SYNC_DEL_CTRL[4:0]	I	Setting to program delay for CLK_SYNC.
CLK_SYNC_INV	I	Option to invert CLK_SYNC.
resync_DQ_wr	I	Signal to enable resynching of DQ being written to avoid setup violations inside I/O.
DDR_EN	I	Enable DDR function, otherwise function will be that of GPIO.
FIXHOLD	I	Enable control for I/O input delay for hold fixing.

Table 28: DDR DQS Interface Signals *(Continued)*

Signal Name	Direction	Function
PBE	I	Input signal for weak pull-up controller.
SLEW[1:0]	I	Slew rate control setting.
P[3:0]	I	Pull-up programmable drive strength.
N[3:0]	I	Pull-down programmable drive strength.
DOI	I	Control for data out inversion.
ISEL	I	DDR: selects between VREF (ISEL=0) or PADI (ISEL=1), to connect to the inverting-input of a differential amplifier inside the DDR I/O driver. GPIO: Select signal for registered or flow-through INZ.
OSEL	I	Select signal for registered or flow-through WRT_EN/OUTZ.
ESEL	I	Select signal for registered or flow-through DQS_OE/OEZ.
DQS_DEL_ CTRL[3:0]	I	Setting to program delay of DQS signal.

DDRIO in GPIO Mode

DDR in GPIO mode features include programmable I/O standards via the VCCIO input pins (1.8V LVCMOS, 2.5V LVCMOS, and 3.3V LVTTL).

NOTE: DDRIOs do not support PCI. For PCI support use the general purpose I/Os.

Very Low Power (VLP) Mode

The QuickLogic PolarPro devices have a unique feature, referred to as VLP mode, which reduces power consumption by placing the device in standby. Specifically, VLP mode can bring the total standby current down to less than 10 µA at room temperature when no incoming signals are toggled. VLP mode is controlled by the VLP pin. The VLP pin is active low, so VLP mode is activated by pulling the VLP pin to ground. Conversely, the VLP pin must be pulled to 3.3 V for normal operation.

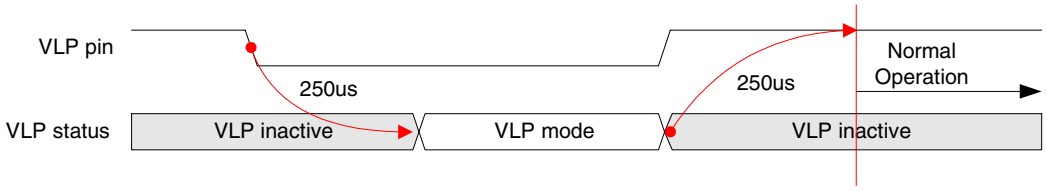
When a PolarPro device goes into VLP mode, the following occurs:

- All logic cell registers and GPIO registers values are held
- All RAM cell data is retained
- The outputs from all GPIO to the internal logic are tied to a weak '1'
- GPIO outputs drive the previous values
- GPIO output enables retain the previous values
- DDRIO outputs are pulled down through a weak pull down circuit
- Clock pad inputs are gated
- CCMs are held in the reset state

The entire operation from normal mode to VLP mode requires 250 µs (300 µs maximum). As mentioned in the VLP behavioral description above, the output of the GPIO to the internal logic is a weak '1'. Therefore, to preserve data retention GPIO should not be used for a set, reset, or clock signal.

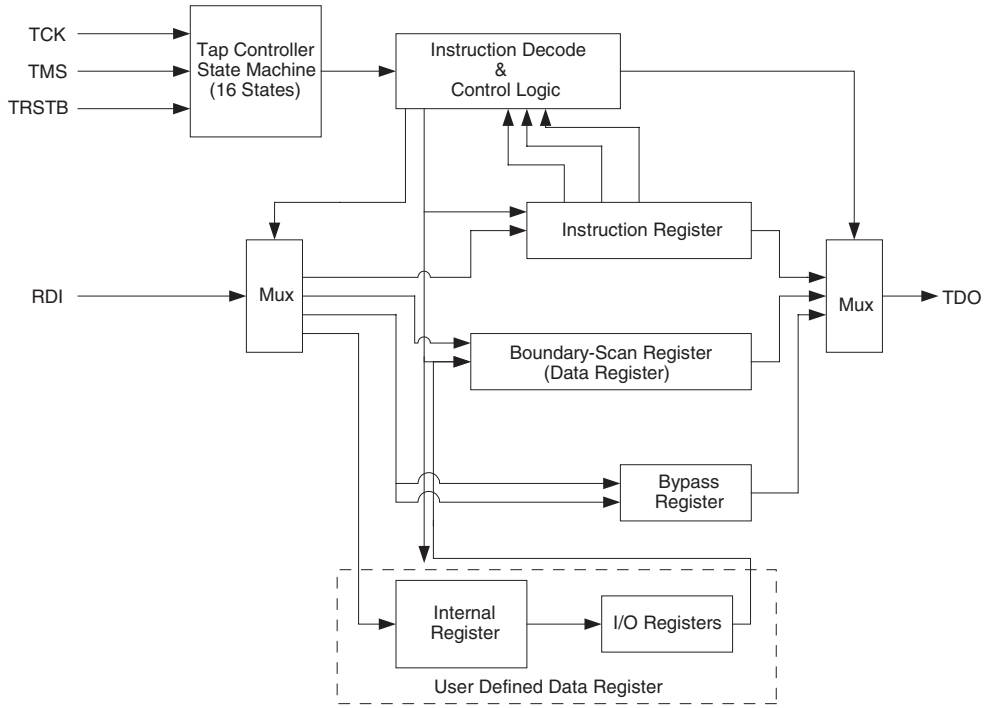
As the device exits out of VLP mode, the data from the registers, RAM, and GPIO will be used to recover the functionality of the device. Furthermore, since the CCMs were in a reset state during VLP mode, they will have to re-acquire the correct output signals before asserting lock_out. The time required to go from VLP mode to normal operation is 250 µs (300 µs maximum). **Figure 23** displays the delays associated with entering and exiting VLP mode.

Figure 21: Typical VLP Mode Timing



Joint Test Access Group (JTAG) Information

Figure 22: JTAG Block Diagram



QuickLogic's PolarPro family complies with IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture. The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR), which allow users to run three required tests along with several user-defined tests. JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for comprehensive verification of higher level system elements.

The 1149.1 standard requires the following three tests:

- **Extest Instruction.** The Extest Instruction performs a printed circuit board (PCB) interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (through the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** The Sample/Preload Instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed through a data scan operation, allowing users to sample the functional data entering and leaving the device.
- **Bypass Instruction.** The Bypass Instruction allows data to skip a device boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

JTAG BSDL Support

- Boundary Scan Description Language (BSDL)
- Machine-readable data for test equipment to generate testing vectors and software
- BSDL files available for all device/package combinations from QuickLogic
- Extensive industry support available and ATVG (Automatic Test Vector Generation)

Electrical Specifications

DC Characteristics

The DC Specifications are provided in **Table 29** through **Table 32**.

Table 29: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
VCC Voltage	-0.5 V to 2.2 V	Latch-up Immunity	±100 mA
VCCIO Voltage	-0.5 V to 4.0 V	ESD Pad Protection	2 kV
VREF Voltage	-0.5 V to 2.0 V	Leaded Package Storage Temperature	-65° C to + 150° C
Input Voltage	-0.5 V to 4.0 V	Laminate Package (BGA) Storage Temperature	-55° C to + 125° C

Table 30: Recommended Operating Range

Symbol	Parameter	Military		Industrial		Commercial		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
VCC	Supply Voltage	1.71	1.89	1.71	1.89	1.71	1.89	V
VCCIO	I/O Input Tolerance Voltage	1.71	3.60	1.71	3.60	1.71	3.60	V
TJ	Junction Temperature	-55	125	-40	100	0	85	°C

Table 31: DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_I	I or I/O Input Leakage Current	VI = VCCIO or GND	-	-	1	µA
I_{OZ}	3-State Output Leakage Current	VI = VCCIO or GND	-	-	1	µA
C_I	I/O Input Capacitance	VCCIO = 3.6 V	-	-	10	pF
C_{CLOCK}	Clock Input Capacitance	VCCIO = 3.6 V	-	-	10	pF
I_{REF}	Quiescent Current on INREF	-	-	-	5	µA
I_{PD}	Current on programmable pull-down	VCCIO = 3.6 V	-200	-	-50	µA
		VCCIO = 2.75 V	-150	-	-25	µA
		VCCIO = 1.89 V	-100	-	-10	µA
I_{PU}	Current on programmable pull-up	VCCIO = 3.6 V	50	-	200	µA
		VCCIO = 2.75 V	25	-	150	µA
		VCCIO = 1.89 V	10	-	100	µA
I_{VLP}	Quiescent Current on VLP pin	VLP=3.3	-	1	10	µA
I_{CCM}	Quiescent Current on each CCMVCC	VCC=1.89 V	-	1	10	µA
I_{VCC}	Quiescent Current	VLP=GND		2.2	40	µA
		VLP=3.3V	-	40	100	µA
I_{VCCIO}	Quiescent Current on VCCIO	VCCIO = 3.6 V	-	2	10	µA
		VCCIO = 2.75 V	-	2	10	µA
		VCCIO = 1.89 V	-	2	10	µA

Table 32: DC Input and Output Levels[a]

Symbol	INREF		V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MIN}	V_{MAX}	V_{MAX}	V_{MIN}	mA	mA
LVTTL	n/a	n/a	-0.3	0.8	2.2	VCCIO + 0.3	0.4	2.4	2.0	-2.0
LVCMOS2	n/a	n/a	-0.3	0.7	1.7	VCCIO + 0.3	0.7	1.7	2.0	-2.0
LVCMOS18	n/a	n/a	-0.3	0.63	1.2	VCCIO + 0.3	0.7	1.7	2.0	-2.0
GTL+	0.88	1.12	-0.3	INREF - 0.2	INREF + 0.2	VCCIO + 0.3	0.6	n/a	40	n/a
PCI	n/a	n/a	-0.3	0.3 x VCCIO	0.6 x V_{CCIO}	VCCIO + 0.5	0.1 x VCCIO	0.9 x VCCIO	1.5	-0.5
SSTL2	1.15	1.35	-0.3	INREF - 0.18	INREF + 0.18	VCCIO + 0.3	0.74	1.76	7.6	-7.6
SSTL3	1.3	1.7	-0.3	INREF - 0.2	INREF + 0.2	VCCIO + 0.3	1.10	1.90	8	-8

a. The data provided in **Table 32** represents the JEDEC and PCI specification. QuickLogic devices either meet or exceed these requirements.

Table 33 and **Table 34** lists the worst case process (T_J=125°C) output currents (in mA) across the output driver at three levels of I/O voltages. All drive strength data was measured at I/O voltages of 0.4 V and VCCIO - 0.4 V.

Table 33: GPIO Programmable Drive Strength

Drive Strength	IOH (mA)			IOL (mA)		
	1.8V	2.5V	3.3V	1.8V	2.5V	3.3V
1	2.2	2.8	3.2	1.7	2.3	2.7
2	4.1	5.2	5.9	3.4	4.4	5
3	6.2	7.8	8.8	5.1	6.7	7.6
4	8	10	11.2	6.6	8.6	9.7
5	10	12.4	13.9	8.3	10.7	12.1
6	11.8	14.6	16.3	9.8	12.7	14.2
7	13.7	16.9	18.9	11.5	14.7	16.6
8	15.3	18.9	21	12.9	16.5	18.5
9	17.1	21.1	23.4	14.5	18.5	20.7
10	18.8	23	25.5	15.9	20.2	22.6
11	20	25	27.6	17.4	22	24.6
12	21.7	26.4	29.1	18.6	23.5	26.1
N/A	Reserved					

Table 34: DDRIO Programmable Drive Strength

Drive Strength	IOH			IOL		
	1.8V	2.5V	3.3V	1.8V	2.5V	3.3V
1	1.9	2.7	3.1	2.1	2.8	3.3
2	3.4	4.4	4.9	2.9	3.8	4.4
3	5.4	7	7.9	4.9	6.5	7.4
4	6.8	8.6	9.6	5.7	7.3	8.2
5	8.6	11	12.4	7.6	9.9	11.2
6	9.9	12.5	14	8.3	10.7	12
7	11.8	14.8	16.6	10.2	13.2	14.9
8	11.6	14.6	16.3	10.2	13.2	14.9
9	12.9	16	17.7	10.9	14	15.7
10	14.7	18.2	20.2	12.7	16.3	18.3
11	15.9	19.5	21.6	13.4	17.1	19
12	17.4	21.6	23.9	15.1	19.2	21.3
13	19.2	23.7	26.2	16.3	20.9	23.5
14	21.5	26.3	28.9	18.2	23	25.6
15	22	27.1	29.8	18.7	23.9	26.8
N/A	Reserved					

Figure 23 and **Figure 24** illustrate quiescent current for QL1P075 and QL1P100 with VLP = 0 V and 3.3 V.

Figure 23: Quiescent Current for QL1P075 and QL1P100 with VLP = 0 V

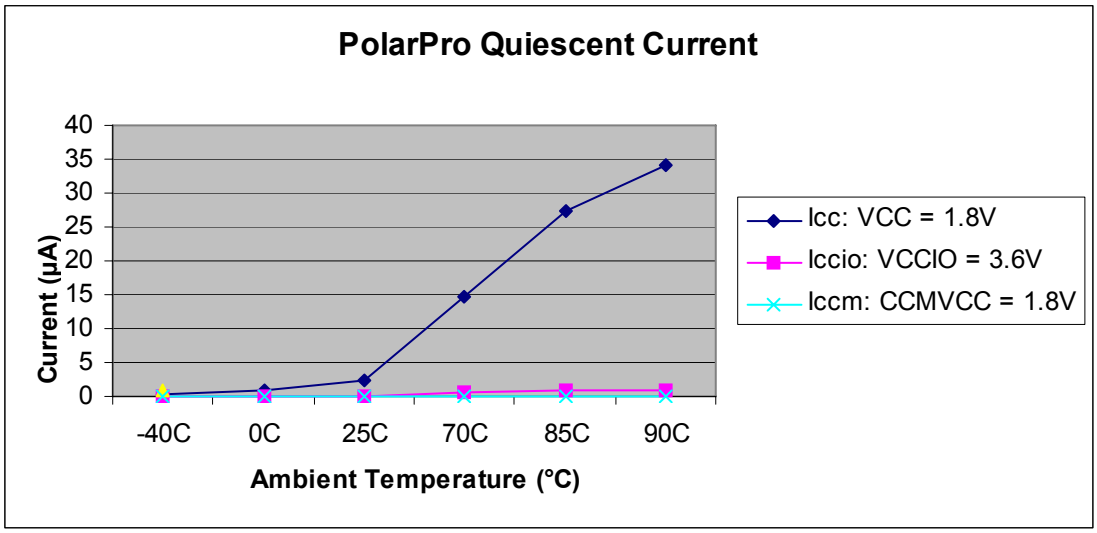


Figure 24: Quiescent Current for QL1P075 and QL1P100 with VLP = 3.3 V

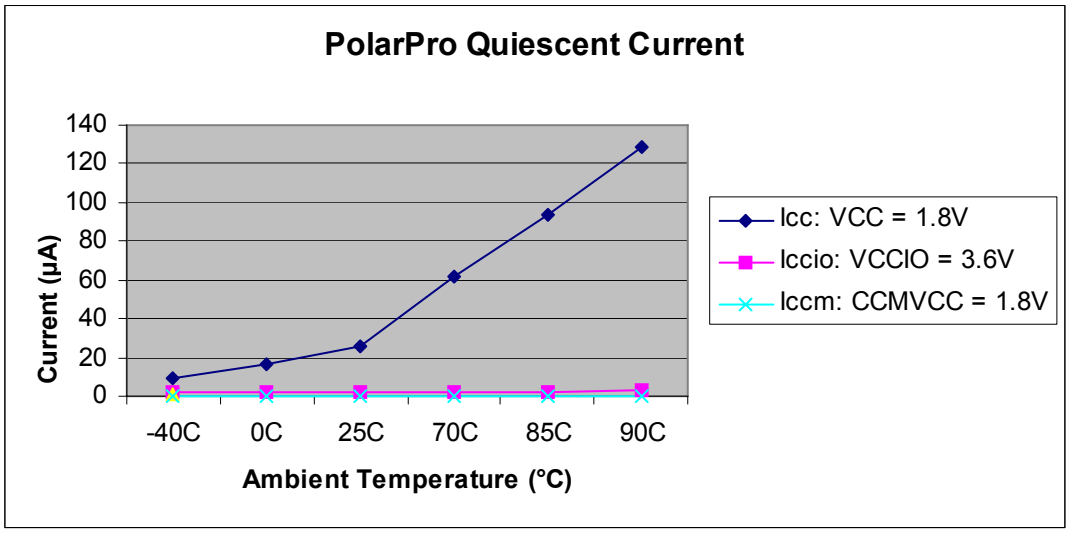


Figure 25 and **Figure 26** illustrate quiescent current for QL1P200 and QL1P300 with VLP = 0 V and 3.3 V.

Figure 25: Quiescent Current for QL1P200 and QL1P300 with VLP = 0 V

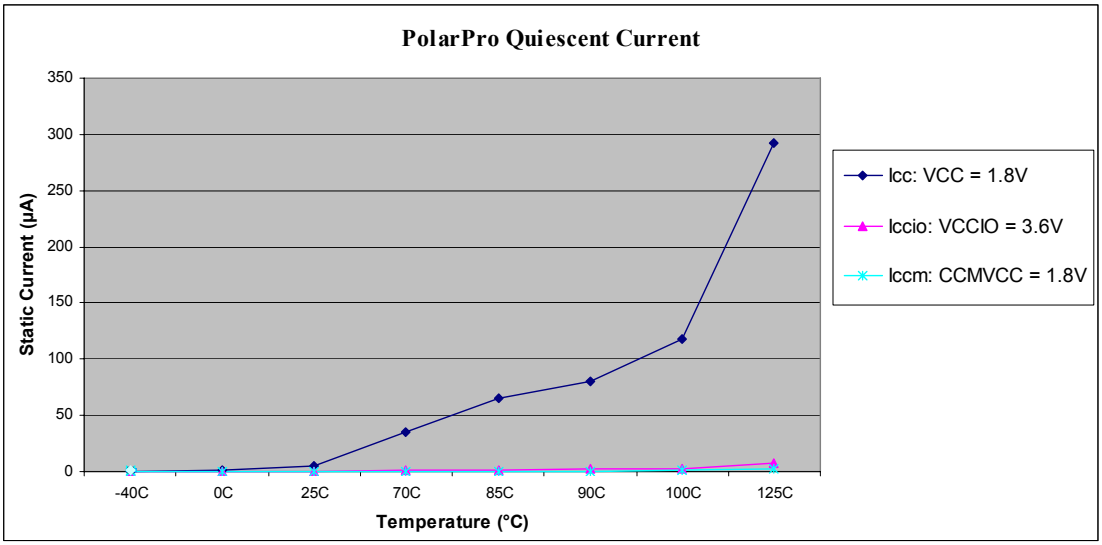
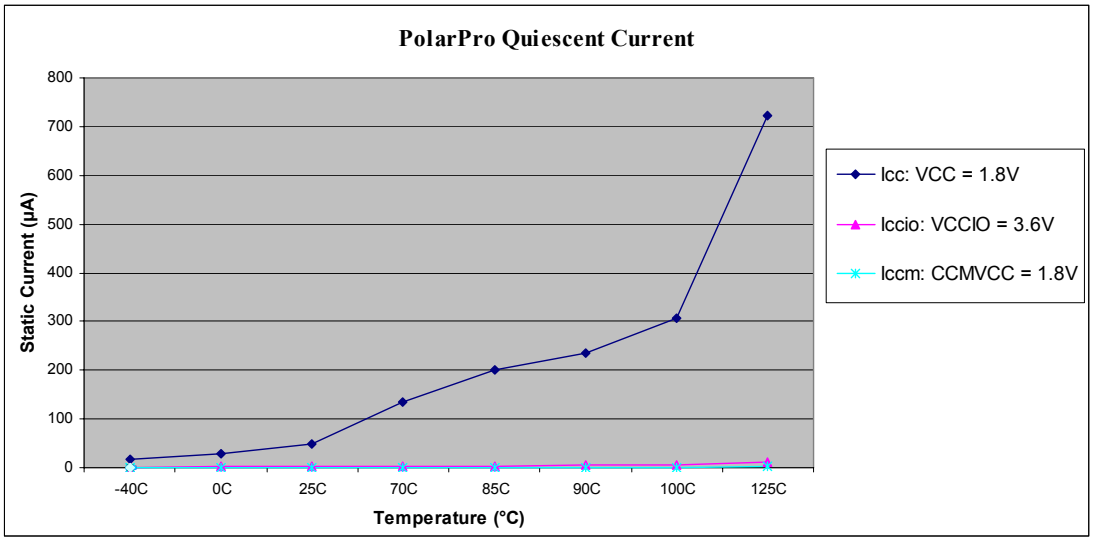


Figure 26: Quiescent Current for QL1P200 and QL1P300 with VLP = 3.3 V



AC Characteristics

AC specifications are provided in **Table 35** through **Table 51**. Logic cell diagrams and waveforms are provided in **Figure 27** through **Figure 42**. All of the following AC timing numbers are for worst case Commercial (T = 85°C Junction, V= 1.71V), and worst case Industrial (T = 100°C Junction, V=1.71V) conditions.

Figure 27: PolarPro Logic Cell

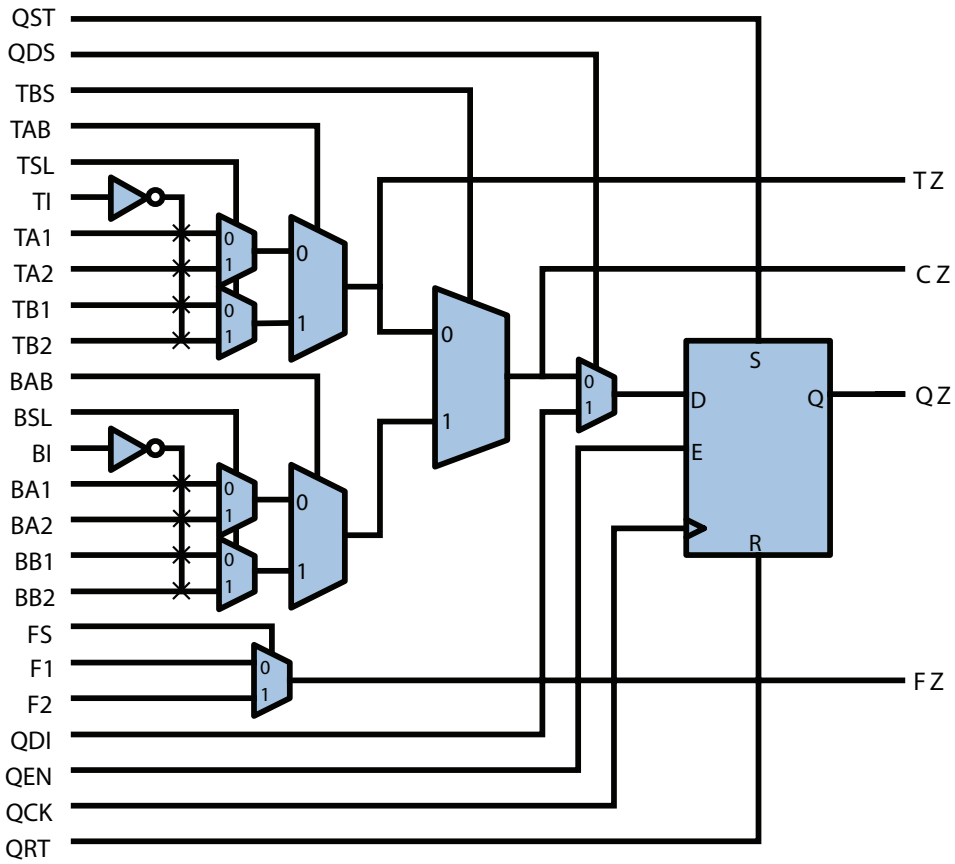


Table 35: Logic Cell Delays

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{PD}	Combinatorial delay of the longest path: time taken by the combinatorial circuit to output	0.32 ns	0.59 ns	0.34 ns	0.62 ns
t_{SU}	Setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	0.23 ns	0.56 ns	0.24 ns	0.58 ns
t_{HL}	Hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	0.32 ns	0 ns	0.34 ns
t_{ESU}	Enable setup time: time the enable input of the flip-flop must be stable before the active clock edge	0.23 ns	0.85 ns	0.89 ns	0.24 ns
t_{EHL}	Enable hold time: time the enable input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{CO}	Clock-to-out delay: the amount of time taken by the flip-flop to output after the active clock edge.	0.48 ns	0.52 ns	0.50 ns	0.55 ns
t_{CWHI}	Clock high time: required minimum time the clock stays high	0.46 ns	0.46 ns	0.46 ns	0.46 ns
t_{CWLO}	Clock low time: required minimum time that the clock stays low	0.46 ns	0.46 ns	0.46 ns	0.46 ns
t_{SET}	Set delay: time between when the flip-flop is “set” (high) and when the output is consequently “set” (high)	0.60 ns	0.60 ns	0.61 ns	0.61 ns
t_{RESET}	Reset delay: time between when the flip-flop is “reset” (low) and when the output is consequently “reset” (low)	0.68 ns	0.68 ns	0.71 ns	0.71 ns
t_{SW}	Set width: time that the SET signal must remain high/low	0.30 ns	0.30 ns	0.30 ns	0.30 ns
t_{RW}	Reset width: time that the RESET signal must remain high/low	0.30 ns	0.30 ns	0.30 ns	0.30 ns

Figure 28: Logic Cell Flip-Flop Timings—First Waveform

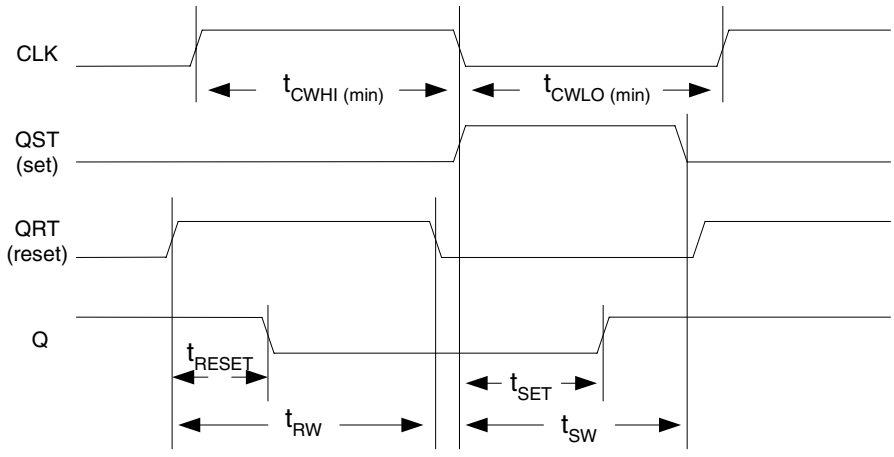


Figure 29: Logic Cell Flip-Flop Timings—Second Waveform

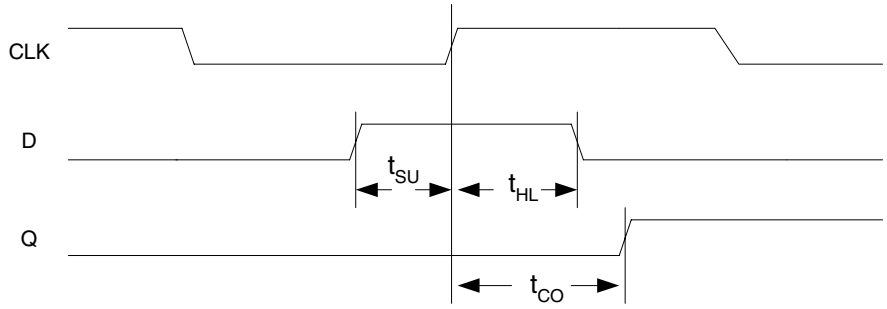


Figure 30: PolarPro Clock Network

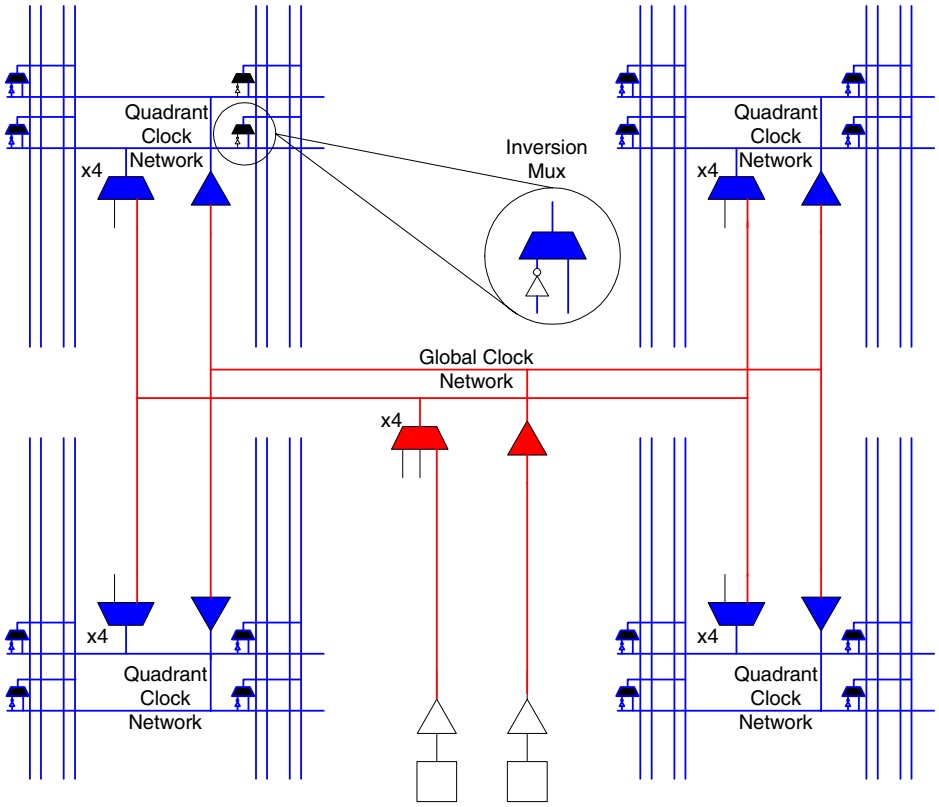
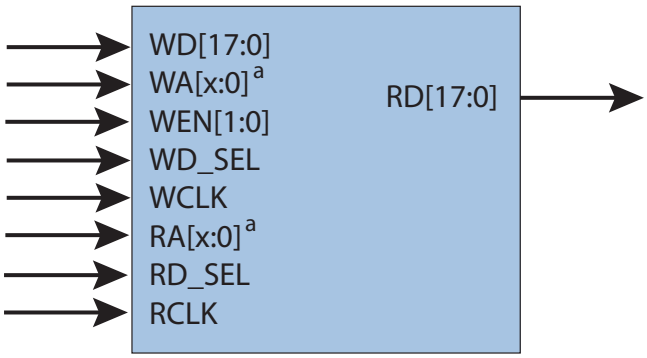


Table 36: PolarPro Tree Clock Delay

Clock Segment	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{PGCK}	Delay from global clock pad input to quadrant network	1.54 ns	1.86 ns	1.56 ns	1.88 ns
t_{PDCK}	Delay from dedicated clock pad input to quadrant network	1.4 ns	1.66 ns	1.42 ns	1.68 ns
t_{BGCK}	Global clock tree delay (quad net to flip-flop)	20 ps	200 ps	30 ps	220 ps
t_{GSKEW}	Global delay clock skew	30 ps	190 ps	40 ps	200 ps
t_{DSKEW}	Dedicated clock skew	30 ps	190 ps	40 ps	200 ps

RAM Timing

Figure 31: RAM Module



a. x=8 for 4-kilobit RAM blocks, x=9 for 8-kilobit RAM blocks.

Table 37: RAM Cell Synchronous Write Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{SWA}	WA setup time to WCLK: time the WRITE ADDRESS must be stable before the active edge of the WRITE CLOCK	0.29 ns	1.10 ns	0.31 ns	1.28 ns
t_{HWA}	WA hold time to WCLK: time the WRITE ADDRESS must be stable after the active edge of the WRITE CLOCK	0 ns	0.21 ns	0 ns	0.20 ns
t_{SWD}	WD setup time to WCLK: time the WRITE DATA must be stable before the active edge of the WRITE CLOCK	0.31 ns	1.74 ns	0.40 ns	2.21 ns
t_{HWD}	WD hold time to WCLK: time the WRITE DATA must be stable after the active edge of the WRITE CLOCK	0 ns	0.22 ns	0 ns	0.17 ns
t_{SWS}	WD_SEL setup time to WCLK: time WRITE CHIP SELECT must be stable before the active edge of the WRITE CLOCK	0.42 ns	1.10 ns	0.49 ns	1.28 ns
t_{HWS}	WD_SEL hold time to WCLK: time WRITE CHIP SELECT must be stable after the active edge of the WRITE CLOCK	0 ns	0.04 ns	0 ns	0.04 ns
t_{SWE}	WEN setup time to WCLK: time the WRITE ENABLE must be stable before the active edge of the WRITE CLOCK	0.63 ns	1.10 ns	0.74 ns	1.28 ns
t_{HWE}	WEN hold time to WCLK: time the WRITE ENABLE must be stable after the active edge of the WRITE CLOCK	0 ns	0 ns	0 ns	0 ns

Figure 32: RAM Cell Write Timing

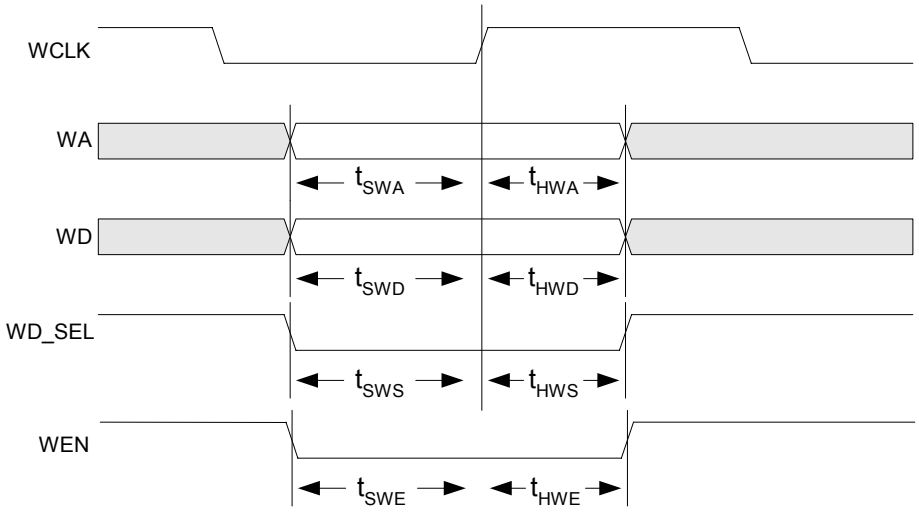
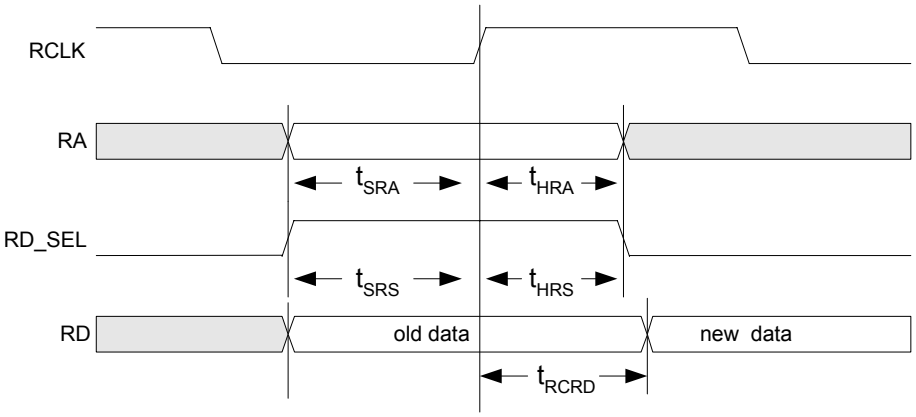


Table 38: RAM Cell Synchronous Read Timing

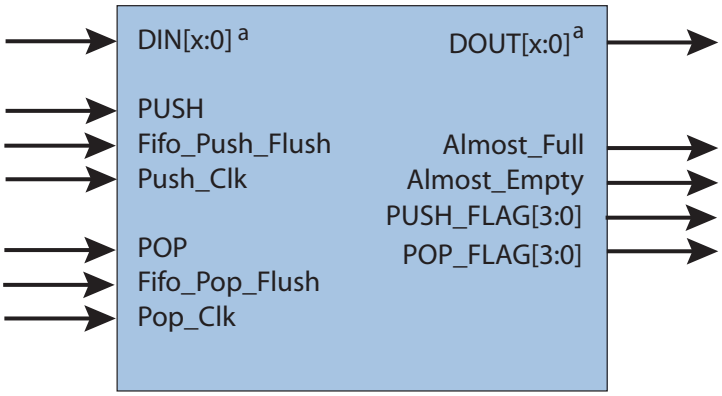
Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{SRA}	RA setup time to RCLK: time the READ ADDRESS must be stable before the active edge of the READ CLOCK	0.29 ns	1.10 ns	0.31 ns	1.28 ns
t_{HRA}	RA hold time to RCLK: time the READ ADDRESS must be stable after the active edge of the READ CLOCK	0 ns	0.21 ns	0 ns	0.20 ns
t_{SRS}	RD_SEL setup time to RCLK: time the READ CHIP SELECT must be stable before the active edge of the READ CLOCK	0.42 ns	1.10 ns	0.49 ns	1.28 ns
t_{HRS}	RD_SEL hold time to RCLK: time the READ CHIP SELECT must be stable after the active edge of the READ CLOCK	0 ns	0.04 ns	0 ns	0.04 ns
t_{RCRD}	RCLK to RD: time between the active READ CLOCK edge and the time when the data is available at RD	2.62 ns	5.67 ns	2.69 ns	5.88 ns

Figure 33: RAM Cell Read Timing



FIFO Timing

Figure 34: FIFO Module



a. x = {1,2,3,....35}.

Table 39: FIFO PUSH Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{SPUSHD}	DIN setup time to Push_Clk: time DIN must be stable before the active edge of the FIFO Push clock	0.31 ns	1.74 ns	0.40 ns	2.21 ns
t_{HPUSHD}	DIN hold time to Push_Clk: time DIN must be stable after the active edge of the FIFO Push clock	0 ns	0.22 ns	0 ns	0.17 ns
$t_{SPUSHEN}$	PUSH setup time to Push_Clk: time PUSH must be stable before the active edge of the FIFO Push clock	1.07 ns	1.57 ns	1.38 ns	2.0 ns
$t_{HPUSHEN}$	PUSH hold time to Push_Clk: time PUSH must be stable after the active edge of the FIFO Push clock	0 ns	0 ns	0 ns	0 ns
$t_{SPUSHFLUSH}$	FLUSH setup time to Push_Clk: time Fifo_Push_Flush must be stable before the active edge of the FIFO Push clock	1.11 ns	1.74 ns	1.43 ns	2.21 ns
$t_{HPUSHFLUSH}$	FLUSH hold time to Push_Clk: time Fifo_Push_Flush must be stable after the active edge of the FIFO Push clock	0 ns	0 ns	0 ns	0 ns
t_{COAF}	Clock-to-out of Almost Full	2.66 ns	3.34 ns	2.72 ns	3.42 ns
$t_{COPUSHFLAG}$	Clock-to-out of FIFO Push level indicator	2.36 ns	4.20 ns	2.41 ns	4.32 ns

Figure 35: FIFO PUSH Timing

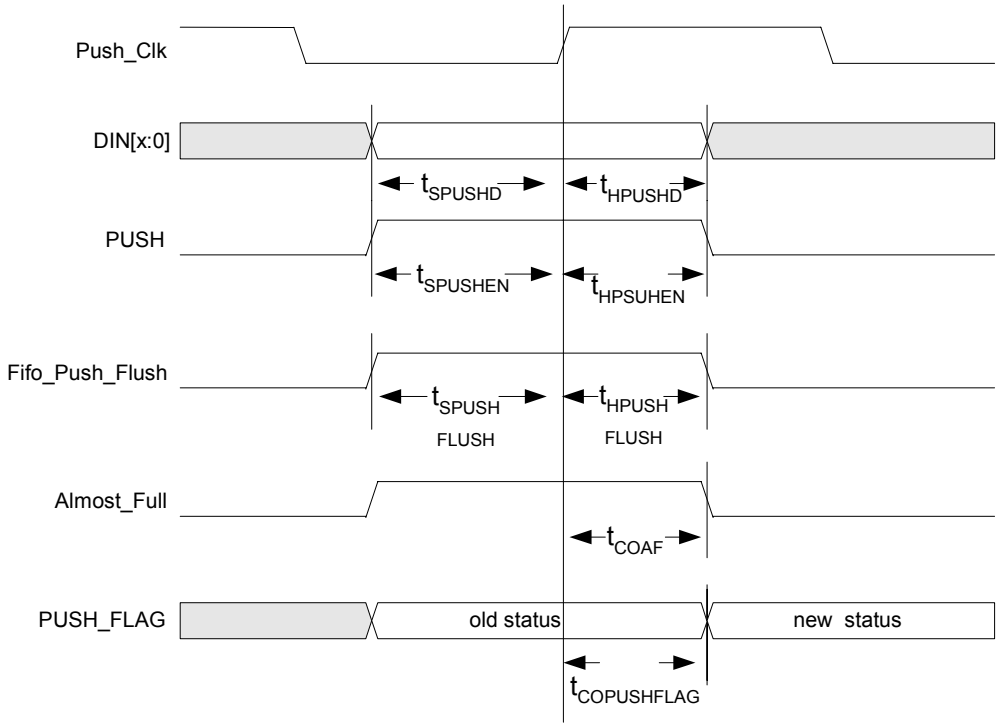
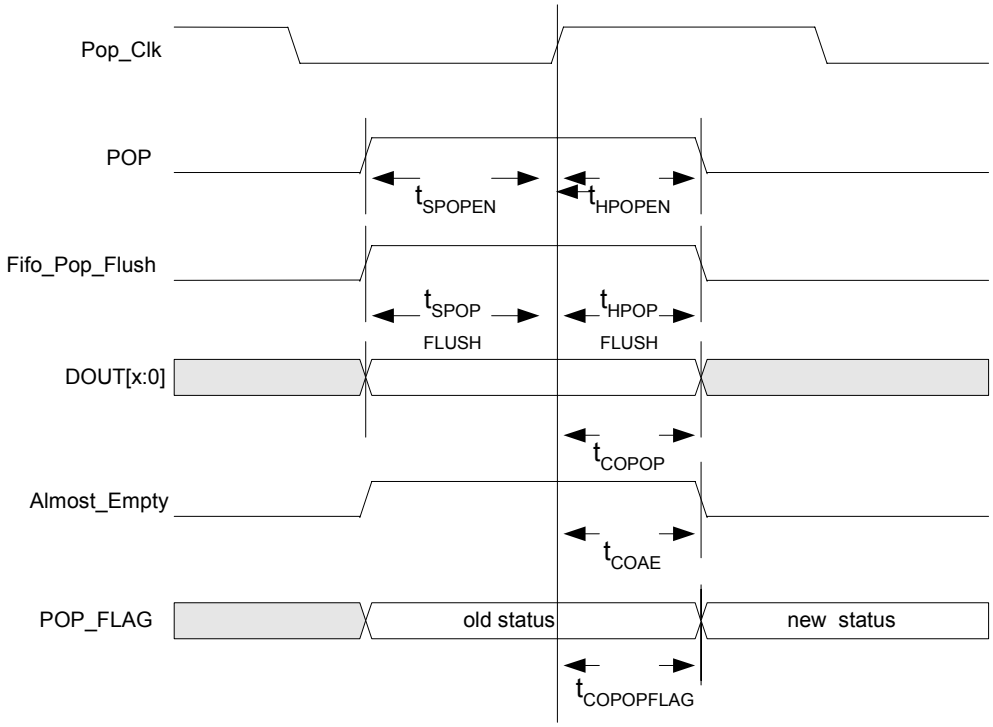


Table 40: FIFO POP Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{SPOPEN}	POP setup time to Pop_Clk: time POP must be stable before the active edge of the FIFO Pop clock	1.01 ns	1.13 ns	1.19 ns	1.32 ns
t_{HPOPEN}	POP hold time to Pop_Clk: time POP must be stable after the active edge of the FIFO Pop clock	0 ns	0 ns	0 ns	0 ns
$t_{SPOPFLUSH}$	FLUSH setup time to Pop_Clk: time Fifo_Pop_Flush must be stable before the active edge of the FIFO Pop clock	1.11 ns	1.74 ns	1.43 ns	2.21 ns
$t_{HPOPFLUSH}$	FLUSH hold time to Pop_Clk: time Fifo_Pop_Flush must be stable after the active edge of the FIFO Pop clock	0 ns	0 ns	0 ns	0 ns
t_{FPOP}	Pop_Clk to Pop: Clock-to-out from the active FIFO CLOCK edge and the time when the data is popped from the FIFO at DOUT	2.32 ns	5.61 ns	2.37 ns	5.88 ns
t_{COAE}	Clock-to-out of Almost Empty	2.64 ns	3.58 ns	2.70 ns	3.66 ns
$t_{COPOPFLAG}$	Clock-to-out of FIFO Pop level indicator	2.32 ns	3.93 ns	2.38 ns	4.03 ns

Figure 36: FIFO POP Timing



GPIO Cell Timing

Figure 37: PolarPro I/O Cell Output Path

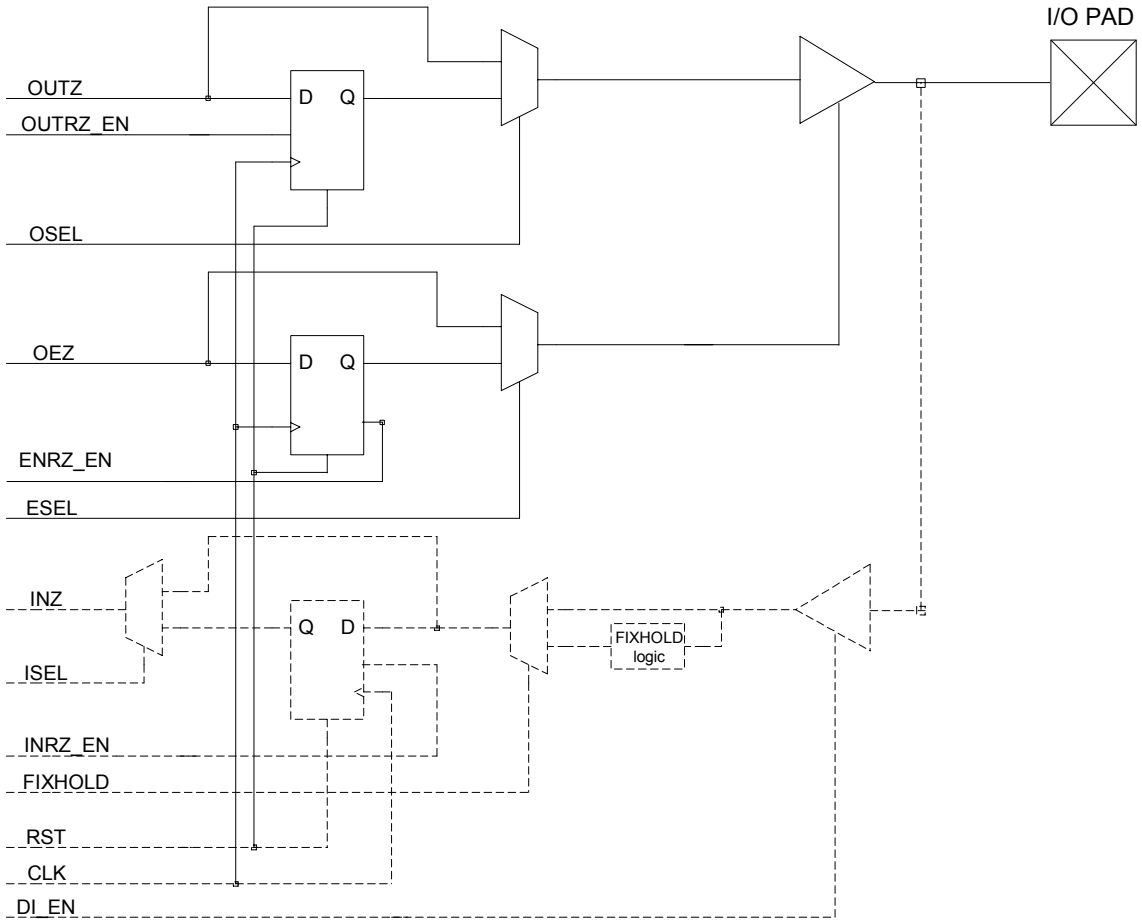


Figure 38: PolarPro I/O Cell Output Enable Timing

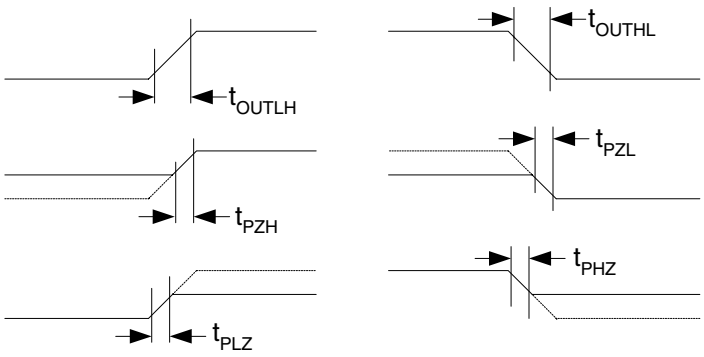


Table 41: Output Timing Characteristics @ VCCIO = 3.3 V, T = 25° C

Symbol	Parameter	Value (ns)	
		Slowest Slew Max.	Fastest Slew Max.
t_{OUTLH}	Output Delay low to high (90% of H)	8.10	1.00
t_{OUTHL}	Output Delay high to low (10% of L)	9.60	0.90
t_{PZH}	Output Delay tri-state to high (90% of H)	3.40	0.30
t_{PZL}	Output Delay tri-state to low (10% of L)	3.90	0.30
t_{PHZ}	Output Delay high to tri-state	3.60	0.36
t_{PLZ}	Output Delay low to tri-state	4.1	0.41

Table 42: Output Timing Characteristics @ VCCIO = 2.5 V, T = 25° C

Symbol	Parameter	Value (ns)	
		Slowest Slew Max.	Fastest Slew Max.
t_{OUTLH}	Output Delay low to high (90% of H)	12.20	1.10
t_{OUTHL}	Output Delay high to low (10% of L)	18.80	1.00
t_{PZH}	Output Delay tri-state to high (90% of H)	4.50	0.45
t_{PZL}	Output Delay tri-state to low (10% of L)	8.40	0.52
t_{PHZ}	Output Delay high to tri-state	8.10	0.52
t_{PLZ}	Output Delay low to tri-state	5.30	0.53

Table 43: Output Timing Characteristics @ VCCIO = 1.8 V, T = 25° C

Symbol	Parameter	Value (ns)	
		Slowest Slew Max.	Fastest Slew Max.
t_{OUTLH}	Output Delay low to high (90% of H)	2.50	2.20
t_{OUTHL}	Output Delay high to low (10% of L)	1.70	1.40
t_{PZH}	Output Delay tri-state to high (90% of H)	8.30	0.70
t_{PZL}	Output Delay tri-state to low (10% of L)	24.70	1.05
t_{PHZ}	Output Delay high to tri-state	23.50	1.25
t_{PLZ}	Output Delay low to tri-state	10.80	0.78

Table 44 lists the typical output slew rates (in V/ns) across three levels of output voltages, with a drive strength of 4, and a load capacitor of 10 pF.

Table 44: GPIO Output Slew Rate

Slew	Output Slew Rate (V/ns) at VCCIO =		
	1.8 V	2.5 V	3.3 V
slow	n/a	0.20	0.36
fast	n/a	0.31	0.66
vfast	0.17	0.61	1.32
wow	0.25	1.18	2.03

Table 45: I/O Output Register Cell Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{OSU}	Output register setup time: time the synchronous OUTZ input of the flip-flop must be stable before the active clock edge	0.33 ns	0.38 ns	0.34 ns	0.36 ns
t_{OHL}	Output register hold time: time the synchronous OUTZ input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OCO}	Output register clock-to-out: time taken by the flip-flop to output after the active clock edge	5.25 ns	5.99 ns	5.46 ns	6.29 ns
t_{ORST}	Output register reset delay: time between when the flip-flop is “reset” (low) and when the output is consequently “reset” (low)	5.85 ns	5.85 ns	6.03 ns	6.03 ns
t_{OESU}	Output register clock enable setup time: time OUTRZ_EN must be stable before the active clock edge	0.33 ns	0.51 ns	0.30 ns	0.54 ns
t_{OEH}	Output register clock enable hold time: time OUTRZ_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OEZSU}	Output register clock enable setup time: time OEZ must be stable before the active clock edge	0.14 ns	0.20 ns	0.15 ns	0.18 ns
t_{OEZH}	Output register clock enable hold time: time OEZ must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OPD}	Output signal propagation delay: propagation delay of OUTZ to the output pad	4.82 ns	5.44 ns	5.03 ns	5.72 ns

Figure 39: PolarPro I/O Cell Input Path

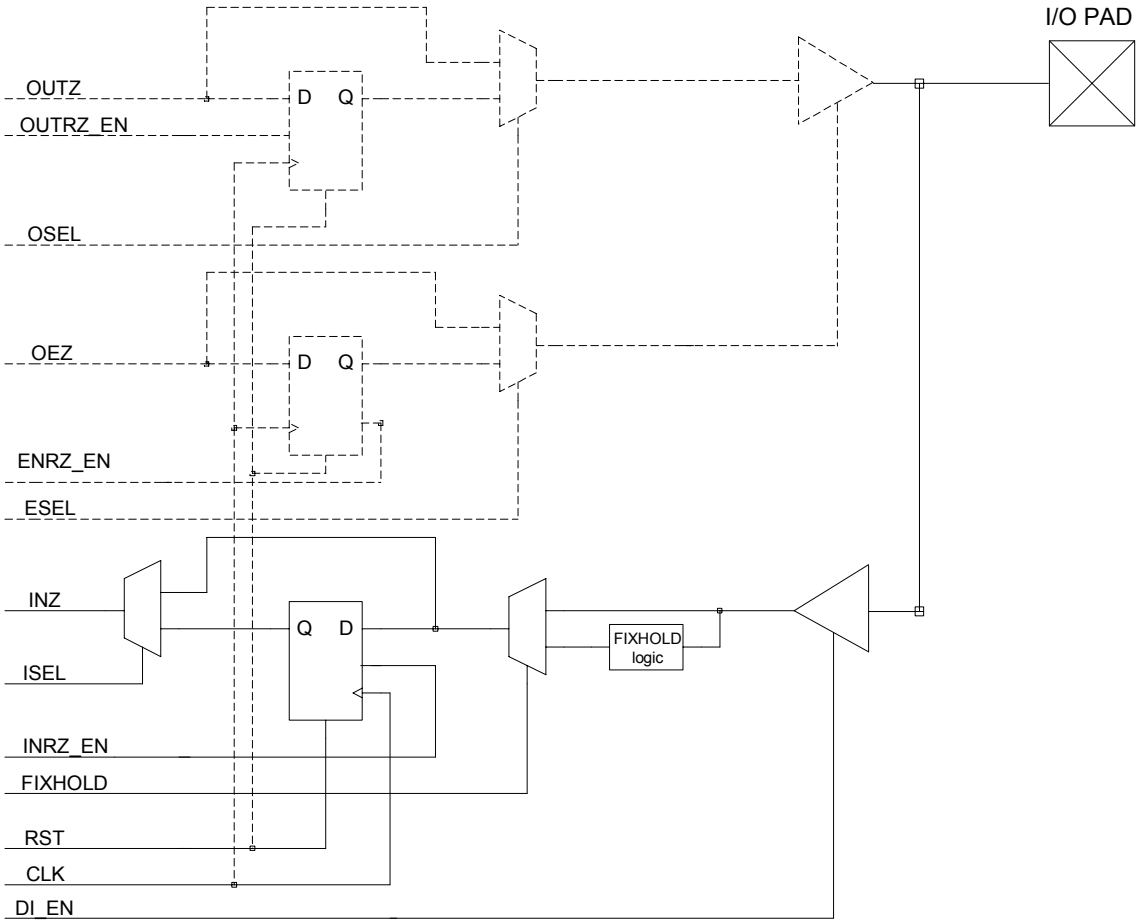


Figure 40: PolarPro Input Register Cell Timing

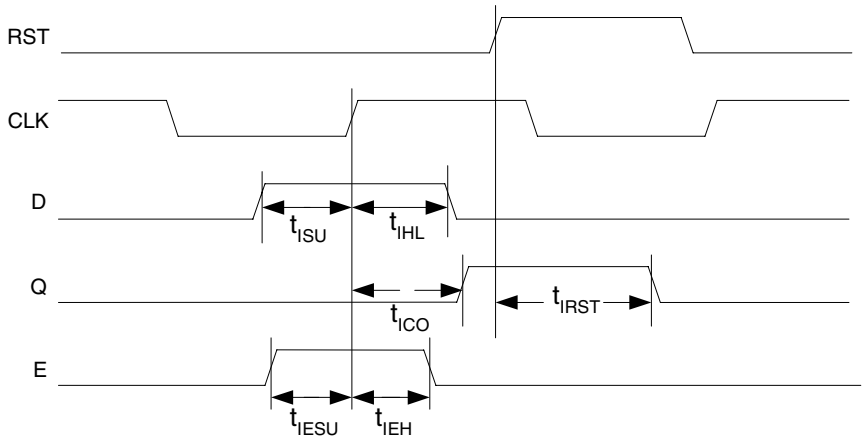


Table 46: I/O Input Register Cell Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{ISU}	Input register setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	2.51 ns	2.85 ns	2.80 ns	2.82 ns
t_{IHL}	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{ICO}	Input register clock-to-out: time taken by the flip-flop to output after the active clock edge	1.68 ns	2.66 ns	1.58 ns	2.70 ns
t_{IRST}	Input register reset delay: time between when the flip-flop is “reset” (low) and when the output is consequently “reset” (low)	1.59 ns	1.59 ns	1.53 ns	1.53 ns
t_{IESU}	Input register clock enable setup time: time INRZ_EN must be stable before the active clock edge	0.25 ns	0.40 ns	0.23 ns	0.43 ns
t_{IEH}	Input register clock enable hold time: time INRZ_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
$t_{IDIENSU}$	Input data enable setup time: time DI_EN must be stable before the active clock edge	2.39 ns	5.38 ns	2.28 ns	5.63 ns
t_{IDIENH}	Input data enable hold time: time DI_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{IFHSU}	Input fixhold setup time: time FIXHOLD must be stable before the active clock edge	2.39 ns	5.38 ns	2.28 ns	5.63 ns
t_{IFHH}	Input fixhold hold time: time FIXHOLD must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns

Table 47: I/O Input Buffer Delays

Symbol	Parameter	Value	
	To get the total input delay add this delay to t_{ISU}	Min.	Max.
t_{SID} (LVTTL)	LVTTL input delay: Low Voltage TTL for 3.3 V applications	TBD	TBD
t_{SID} (LVCMOS2)	LVCMOS2 input delay: Low Voltage CMOS for 2.5 V and lower applications	TBD	TBD
t_{SID} (LVCMOS18)	LVCMOS18 input delay: Low Voltage CMOS for 1.8 V applications	TBD	TBD
t_{SID} (GTL+)	GTL+ input delay: Gunning Transceiver Logic	TBD	TBD
t_{SID} (SSTL3)	SSTL3 input delay: Stub Series Terminated Logic for 3.3 V	TBD	TBD
t_{SID} (SSTL2)	SSTL2 input delay: Stub Series Terminated Logic for 2.5 V	TBD	TBD
t_{SID} (PCI)	PCI input delay: Peripheral Component Interconnect for 3.3 V	TBD	TBD

DDR Cell Timing

Figure 41: DDRIO DQ Configuration

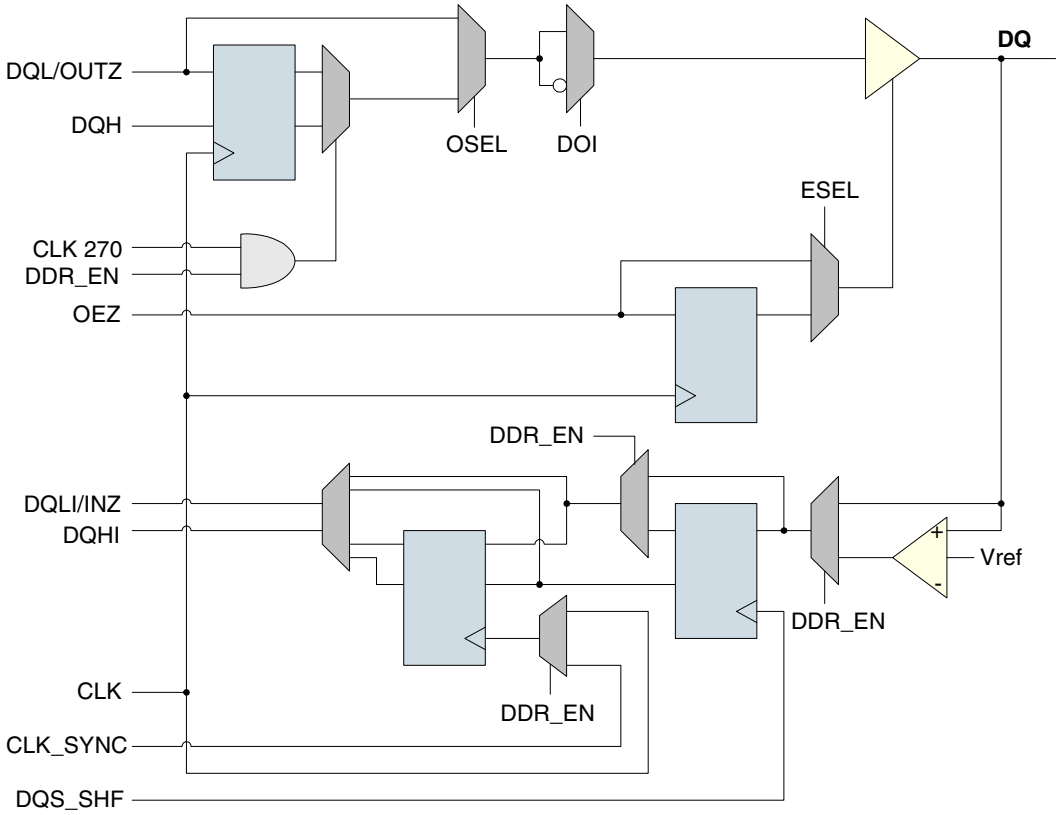


Table 48: DQ Cell Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{DQLSU}	Output register setup time: time the synchronous DQL input of the flip-flop must be stable before the active clock edge	0.37 ns	0.38 ns	0.35 ns	0.39 ns
t_{DQLH}	Output register hold time: time the synchronous DQL input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OCO}	Output register clock-to-out: time taken by the DQL flip-flop to output to the DQ pad after the active clock edge	4.13 ns	4.39 ns	4.48 ns	4.85 ns
t_{ODQHSU}	Output higher bit register clock setup time: time DQH must be stable before the active clock edge	0.32 ns	0.34 ns	0.31 ns	0.35 ns
t_{ODQHH}	Output higher bit register clock hold time: time DQH must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OPD}	Output propagation delay: propagation time from DQL to the output pad	3.64 ns	3.92 ns	4.17 ns	4.20 ns

Table 48: DQ Cell Timing *(Continued)*

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{IDQSU}	Input register setup time: time DQ must be stable before the active clock edge	1.45 ns	1.48 ns	1.24 ns	1.69 ns
t_{IDQH}	Input register hold time: time DQ must be stable after the active clock edge	0.62 ns	0.65 ns	0.47 ns	0.83 ns
t_{IPD}	Input propagation delay: propagation time from DQ to DQLI	2.35 ns	2.63 ns	2.19 ns	2.75 ns

Table 49: DQ Cell Configured as a GPIO Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{OSU}	Output register setup time: time the synchronous OUTZ input of the flip-flop must be stable before the active clock edge	0.37 ns	0.38 ns	0.35 ns	0.39 ns
t_{OH}	Output register hold time: time the synchronous OUTZ input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OCO}	Output register clock-to-out: time taken by the OUTZ flip-flop to output to the output pad after the active clock edge	4.17 ns	4.43 ns	4.61 ns	4.80 ns
t_{OESU}	Output data enable setup time: time OEZ must be stable before the active clock edge	0.43 ns	0.54 ns	0.42 ns	0.55 ns
t_{OEH}	Output data enable hold time: time OEZ must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OESU}	Output register clock enable setup time: time OUTRZ_EN must be stable before the active clock edge	0.38 ns	0.64 ns	0.35 ns	0.67 ns
t_{OEH}	Output register clock enable hold time: time OUTRZ_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OPD}	Output propagation delay: propagation time from OUTZ to the output pad	3.65 ns	3.87 ns	4.06 ns	4.24 ns
t_{ISU}	Input register setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	2.54 ns	2.63 ns	2.46 ns	2.62 ns
t_{IHL}	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{ICO}	Input register clock-to-out: time taken by the flip-flop to output to INZ after the active clock edge	2.88 ns	3.12 ns	2.73 ns	3.21 ns
t_{IESU}	Input register clock enable setup time: time INRZ_EN must be stable before the active clock edge	0.26 ns	0.55 ns	0.23 ns	0.58 ns
t_{IEH}	Input register clock enable hold time: time INRZ_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{IPD}	Input propagation delay: propagation time from the input pad to INZ	2.35 ns	3.12 ns	2.19 ns	3.21 ns

Figure 42: DDRIO DQS Configuration

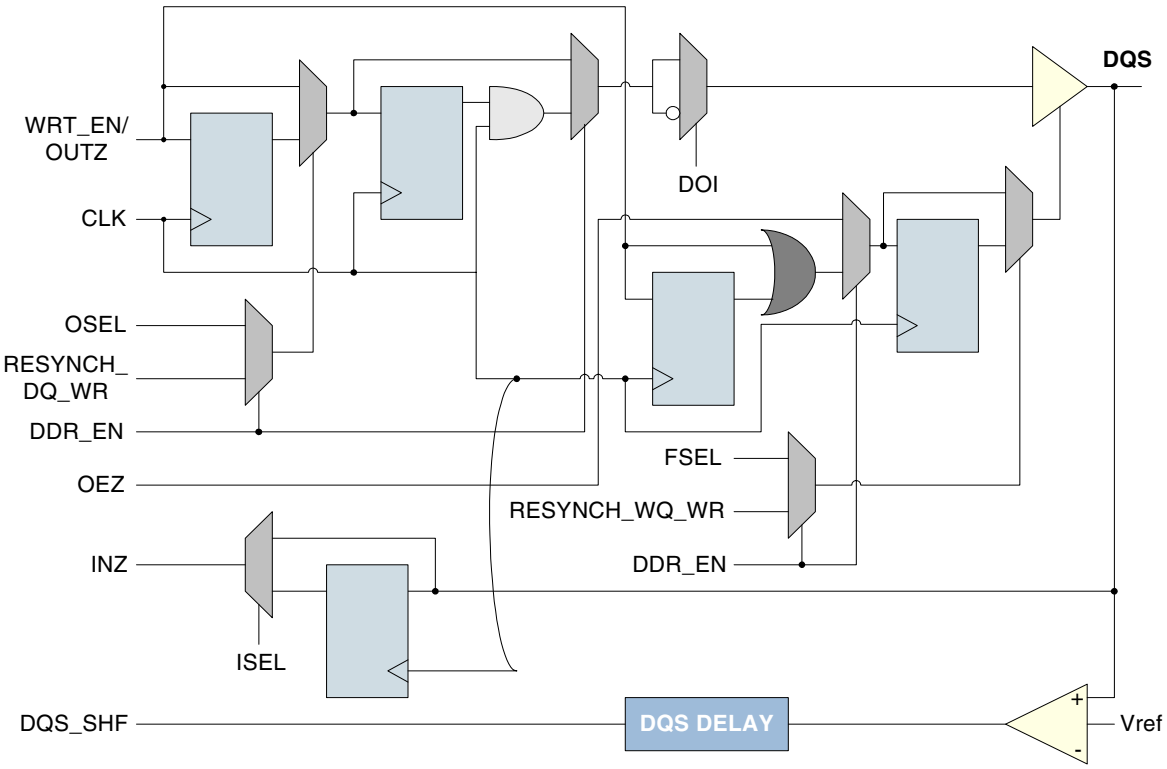


Table 50: DQS Cell Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{WESU}	Output register setup time: time the synchronous WRT_EN input of the flip-flop must be stable before the active clock edge	0.61 ns	0.64 ns	0.61 ns	0.64 ns
t_{WEH}	Output register hold time: time the synchronous WRT_EN input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{WEPD}	Output propagation delay: propagation time from WRT_EN to the output pad	3.56 ns	3.62 ns	3.85 ns	3.99 ns
t_{IDQSPD}	Input propagation delay: propagation time from DQS to DQS_SHF	1.58 ns	3.53 ns	1.37 ns	3.77 ns

Table 51: DQS Cell Configured as a GPIO Timing

Symbol	Parameter	Commercial		Industrial	
		Min.	Max.	Min.	Max.
t_{OSU}	Output register setup time: time the synchronous OUTZ input of the flip-flop must be stable before the active clock edge	0.47 ns	0.48 ns	0.45 ns	0.50 ns
t_{OH}	Output register hold time: time the synchronous OUTZ input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OCO}	Output register clock-to-out: time taken by the OUTZ flip-flop to output to the output pad after the active clock edge	4.14 ns	4.46 ns	4.66 ns	4.77ns
t_{OESU}	Output data enable setup time: time OEZ must be stable before the active clock edge	0.47 ns	0.49 ns	0.49 ns	0.49 ns
t_{OEH}	Output data enable hold time: time OEZ must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OESU}	Output register clock enable setup time: time OUTRZ_EN must be stable before the active clock edge	0.35 ns	0.66 ns	0.33 ns	0.77 ns
t_{OEH}	Output register clock enable hold time: time OUTRZ_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{OPD}	Output propagation delay: propagation time from OUTZ to the output pad	3.88 ns	4.13 ns	4.41 ns	4.42 ns
t_{ISU}	Input register setup time: time the synchronous input of the flip-flop must be stable before the active clock edge	2.38 ns	2.45 ns	2.47 ns	2.29 ns
t_{IHL}	Input register hold time: time the synchronous input of the flip-flop must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{ICO}	Input register clock-to-out: time taken by the flip-flop to output to INZ after the active clock edge	2.76 ns	2.78 ns	2.73 ns	3.21 ns
t_{IESU}	Input register clock enable setup time: time INRZ_EN must be stable before the active clock edge	0.40 ns	0.71 ns	0.23 ns	0.58 ns
t_{IEH}	Input register clock enable hold time: time INRZ_EN must be stable after the active clock edge	0 ns	0 ns	0 ns	0 ns
t_{IPD}	Input propagation delay: propagation time from the input pad to INZ	2.25 ns	2.78 ns	2.19 ns	3.21 ns

Package Thermal Characteristics

The PolarPro device is available for Commercial (0°C to 85°C Junction), Industrial (-40°C to 100°C Junction), and Military (-55°C to 125°C Junction) temperature ranges.

Thermal Resistance Equations:

$\theta_{JC} = (T_J - T_C)/P$
$\theta_{JA} = (TJ - TA)/P$
$P_{MAX} = (T_{JMAX} - T_{AMAX})/\theta_{JA}$

Parameter Description:

θ_{JC}: Junction-to-case thermal resistance

θ_{JA}: Junction-to-ambient thermal resistance

T_J: Junction temperature

T_A: Ambient temperature

P: Power dissipated by the device while operating

P_{MAX}: The maximum power dissipation for the device

T_{JMAX}: Maximum junction temperature

T_{AMAX}: Maximum ambient temperature

NOTE: Maximum junction temperature (T_{JMAX}) is 125°C. To calculate the maximum power dissipation for a device package look up θ_{JA} from **Table 52**, pick an appropriate T_{AMAX} and use:
$P_{MAX} = (125°C - T_{AMAX})/ \theta_{JA}$

Table 52: Package Thermal Characteristics

Package Description				Theta-JA (° C/W)		
Device	Package Code	Package Type	Pin Count	0 LFM	200 LFM	400 LFM
QL1P075	PF	TQFP	144	50	44	42
	PT	TFBGA (12 mm x 12 mm)	196	42.0	35.0	33.5
	PS	LBGA	256	48.2	41.7	40.2
QL1P100	PF	TQFP	144	50	44	42
	PT	TFBGA (12 mm x 12 mm)	196	42.0	35.0	33.5
	PS	LBGA	256	48.2	41.7	40.2
QL1P150	PS	LBGA	256	35.5	29.0	27.7
	PS	LBGA	324	TBD	TBD	TBD
QL1P300	PS	LBGA	256	35.5	29.0	27.7
	PS	LBGA	324	TBD	TBD	TBD
QL1P600	PS	LBGA	256	TBD	TBD	TBD
	PS	LBGA	324	TBD	TBD	TBD
QL1P1000	PS	LBGA	256	TBD	TBD	TBD
	PS	LBGA	324	TBD	TBD	TBD

Moisture Sensitivity Level

All PolarPro devices are Moisture Sensitivity Level 3.

Table 53: Solder and Lead Finish Composition

	Lead Included	Lead-free
BGA Solder	63% Pb, 37% Sn	Sn3AgCu:Sn4AgCu[a]
QFP Lead Finish	85% Pb, 15% Sn	Sn (matte)

a. Sn3AgCu:Sn4AgCu means that Ag can range from 3% to 4%. Cu is always 0.5%.

Power Vs. Operating Frequency

The basic power equation which best models power consumption is given below:

$$P_{TOTAL} = 0.350 + f[0.0031\ \eta_{LC} + 0.0948\ \eta_{CKBF} + 0.01\ \eta_{CLBF} + 0.0263\ \eta_{CKLD} + 0.543\ \eta_{RAM} + 0.20\ \eta_{PLL} + 0.0035\ \eta_{INP} + 0.0257\ \eta_{OUTP}]\ (mW)$$

Where:

η_{LC} = number of logic cells in the design

η_{CKBF} = number of clock buffers

η_{CLBF} = number of column clock buffers

η_{CKLD} = number of loads connected to the column clock buffers

η_{RAM} = number of RAM blocks

η_{PLL} = number of PLLs

η_{INP} = number of input pins

η_{OUTP} = number of output pins

NOTE: To learn more about power consumption, see QuickLogic Application Note 60 at http://www.quicklogic.com/images/appnote60.pdf.

Power-Up Sequencing

Figure 43: Power-Up Sequencing

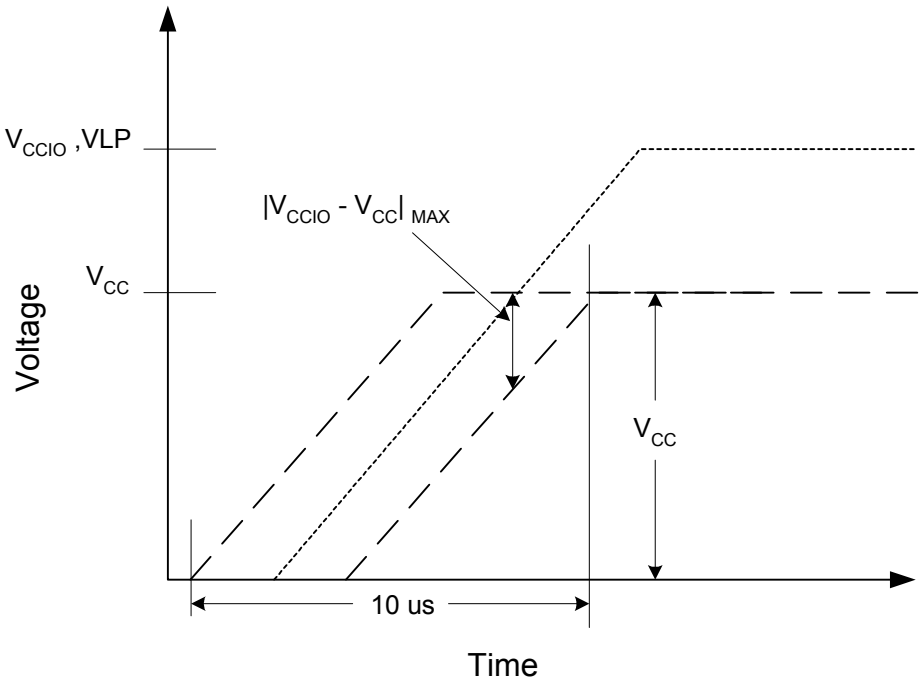


Figure 43 shows an example where all VCCIO = 3.3 V.

When powering up a PolarPro device, VCC, VCCIO rails must take 10 µs or longer to reach the maximum value (refer to **Figure 43**). Ramping VCC and VCCIO faster than 10 µs can cause the device to behave improperly.

It is also important to ensure VCCIO and VLP are within 500 mV of VCC when ramping up the power supplies. In the case where VCCIO or VLP are greater than VCC by more than 500 mV an additional current draw can occur as VCC passes its threshold voltage. In a case where VCC is greater than VCCIO by more than 500 mV the protection diodes between the power supplies become forward biased. If this occurs then there will be an additional current load on the power supply. Having the diodes on can cause a reliability problem, since it can wear out the diodes and subsequently damage the internal transistors.

Programming Stipulation

For PolarPro devices to correctly program, there must not be any race conditions or internally generated free-running oscillators in the design. This will cause an ICC programming failure during the programming process. QuickLogic cannot guarantee the operation of any device that fails programming. Therefore, race conditions and free-running oscillators must be removed from designs so that PolarPro devices can correctly pass programming.

Pin Descriptions

Table 54: Pin Descriptions

Pin	Direction	Function	Description
Dedicated Pin Descriptions			
GPIO(C:A)	I/O	General purpose input/output pin	The I/O pin is a bi-directional pin, configurable to either an input-only, output-only, or bi-directional pin. The letter inside the parenthesis means that the I/O is located in the bank with that letter. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
CLK(C:A)	I	Global clock network pin low skew global clock	This pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to the Logic Cell, READ and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The voltage tolerance of this pin is specified by VCCIO(C:A).
DEDCLK(D)	I	Dedicated clock network pin low skew clock	This pin provides access to a distributed network capable of driving the CLOCK, SET, RESET, all inputs to the Logic Cell, READ and WRITE CLOCKS, Read and Write Enables of the Embedded RAM Blocks, and I/O inputs. The voltage tolerance of this pin is specified by VCCIO(D).
CCMIN(1:0)	I	CCM clock input	Input clock for CCM. The voltage tolerance for this pin is specified by the VCCIO of the same bank.
CCMVCC (1:0)	I	Power supply pin for CCM	CCM input voltage level. Configurable as 1.8 V only.
CCMGND(1:0)	I	Ground pin for CCM	Connect to ground.
VLP	I	Voltage low power	Active low. Therefore, when VLP pin is low, the device will go into low power mode. Tie VLP to 3.3 V to disable low power mode.
VCC	I	Power supply pin	Connect to 1.8 V supply.
VCCIO(D:A)	I	Input voltage tolerance pin	This pin provides the flexibility to interface the device with either a 3.3 V, 2.5 V, or 1.8 V device. The letter inside the parenthesis means that the VCCIO is located in the bank with that letter. Every I/O pin in the same bank will be tolerant of the same VCCIO input signals and will drive VCCIO level output signals. This pin must be connected to either 3.3 V, 2.5 V, or 1.8 V.
GND	I	Ground pin	Connect to ground.
DQ/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ or as a general purpose I/O	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
DQS/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQS or as a general purpose I/O	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.

Table 54: Pin Descriptions *(Continued)*

Pin	Direction	Function	Description
DQCK_N/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ, DDR negative clock, or as a general purpose I/O.	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of tying that pin to GND, VCCIO, or Hi-Z.
DQCK_P/ GPIO(D)	I/O	Configurable pin can be declared as either a DDRIO DQ, DDR positive clock, or as a general purpose I/O.	The D inside the parenthesis means that the I/O is located in Bank D. If an I/O is not used, the development software provides the option of typing that pin to GND, VCCIO, or Hi-Z.
VREF(D)	I	Differential reference voltage	The INREF is the reference voltage pin for the SSTL1.8 and SSTL2 standards. The D inside the parenthesis means that INREF is located in Bank D. Tie this pin to GND if voltage referenced standards are not used.
JTAG Pin Descriptions			
TDI/RSI	I	Test data in for JTAG/RAM init. serial data in	Hold HIGH during normal operation. Connect to VCCIO(B) if unused.
TRSTB	I	Active low reset for JTAG	Hold LOW during normal operation. Connect to GND if unused. During JTAG, a high voltage is based on VCCIO(B).
TMS	I	Test mode select for JTAG	Hold HIGH during normal operation. Connect to VCCIO(B) if not used for JTAG.
TCK	I	Test clock for JTAG	Hold HIGH or LOW during normal operation. Connect to VCCIO(B) or GND if not used for JTAG.
TDO	O	Test data out for JTAG	Must be left unconnected if not used for JTAG. The output voltage drive is specified by VCCIO(B).

Recommended Unused Pin Terminations for PolarPro Devices

All unused, general purpose I/O pins can be tied to VCCIO, GND, or Hi-Z (high impedance) internally. By default, QuickLogic QuickWorks software ties unused I/Os to GND.

Terminate the rest of the pins at the board level as recommended in **Table 55**.

Table 55: Recommended Unused Pin Terminations

Signal Name	Recommended Termination
VREF	If an I/O bank does not require the use of the INREF signal, connect the pin to GND.
CLK <x>[a]	Connect to GND or VCCIO(x) if unused.
VLP	Tie VLP to 3.3 V to disable low power mode.
CCMVCC(1:0)	If a CCM is not used, the corresponding CCMVCC may be tied to GND to reduce power consumption. If a CCM is used, do not try to disable the CCM by tying the CCMVCC to GND.
TDI	Connect to VCCIO(B) if not used for JTAG.
TRSTB	Connect to GND if not used for JTAG.
TMS	Connect to VCCIO(B) if not used for JTAG
TCK	Connect to VCCIO(B) or GND if not used for JTAG.
TDO	Must be left unconnected if not used for JTAG.

a. x represents A, B, C or D.

Packaging Pinout Tables

PolarPro QL1P075 - 132 TFBGA Pinout Table

Table 56: QL1P075 – 132 TFBGA Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	VCC	D7	DQ/GPIO(D)	H1	CLK(C)	L9	GPIO(B)
A2	VCCIO(D)	D8	DQ/GPIO(D)	H3	TCK	L10	GPIO(B)
A3	DQS/GPIO(D)	D9	DQ/GPIO(D)	H4	GPIO(C)	L11	GPIO(A)
A4	DQCK_P/GPIO(D)	D10	DQ/GPIO(D)	H6	GND	L12	GPIO(A)
A5	DQCK_N/GPIO(D)	D11	GPIO(A)	H7	GND	L14	GPIO(A)
A6	DQ/GPIO(D)	D12	GPIO(A)	H8	GND	M1	VCC
A7	DEDCLK(D)	D14	VCCIO(A)	H9	GND	M3	GPIO(B)
A8	DQ/GPIO(D)	E1	VCCIO(C)	H11	GPIO(A)	M4	GPIO(B)
A9	DQS/GPIO(D)	E3	GPIO(C)	H12	GPIO(A)	M5	GPIO(B)
A10	DQCK_P/GPIO(D)	E4	DQ/GPIO(D)	H14	VCC	M6	GPIO(B)
A11	DQCK_N/GPIO(D)	E11	GPIO(A)	J1	GPIO(C)	M7	GPIO(B)
A12	VCCIO(D)	E12	GPIO(A)	J3	GPIO(C)	M8	VCC
A13	GND	E14	GPIO(A)	J4	GPIO(C)	M9	GPIO(B)
A14	VCC	F1	VCC	J6	GPIO(C)	M10	GPIO(B)
B1	VREF	F3	GPIO(C)	J7	GPIO(B)	M11	GPIO(B)
B14	CCMGND(1)	F4	GND	J8	GND	M12	GPIO(A)
C1	GPIO(C)	F6	TMS	J9	GPIO(A)	M14	VCCIO(A)
C3	GPIO(C)	F7	GND	J11	GPIO(A)	N1	GND
C4	DQ/GPIO(D)	F8	GND	J12	GPIO(A)	N14	VCC
C5	DQ/GPIO(D)	F9	GPIO(A)	J14	CLK(A)/CCMIN(1)	P1	VCCIO(B)
C6	VCC	F11	GPIO(A)	K1	VCCIO(C)	P2	GPIO(B)
C7	DQ/GPIO(D)	F12	GPIO(A)	K3	GPIO(C)	P3	TDO
C8	VCCIO(D)	F14	VCCIO(A)	K4	VCCIO(B)	P4	GPIO(B)
C9	DQ/GPIO(D)	G1	VCC	K11	GPIO(A)	P5	VCCIO(B)
C10	DQ/GPIO(D)	G3	GPIO(C)	K12	TRSTB	P6	GPIO(B)
C11	VREF	G4	GPIO(C)	K14	VCCIO(B)	P7	CLK(B)
C12	CCMVCC(1)	G6	GND	L1	GPIO(C)	P8	CLK(B)
C14	GPIO(A)	G7	GND	L3	GPIO(C)	P9	VCC
D1	GPIO(C)	G8	GND	L4	GPIO(C)	P10	VCCIO(B)
D3	GPIO(C)	G9	GND	L5	GPIO(C)	P11	GPIO(B)
D4	VCCIO(D)	G11	GPIO(A)	L6	GPIO(C)	P12	GPIO(B)
D5	DQ/GPIO(D)	G12	GPIO(A)	L7	GPIO(B)	P13	VLP
D6	DQ/GPIO(D)	G14	VCC	L8	TDI	P14	GND

PolarPro QL1P075 - 144 TQFP Pinout Table

Table 57: QL1P075 – 144 TQFP Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	VCCIO(C)	37	GND	73	VCCIO(A)	109	VCCIO(D)
2	GPIO(C)	38	GPIO(B)	74	GPIO(A)	110	VREF(D)
3	GPIO(C)	39	GPIO(B)	75	GPIO(A)	111	DQ/GPIO(D)
4	GPIO(C)	40	TDO	76	GPIO(A)	112	DQ/GPIO(D)
5	GPIO(C)	41	VCCIO(B)	77	GPIO(A)	113	DQ/GPIO(D)
6	GPIO(C)	42	GPIO(B)	78	GPIO(A)	114	DQ/GPIO(D)
7	GPIO(C)	43	GPIO(B)	79	VCCIO(B)	115	DQCK_P/GPIO(D)
8	GPIO(C)	44	GPIO(B)	80	GPIO(A)	116	DQCK_N/GPIO(D)
9	GPIO(C)	45	GPIO(B)	81	TRSTB	117	DQS/GPIO(D)
10	GPIO(C)	46	GPIO(B)	82	GPIO(A)	118	DQ/GPIO(D)
11	GPIO(C)	47	GPIO(B)	83	GPIO(A)	119	DQ/GPIO(D)
12	GPIO(C)	48	GPIO(B)	84	CLK(A)/CCMIN(1)	120	DQ/GPIO(D)
13	VCC	49	GPIO(B)	85	GPIO(A)	121	TMS
14	GPIO(C)	50	GPIO(B)	86	VCCIO(A)	122	DQ/GPIO(D)
15	GPIO(C)	51	GPIO(B)	87	GPIO(A)	123	DQ/GPIO(D)
16	VCC	52	TDI	88	GPIO(A)	124	VCC
17	GPIO(C)	53	CLK(B)	89	GPIO(A)	125	DEDCLK(D)
18	GPIO(C)	54	VCCIO(B)	90	VCC	126	VCCIO(D)
19	VCCIO(C)	55	VCC	91	GPIO(A)	127	DQ/GPIO(D)
20	GPIO(C)	56	CLK(B)	92	GPIO(A)	128	DQ/GPIO(D)
21	GPIO(C)	57	GPIO(B)	93	VCC	129	DQ/GPIO(D)
22	GPIO(C)	58	VCC	94	GPIO(A)	130	DQ/GPIO(D)
23	CLK(C)	59	GPIO(B)	95	GPIO(A)	131	DQCK_N/GPIO(D)
24	TCK	60	GPIO(B)	96	GPIO(A)	132	DQCK_P/GPIO(D)
25	GPIO(C)	61	GPIO(B)	97	GPIO(A)	133	DQS/GPIO(D)
26	GPIO(C)	62	GPIO(B)	98	GPIO(A)	134	DQ/GPIO(D)
27	VCCIO(B)	63	GPIO(B)	99	GPIO(A)	135	DQ/GPIO(D)
28	GPIO(C)	64	GPIO(B)	100	GPIO(A)	136	DQ/GPIO(D)
29	GPIO(C)	65	GPIO(B)	101	GPIO(A)	137	DQ/GPIO(D)
30	GPIO(C)	66	GPIO(B)	102	GPIO(A)	138	VREF(D)
31	GPIO(C)	67	GPIO(B)	103	GPIO(A)	139	DQ/GPIO(D)
32	GPIO(C)	68	GPIO(B)	104	CCMVCC(1)	140	VCCIO(D)
33	GPIO(C)	69	VCCIO(B)	105	VCCIO(A)	141	VCC
34	VCCIO(C)	70	VLP	106	CCMGND(1)	142	VCCIO(D)
35	GND	71	GND	107	GND	143	GND
36	GND	72	GND	108	GND	144	GND

PolarPro QL1P075 - 196 TFBGA (12 mm x 12 mm) Pinout Table

Table 58: QL1P075 – 196 TFBGA (12 mm x 12 mm) Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	DQS/GPIO(D)	C13	DQ/GPIO(D)	F11	GPIO(A)	J9	GND	M7	GPIO(B)
A2	DQCK_P/GPIO(D)	C14	DQ/GPIO(D)	F12	GPIO(A)	J10	VCC	M8	GPIO(B)
A3	DQCK_N/GPIO(D)	D1	GPIO(C)	F13	GPIO(A)	J11	VCCIO(B)	M9	GPIO(B)
A4	DQ/GPIO(D)	D2	GND	F14	GPIO(A)	J12	GPIO(A)	M10	GPIO(B)
A5	DQ/GPIO(D)	D3	DQ/GPIO(D)	G1	GPIO(C)	J13	GPIO(A)	M11	GPIO(B)
A6	DQCK_P/GPIO(D)	D4	DQ/GPIO(D)	G2	GPIO(C)	J14	GPIO(A)	M12	GPIO(A)
A7	DQCK_N/GPIO(D)	D5	DQ/GPIO(D)	G3	GPIO(C)	K1	GPIO(C)	M13	GPIO(A)
A8	DQ/GPIO(D)	D6	DQ/GPIO(D)	G4	TCK	K2	GPIO(C)	M14	GPIO(A)
A9	DQCK_P/GPIO(D)	D7	DQ/GPIO(D)	G5	VCC	K3	GPIO(C)	N1	GPIO(C)
A10	DQCK_N/GPIO(D)	D8	DQ/GPIO(D)	G6	GND	K4	GND	N2	GPIO(C)
A11	DQ/GPIO(D)	D9	DQ/GPIO(D)	G7	GND	K5	VCCIO(B)	N3	GPIO(B)
A12	DQ/GPIO(D)	D10	DQ/GPIO(D)	G8	GND	K6	VCCIO(B)	N4	GPIO(B)
A13	DQCK_P/GPIO(D)	D11	DQS/GPIO(D)	G9	GND	K7	VCC	N5	GPIO(B)
A14	DQCK_N/GPIO(D)	D12	DQ/GPIO(D)	G10	VCC	K8	VCCIO(B)	N6	GPIO(B)
B1	DQ/GPIO(D)	D13	DQ/GPIO(D)	G11	GPIO(A)	K9	VCCIO(B)	N7	CLK(B)
B2	DQ/GPIO(D)	D14	GND	G12	GPIO(A)	K10	VCCIO(A)	N8	GPIO(B)
B3	DQ/GPIO(D)	E1	GPIO(C)	G13	GPIO(A)	K11	GPIO(A)	N9	GPIO(B)
B4	VREF(D)	E2	GPIO(C)	G14	GPIO(A)	K12	GPIO(A)	N10	GPIO(B)
B5	DQ/GPIO(D)	E3	GPIO(C)	H1	CLK(C)/CCMIN(0)	K13	GPIO(A)	N11	GPIO(B)
B6	DQ/GPIO(D)	E4	CCMGND(0)	H2	GPIO(C)	K14	GPIO(A)	N12	GPIO(B)
B7	DEDCLK(D)	E5	VCCIO(C)	H3	GPIO(C)	L1	GPIO(C)	N13	VLP
B8	TMS	E6	VCCIO(D)	H4	VCCIO(B)	L2	GPIO(C)	N14	GPIO(A)
B9	VREF(D)	E7	VCCIO(D)	H5	VCC	L3	GPIO(C)	P1	GPIO(C)
B10	DQ/GPIO(D)	E8	VCC	H6	GND	L4	GPIO(B)	P2	GPIO(B)
B11	DQ/GPIO(D)	E9	VCCIO(D)	H7	GND	L5	GPIO(B)	P3	GPIO(B)
B12	DQS/GPIO(D)	E10	VCCIO(D)	H8	GND	L6	GPIO(B)	P4	GPIO(B)
B13	DQ/GPIO(D)	E11	CCMGND(1)	H9	GND	L7	TDO	P5	GPIO(B)
B14	DQ/GPIO(D)	E12	CCMVCC(1)	H10	VCC	L8	TDI	P6	CLK(B)
C1	GPIO(C)	E13	GPIO(A)	H11	GPIO(A)	L9	GPIO(B)	P7	GPIO(B)
C2	DQ/GPIO(D)	E14	GPIO(A)	H12	GPIO(A)	L10	GND	P8	GPIO(B)
C3	DQ/GPIO(D)	F1	GPIO(C)	H13	GPIO(A)	L11	GPIO(A)	P9	GPIO(B)
C4	DQ/GPIO(D)	F2	GPIO(C)	H14	CLK(A)/CCMIN(1)	L12	GPIO(A)	P10	GPIO(B)
C5	DQ/GPIO(D)	F3	GPIO(C)	J1	GPIO(C)	L13	GPIO(A)	P11	GPIO(B)
C6	DQS/GPIO(D)	F4	CCMVCC(0)	J2	GPIO(C)	L14	TRSTB	P12	GPIO(B)
C7	DQ/GPIO(D)	F5	VCC	J3	GPIO(C)	M1	GPIO(C)	P13	GPIO(A)
C8	DQ/GPIO(D)	F6	GND	J4	GND	M2	GPIO(C)	P14	GPIO(A)
C9	DQ/GPIO(D)	F7	GND	J5	VCCIO(C)	M3	GPIO(C)		
C10	DQ/GPIO(D)	F8	GND	J6	GND	M4	GPIO(B)		
C11	DQ/GPIO(D)	F9	GND	J7	GND	M5	GPIO(B)		
C12	DQ/GPIO(D)	F10	VCCIO(A)	J8	GND	M6	GPIO(B)		

PolarPro QL1P075 - 256 LBGA Pinout Table

Table 59: QL1P075 – 256 LBGA Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	GND	C12	DQCK_P/GPIO(D)	F7	VCC	J2	GPIO(C)	L13	NC	P8	GPIO(B)
A2	DQ/GPIO(D)	C13	DQCK_N/GPIO(D)	F8	GND	J3	GPIO(C)	L14	GPIO(A)	P9	GPIO(B)
A3	DQ/GPIO(D)	C14	GND	F9	TMS	J4	GPIO(C)	L15	GPIO(A)	P10	GPIO(B)
A4	DQ/GPIO(D)	C15	DQ/GPIO(D)	F10	VCC	J5	VCCIO(C)	L16	GPIO(A)	P11	GPIO(B)
A5	DQ/GPIO(D)	C16	DQ/GPIO(D)	F11	DQ/GPIO(D)	J6	GND	M1	NC	P12	GPIO(B)
A6	DQ/GPIO(D)	D1	GPIO(C)	F12	CCMVCC(1)	J7	GND	M2	NC	P13	GPIO(B)
A7	DQS/GPIO(D)	D2	NC	F13	GPIO(A)	J8	VCC	M3	GPIO(B)	P14	GND
A8	DQ/GPIO(D)	D3	NC	F14	GPIO(A)	J9	VCC	M4	GPIO(B)	P15	GPIO(B)
A9	DEDCLK(D)	D4	NC	F15	GPIO(A)	J10	GND	M5	GPIO(B)	P16	GPIO(B)
A10	DQ/GPIO(D)	D5	VREF(D)	F16	GPIO(A)	J11	TRSTB	M6	VCCIO(B)	R1	GPIO(B)
A11	DQ/GPIO(D)	D6	DQS/GPIO(D)	G1	GPIO(C)	J12	VCCIO(A)	M7	VCCIO(B)	R2	GPIO(B)
A12	DQ/GPIO(D)	D7	DQ/GPIO(D)	G2	GPIO(C)	J13	GPIO(A)	M8	VCCIO(B)	R3	GPIO(B)
A13	DQ/GPIO(D)	D8	DQ/GPIO(D)	G3	GPIO(C)	J14	GPIO(A)	M9	VCCIO(B)	R4	GPIO(B)
A14	DQ/GPIO(D)	D9	DQS/GPIO(D)	G4	GPIO(C)	J15	GPIO(A)	M10	VCCIO(B)	R5	TDO
A15	NC	D10	DQCK_P/GPIO(D)	G5	GPIO(C)	J16	CLK(A)/CCMIN(1)	M11	VCCIO(B)	R6	GPIO(B)
A16	GND	D11	DQ/GPIO(D)	G6	VCC	K1	GPIO(C)	M12	GPIO(B)	R7	GPIO(B)
B1	DQ/GPIO(D)	D12	VREF(D)	G7	GND	K2	GPIO(C)	M13	NC	R8	GPIO(B)
B2	DQ/GPIO(D)	D13	DQ/GPIO(D)	G8	GND	K3	GPIO(C)	M14	GPIO(A)	R9	GPIO(B)
B3	DQ/GPIO(D)	D14	NC	G9	GND	K4	GPIO(C)	M15	GPIO(A)	R10	GPIO(B)
B4	DQ/GPIO(D)	D15	NC	G10	GND	K5	GPIO(C)	M16	NC	R11	GPIO(B)
B5	DQ/GPIO(D)	D16	NC	G11	VCC	K6	VCC	N1	GPIO(B)	R12	GPIO(B)
B6	DQ/GPIO(D)	E1	GPIO(C)	G12	GPIO(A)	K7	GND	N2	GPIO(B)	R13	GPIO(B)
B7	DQCK_P/GPIO(D)	E2	GPIO(C)	G13	GPIO(A)	K8	GND	N3	GPIO(B)	R14	GPIO(B)
B8	DQCK_N/GPIO(D)	E3	GPIO(C)	G14	GPIO(A)	K9	GND	N4	GPIO(B)	R15	GPIO(B)
B9	DQ/GPIO(D)	E4	GPIO(C)	G15	GPIO(A)	K10	GND	N5	GPIO(B)	R16	GPIO(B)
B10	DQ/GPIO(D)	E5	CCMGND(0)	G16	GPIO(A)	K11	VCC	N6	GPIO(B)	T1	GND
B11	DQ/GPIO(D)	E6	VCCIO(D)	H1	CLK(C)/CCMIN(0)	K12	GPIO(A)	N7	GPIO(B)	T2	GPIO(B)
B12	DQ/GPIO(D)	E7	VCCIO(D)	H2	GPIO(C)	K13	GPIO(A)	N8	GPIO(B)	T3	GPIO(B)
B13	DQ/GPIO(D)	E8	VCCIO(D)	H3	GPIO(C)	K14	GPIO(A)	N9	GPIO(B)	T4	GPIO(B)
B14	DQ/GPIO(D)	E9	VCCIO(D)	H4	GPIO(C)	K15	GPIO(A)	N10	GPIO(B)	T5	GPIO(B)
B15	DQ/GPIO(D)	E10	VCCIO(D)	H5	VCCIO(C)	K16	GPIO(A)	N11	GPIO(B)	T6	GPIO(B)
B16	DQS/GPIO(D)	E11	VCCIO(D)	H6	TCK	L1	GPIO(C)	N12	GPIO(B)	T7	CLK(B)
C1	NC	E12	CCMGND(1)	H7	GND	L2	GPIO(C)	N13	GPIO(B)	T8	GPIO(B)
C2	GPIO(C)	E13	GPIO(A)	H8	VCC	L3	GPIO(C)	N14	GPIO(B)	T9	CLK(B)
C3	GND	E14	GPIO(A)	H9	VCC	L4	NC	N15	NC	T10	GPIO(B)
C4	DQ/GPIO(D)	E15	GPIO(A)	H10	GND	L5	NC	N16	GPIO(B)	T11	GPIO(B)
C5	DQCK_P/GPIO(D)	E16	GPIO(A)	H11	GND	L6	GND	P1	GPIO(B)	T12	GPIO(B)
C6	DQCK_N/GPIO(D)	F1	GPIO(C)	H12	VCCIO(A)	L7	VCC	P2	GPIO(B)	T13	GPIO(B)
C7	DQ/GPIO(D)	F2	GPIO(C)	H13	GPIO(A)	L8	TDI	P3	GND	T14	GPIO(B)
C8	DQ/GPIO(D)	F3	GPIO(C)	H14	GPIO(A)	L9	GND	P4	GPIO(B)	T15	GPIO(B)
C9	DQ/GPIO(D)	F4	GPIO(C)	H15	GPIO(A)	L10	VCC	P5	GPIO(B)	T16	GND
C10	DQCK_N/GPIO(D)	F5	CCMVCC(0)	H16	GPIO(A)	L11	VCCIO(B)	P6	GPIO(B)		
C11	DQ/GPIO(D)	F6	VCCIO(B)	J1	GPIO(C)	L12	VLP	P7	GPIO(B)		

PolarPro QL1P100 - 132 TFBGA Pinout Table

Table 60: QL1P100 – 132 TFBGA Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	VCC	D7	DQ/GPIO(D)	H1	CLK(C)	L9	GPIO(B)
A2	VCCIO(D)	D8	DQ/GPIO(D)	H3	TCK	L10	GPIO(B)
A3	DQS/GPIO(D)	D9	DQ/GPIO(D)	H4	GPIO(C)	L11	GPIO(A)
A4	DQCK_P/GPIO(D)	D10	DQ/GPIO(D)	H6	GND	L12	GPIO(A)
A5	DQCK_N/GPIO(D)	D11	GPIO(A)	H7	GND	L14	GPIO(A)
A6	DQ/GPIO(D)	D12	GPIO(A)	H8	GND	M1	VCC
A7	DEDCLK(D)	D14	VCCIO(A)	H9	GND	M3	GPIO(B
A8	DQ/GPIO(D)	E1	VCCIO(C)	H11	GPIO(A)	M4	GPIO(B)
A9	DQS/GPIO(D)	E3	GPIO(C)	H12	GPIO(A)	M5	GPIO(B)
A10	DQCK_P/GPIO(D)	E4	DQ/GPIO(D)	H14	VCC	M6	GPIO(B)
A11	DQCK_N/GPIO(D)	E11	GPIO(A)	J1	GPIO(C)	M7	GPIO(B)
A12	VCCIO(D)	E12	GPIO(A)	J3	GPIO(C)	M8	VCC
A13	GND	E14	GPIO(A)	J4	GPIO(C)	M9	GPIO(B)
A14	VCC	F1	VCC	J6	GPIO(C)	M10	GPIO(B)
B1	VREF	F3	GPIO(C)	J7	GPIO(B)	M11	GPIO(B)
B14	CCMGND(1)	F4	GND	J8	GND	M12	GPIO(A)
C1	GPIO(C)	F6	TMS	J9	GPIO(A)	M14	VCCIO(A)
C3	GPIO(C)	F7	GND	J11	GPIO(A)	N1	GND
C4	DQ/GPIO(D)	F8	GND	J12	GPIO(A)	N14	VCC
C5	DQ/GPIO(D)	F9	GPIO(A)	J14	CLK(A)/CCMIN(1)	P1	VCCIO(B)
C6	VCC	F11	GPIO(A)	K1	VCCIO(C)	P2	GPIO(B)
C7	DQ/GPIO(D)	F12	GPIO(A)	K3	GPIO(C)	P3	TDO
C8	VCCIO(D)	F14	VCCIO(A)	K4	VCCIO(B)	P4	GPIO(B)
C9	DQ/GPIO(D)	G1	VCC	K11	GPIO(A)	P5	VCCIO(B)
C10	DQ/GPIO(D)	G3	GPIO(C)	K12	TRSTB	P6	GPIO(B)
C11	VREF	G4	GPIO(C)	K14	VCCIO(B)	P7	CLK(B)
C12	CCMVCC(1)	G6	GND	L1	GPIO(C)	P8	CLK(B)
C14	GPIO(A)	G7	GND	L3	GPIO(C)	P9	VCC
D1	GPIO(C)	G8	GND	L4	GPIO(C)	P10	VCCIO(B)
D3	GPIO(C)	G9	GND	L5	GPIO(C)	P11	GPIO(B)
D4	VCCIO(D)	G11	GPIO(A)	L6	GPIO(C)	P12	GPIO(B)
D5	DQ/GPIO(D)	G12	GPIO(A)	L7	GPIO(B)	P13	VLP
D6	DQ/GPIO(D)	G14	VCC	L8	TDI	P14	GND

PolarPro QL1P100 - 144 TQFP Pinout Table

Table 61: QL1P100 – 144 TQFP Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	VCCIO(C)	37	GND	73	VCCIO(A)	109	VCCIO(D)
2	GPIO(C)	38	GPIO(B)	74	GPIO(A)	110	VREF(D)
3	GPIO(C)	39	GPIO(B)	75	GPIO(A)	111	DQ/GPIO(D)
4	GPIO(C)	40	TDO	76	GPIO(A)	112	DQ/GPIO(D)
5	GPIO(C)	41	VCCIO(B)	77	GPIO(A)	113	DQ/GPIO(D)
6	GPIO(C)	42	GPIO(B)	78	GPIO(A)	114	DQ/GPIO(D)
7	GPIO(C)	43	GPIO(B)	79	VCCIO(B)	115	DQCK_P/GPIO(D)
8	GPIO(C)	44	GPIO(B)	80	GPIO(A)	116	DQCK_N/GPIO(D)
9	GPIO(C)	45	GPIO(B)	81	TRSTB	117	DQS/GPIO(D)
10	GPIO(C)	46	GPIO(B)	82	GPIO(A)	118	DQ/GPIO(D)
11	GPIO(C)	47	GPIO(B)	83	GPIO(A)	119	DQ/GPIO(D)
12	GPIO(C)	48	GPIO(B)	84	CLK(A)/CCMIN(1)	120	DQ/GPIO(D)
13	VCC	49	GPIO(B)	85	GPIO(A)	121	TMS
14	GPIO(C)	50	GPIO(B)	86	VCCIO(A)	122	DQ/GPIO(D)
15	GPIO(C)	51	GPIO(B)	87	GPIO(A)	123	DQ/GPIO(D)
16	VCC	52	TDI	88	GPIO(A)	124	VCC
17	GPIO(C)	53	CLK(B)	89	GPIO(A)	125	DEDCLK(D)
18	GPIO(C)	54	VCCIO(B)	90	VCC	126	VCCIO(D)
19	VCCIO(C)	55	VCC	91	GPIO(A)	127	DQ/GPIO(D)
20	GPIO(C)	56	CLK(B)	92	GPIO(A)	128	DQ/GPIO(D)
21	GPIO(C)	57	GPIO(B)	93	VCC	129	DQ/GPIO(D)
22	GPIO(C)	58	VCC	94	GPIO(A)	130	DQ/GPIO(D)
23	CLK(C)	59	GPIO(B)	95	GPIO(A)	131	DQCK_N/GPIO(D)
24	TCK	60	GPIO(B)	96	GPIO(A)	132	DQCK_P/GPIO(D)
25	GPIO(C)	61	GPIO(B)	97	GPIO(A)	133	DQS/GPIO(D)
26	GPIO(C)	62	GPIO(B)	98	GPIO(A)	134	DQ/GPIO(D)
27	VCCIO(B)	63	GPIO(B)	99	GPIO(A)	135	DQ/GPIO(D)
28	GPIO(C)	64	GPIO(B)	100	GPIO(A)	136	DQ/GPIO(D)
29	GPIO(C)	65	GPIO(B)	101	GPIO(A)	137	DQ/GPIO(D)
30	GPIO(C)	66	GPIO(B)	102	GPIO(A)	138	VREF(D)
31	GPIO(C)	67	GPIO(B)	103	GPIO(A)	139	DQ/GPIO(D)
32	GPIO(C)	68	GPIO(B)	104	CCMVCC(1)	140	VCCIO(D)
33	GPIO(C)	69	VCCIO(B)	105	VCCIO(A)	141	VCC
34	VCCIO(C)	70	VLP	106	CCMGND(1)	142	VCCIO(D)
35	GND	71	GND	107	GND	143	GND
36	GND	72	GND	108	GND	144	GND

PolarPro QL1P100 - 196 TFBGA (12 mm x 12 mm) Pinout Table

Table 62: QL1P100 – 196 TFBGA (12 mm x 12 mm) Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	DQS/GPIO(D)	C13	DQ/GPIO(D)	F11	GPIO(A)	J9	GND	M7	GPIO(B)
A2	DQCK_P/GPIO(D)	C14	DQ/GPIO(D)	F12	GPIO(A)	J10	VCC	M8	GPIO(B)
A3	DQCK_N/GPIO(D)	D1	GPIO(C)	F13	GPIO(A)	J11	VCCIO(B)	M9	GPIO(B)
A4	DQ/GPIO(D)	D2	GND	F14	GPIO(A)	J12	GPIO(A)	M10	GPIO(B)
A5	DQ/GPIO(D)	D3	DQ/GPIO(D)	G1	GPIO(C)	J13	GPIO(A)	M11	GPIO(B)
A6	DQCK_P/GPIO(D)	D4	DQ/GPIO(D)	G2	GPIO(C)	J14	GPIO(A)	M12	GPIO(A)
A7	DQCK_N/GPIO(D)	D5	DQ/GPIO(D)	G3	GPIO(C)	K1	GPIO(C)	M13	GPIO(A)
A8	DQ/GPIO(D)	D6	DQ/GPIO(D)	G4	TCK	K2	GPIO(C)	M14	GPIO(A)
A9	DQCK_P/GPIO(D)	D7	DQ/GPIO(D)	G5	VCC	K3	GPIO(C)	N1	GPIO(C)
A10	DQCK_N/GPIO(D)	D8	DQ/GPIO(D)	G6	GND	K4	GND	N2	GPIO(C)
A11	DQ/GPIO(D)	D9	DQ/GPIO(D)	G7	GND	K5	VCCIO(B)	N3	GPIO(B)
A12	DQ/GPIO(D)	D10	DQ/GPIO(D)	G8	GND	K6	VCCIO(B)	N4	GPIO(B)
A13	DQCK_P/GPIO(D)	D11	DQS/GPIO(D)	G9	GND	K7	VCC	N5	GPIO(B)
A14	DQCK_N/GPIO(D)	D12	DQ/GPIO(D)	G10	VCC	K8	VCCIO(B)	N6	GPIO(B)
B1	DQ/GPIO(D)	D13	DQ/GPIO(D)	G11	GPIO(A)	K9	VCCIO(B)	N7	CLK(B)
B2	DQ/GPIO(D)	D14	GND	G12	GPIO(A)	K10	VCCIO(A)	N8	GPIO(B)
B3	DQ/GPIO(D)	E1	GPIO(C)	G13	GPIO(A)	K11	GPIO(A)	N9	GPIO(B)
B4	VREF(D)	E2	GPIO(C)	G14	GPIO(A)	K12	GPIO(A)	N10	GPIO(B)
B5	DQ/GPIO(D)	E3	GPIO(C)	H1	CLK(C)/CCMIN(0)	K13	GPIO(A)	N11	GPIO(B)
B6	DQ/GPIO(D)	E4	CCMGND(0)	H2	GPIO(C)	K14	GPIO(A)	N12	GPIO(B)
B7	DEDCLK(D)	E5	VCCIO(C)	H3	GPIO(C)	L1	GPIO(C)	N13	VLP
B8	TMS	E6	VCCIO(D)	H4	VCCIO(B)	L2	GPIO(C)	N14	GPIO(A)
B9	VREF(D)	E7	VCCIO(D)	H5	VCC	L3	GPIO(C)	P1	GPIO(C)
B10	DQ/GPIO(D)	E8	VCC	H6	GND	L4	GPIO(B)	P2	GPIO(B)
B11	DQ/GPIO(D)	E9	VCCIO(D)	H7	GND	L5	GPIO(B)	P3	GPIO(B)
B12	DQS/GPIO(D)	E10	VCCIO(D)	H8	GND	L6	GPIO(B)	P4	GPIO(B)
B13	DQ/GPIO(D)	E11	CCMGND(1)	H9	GND	L7	TDO	P5	GPIO(B)
B14	DQ/GPIO(D)	E12	CCMVCC(1)	H10	VCC	L8	TDI	P6	CLK(B)
C1	GPIO(C)	E13	GPIO(A)	H11	GPIO(A)	L9	GPIO(B)	P7	GPIO(B)
C2	DQ/GPIO(D)	E14	GPIO(A)	H12	GPIO(A)	L10	GND	P8	GPIO(B)
C3	DQ/GPIO(D)	F1	GPIO(C)	H13	GPIO(A)	L11	GPIO(A)	P9	GPIO(B)
C4	DQ/GPIO(D)	F2	GPIO(C)	H14	CLK(A)/CCMIN(1)	L12	GPIO(A)	P10	GPIO(B)
C5	DQ/GPIO(D)	F3	GPIO(C)	J1	GPIO(C)	L13	GPIO(A)	P11	GPIO(B)
C6	DQS/GPIO(D)	F4	CCMVCC(0)	J2	GPIO(C)	L14	TRSTB	P12	GPIO(B)
C7	DQ/GPIO(D)	F5	VCC	J3	GPIO(C)	M1	GPIO(C)	P13	GPIO(A)
C8	DQ/GPIO(D)	F6	GND	J4	GND	M2	GPIO(C)	P14	GPIO(A)
C9	DQ/GPIO(D)	F7	GND	J5	VCCIO(C)	M3	GPIO(C)		
C10	DQ/GPIO(D)	F8	GND	J6	GND	M4	GPIO(B)		
C11	DQ/GPIO(D)	F9	GND	J7	GND	M5	GPIO(B)		
C12	DQ/GPIO(D)	F10	VCCIO(A)	J8	GND	M6	GPIO(B)		

PolarPro QL1P100 - 256 LBGA Pinout Table

Table 63: QL1P100 – 256 LBGA Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	GND	C12	DQCK_P/GPIO(D)	F7	VCC	J2	GPIO(C)	L13	GPIO(A)	P8	GPIO(B)
A2	DQ/GPIO(D)	C13	DQCK_N/GPIO(D)	F8	GND	J3	GPIO(C)	L14	GPIO(A)	P9	GPIO(B)
A3	DQ/GPIO(D)	C14	GND	F9	TMS	J4	GPIO(C)	L15	GPIO(A)	P10	GPIO(B)
A4	DQ/GPIO(D)	C15	DQ/GPIO(D)	F10	VCC	J5	VCCIO(C)	L16	GPIO(A)	P11	GPIO(B)
A5	DQ/GPIO(D)	C16	DQ/GPIO(D)	F11	DQ/GPIO(D)	J6	GND	M1	GPIO(C)	P12	GPIO(B)
A6	DQ/GPIO(D)	D1	GPIO(C)	F12	CCMVCC(1)	J7	GND	M2	GPIO(C)	P13	GPIO(B)
A7	DQS/GPIO(D)	D2	GPIO(C)	F13	GPIO(A)	J8	VCC	M3	GPIO(B)	P14	GND
A8	DQ/GPIO(D)	D3	GPIO(C)	F14	GPIO(A)	J9	VCC	M4	GPIO(B)	P15	GPIO(B)
A9	DEDCLK(D)	D4	GPIO(C)	F15	GPIO(A)	J10	GND	M5	GPIO(B)	P16	GPIO(B)
A10	DQ/GPIO(D)	D5	VREF(D)	F16	GPIO(A)	J11	TRSTB	M6	VCCIO(B)	R1	GPIO(B)
A11	DQ/GPIO(D)	D6	DQS/GPIO(D)	G1	GPIO(C)	J12	VCCIO(A)	M7	VCCIO(B)	R2	GPIO(B)
A12	DQ/GPIO(D)	D7	DQ/GPIO(D)	G2	GPIO(C)	J13	GPIO(A)	M8	VCCIO(B)	R3	GPIO(B)
A13	DQ/GPIO(D)	D8	DQ/GPIO(D)	G3	GPIO(C)	J14	GPIO(A)	M9	VCCIO(B)	R4	GPIO(B)
A14	DQ/GPIO(D)	D9	DQS/GPIO(D)	G4	GPIO(C)	J15	GPIO(A)	M10	VCCIO(B)	R5	TDO
A15	GPIO(A)	D10	DQCK_P/GPIO(D)	G5	GPIO(C)	J16	CLK(A) CCMIN(1)	M11	VCCIO(B)	R6	GPIO(B)
A16	GND	D11	DQ/GPIO(D)	G6	VCC	K1	GPIO(C)	M12	GPIO(B)	R7	GPIO(B)
B1	DQ/GPIO(D)	D12	VREF(D)	G7	GND	K2	GPIO(C)	M13	GPIO(A)	R8	GPIO(B)
B2	DQ/GPIO(D)	D13	DQ/GPIO(D)	G8	GND	K3	GPIO(C)	M14	GPIO(A)	R9	GPIO(B)
B3	DQ/GPIO(D)	D14	GPIO(A)	G9	GND	K4	GPIO(C)	M15	GPIO(A)	R10	GPIO(B)
B4	DQ/GPIO(D)	D15	GPIO(A)	G10	GND	K5	GPIO(C)	M16	GPIO(A)	R11	GPIO(B)
B5	DQ/GPIO(D)	D16	GPIO(A)	G11	VCC	K6	VCC	N1	GPIO(B)	R12	GPIO(B)
B6	DQ/GPIO(D)	E1	GPIO(C)	G12	GPIO(A)	K7	GND	N2	GPIO(B)	R13	GPIO(B)
B7	DQCK_P/GPIO(D)	E2	GPIO(C)	G13	GPIO(A)	K8	GND	N3	GPIO(B)	R14	GPIO(B)
B8	DQCK_N/GPIO(D)	E3	GPIO(C)	G14	GPIO(A)	K9	GND	N4	GPIO(B)	R15	GPIO(B)
B9	DQ/GPIO(D)	E4	GPIO(C)	G15	GPIO(A)	K10	GND	N5	GPIO(B)	R16	GPIO(B)
B10	DQ/GPIO(D)	E5	CCMGND(0)	G16	GPIO(A)	K11	VCC	N6	GPIO(B)	T1	GND
B11	DQ/GPIO(D)	E6	VCCIO(D)	H1	CLK(C)/ CCMIN(0)	K12	GPIO(A)	N7	GPIO(B)	T2	GPIO(B)
B12	DQ/GPIO(D)	E7	VCCIO(D)	H2	GPIO(C)	K13	GPIO(A)	N8	GPIO(B)	T3	GPIO(B)
B13	DQ/GPIO(D)	E8	VCCIO(D)	H3	GPIO(C)	K14	GPIO(A)	N9	GPIO(B)	T4	GPIO(B)
B14	DQ/GPIO(D)	E9	VCCIO(D)	H4	GPIO(C)	K15	GPIO(A)	N10	GPIO(B)	T5	GPIO(B)
B15	DQ/GPIO(D)	E10	VCCIO(D)	H5	VCCIO(C)	K16	GPIO(A)	N11	GPIO(B)	T6	GPIO(B)
B16	DQS/GPIO(D)	E11	VCCIO(D)	H6	TCK	L1	GPIO(C)	N12	GPIO(B)	T7	CLK(B)
C1	GPIO(C)	E12	CCMGND(1)	H7	GND	L2	GPIO(C)	N13	GPIO(B)	T8	GPIO(B)
C2	GPIO(C)	E13	GPIO(A)	H8	VCC	L3	GPIO(C)	N14	GPIO(B)	T9	CLK(B)
C3	GND	E14	GPIO(A)	H9	VCC	L4	GPIO(C)	N15	GPIO(A)	T10	GPIO(B)
C4	DQ/GPIO(D)	E15	GPIO(A)	H10	GND	L5	GPIO(C)	N16	GPIO(B)	T11	GPIO(B)
C5	DQCK_P/GPIO(D)	E16	GPIO(A)	H11	GND	L6	GND	P1	GPIO(B)	T12	GPIO(B)
C6	DQCK_N/GPIO(D)	F1	GPIO(C)	H12	VCCIO(A)	L7	VCC	P2	GPIO(B)	T13	GPIO(B)
C7	DQ/GPIO(D)	F2	GPIO(C)	H13	GPIO(A)	L8	TDI	P3	GND	T14	GPIO(B)
C8	DQ/GPIO(D)	F3	GPIO(C)	H14	GPIO(A)	L9	GND	P4	GPIO(B)	T15	GPIO(B)
C9	DQ/GPIO(D)	F4	GPIO(C)	H15	GPIO(A)	L10	VCC	P5	GPIO(B)	T16	GND
C10	DQCK_N/GPIO(D)	F5	CCMVCC(0)	H16	GPIO(A)	L11	VCCIO(B)	P6	GPIO(B)		
C11	DQ/GPIO(D)	F6	VCCIO(B)	J1	GPIO(C)	L12	VLP	P7	GPIO(B)		

PolarPro QL1P200 - 132 TFBGA Pinout Table

Table 64: PolarPro QL1P200 – 132 TFBGA

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	VCC	D7	DQ/GPIO(D)	H1	CLK(C)/CCMIN(0)	L9	GPIO(B)
A2	VCC	D8	DQ/GPIO(D)	H3	VCCIO(C)	L10	GPIO(B)
A3	VREF	D9	DQ/GPIO(D)	H4	GPIO(C)	L11	GPIO(A)
A4	DQS/GPIO(D)	D10	VCCIO(D)	H6	GND	L12	GPIO(A)
A5	DQCK_P/GPIO(D)	D11	GPIO(A)	H7	GND	L14	GPIO(A)
A6	DQCK_N/GPIO(D)	D12	VCCIO(A)	H8	GND	M1	VCC
A7	DEDCLK(D)	D14	GPIO(A)	H9	GND	M3	GND
A8	VCCIO(D)	E1	VCCIO(C)	H11	GPIO(A)	M4	GPIO(B)
A9	DQS/GPIO(D)	E3	GPIO(C)	H12	GPIO(A)	M5	GPIO(B)
A10	DQCK_N/GPIO(D)	E4	GPIO(C)	H14	CLK(A)/CCMIN(1)	M6	GPIO(B)
A11	DQCK_P/GPIO(D)	E11	GPIO(A)	J1	GPIO(C)	M7	GPIO(B)
A12	DQ/GPIO(D)	E12	GPIO(A)	J3	TCK	M8	GPIO(B)
A13	VREF	E14	VCCIO(A)	J4	VCCIO(B)	M9	GPIO(B)
A14	VCC	F1	GPIO(C)	J6	GPIO(C)	M10	VCCIO(B)
B1	CCMVCC(0)	F3	GPIO(C)	J7	TDI	M11	GPIO(B)
B14	CCMVCC(1)	F4	GPIO(C)	J8	GND	M12	GPIO(A)
C1	CCMGND(0)	F6	VCCIO(D)	J9	GPIO(A)	M14	VCCIO(A)
C3	GND	F7	TMS	J11	GPIO(A)	N1	GND
C4	DQ/GPIO(D)	F8	GND	J12	VCCIO(A)	N14	VLP
C5	VCC	F9	DQ/GPIO(D)	J14	VCCIO(B)	P1	VCC
C6	DQ/GPIO(D)	F11	GPIO(A)	K1	VCCIO(C)	P2	TDO
C7	DQ/GPIO(D)	F12	GPIO(A)	K3	GPIO(C)	P3	GPIO(B)
C8	DQ/GPIO(D)	F14	GPIO(A)	K4	GPIO(C)	P4	VCCIO(B)
C9	DQ/GPIO(D)	G1	GPIO(C)	K11	TRSTB	P5	GPIO(B)
C10	DQ/GPIO(D)	G3	GPIO(C)	K12	GPIO(A)	P6	CLK(B)
C11	GND	G4	GPIO(C)	K14	GPIO(A)	P7	CLK(B)
C12	CCMGND(1)	G6	GND	L1	VCC	P8	VCCIO(B)
C14	VCC	G7	GND	L3	GPIO(C)	P9	GPIO(B)
D1	GPIO(C)	G8	GND	L4	GPIO(C)	P10	VCC
D3	GPIO(C)	G9	GND	L5	GPIO(B)	P11	VCC
D4	DQ/GPIO(D)	G11	GPIO(A)	L6	GPIO(B)	P12	GPIO(A)
D5	DQ/GPIO(D)	G12	GPIO(A)	L7	GPIO(B)	P13	GND
D6	DQ/GPIO(D)	G14	GPIO(A)	L8	GPIO(B)	P14	VCC

PolarPro QL1P200 - 256 LBGA Pinout Table

Table 65: PolarPro QL1P200 - 256 LBGA

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	GND	C12	DQCK_N/GPIO(D)	F7	VCC	J2	GPIO(C)	L13	GPIO(A)	P8	GPIO(B)
A2	DQ/GPIO(D)	C13	DQCK_P/GPIO(D)	F8	GND	J3	GPIO(C)	L14	GPIO(A)	P9	GPIO(B)
A3	DQ/GPIO(D)	C14	GND	F9	TMS	J4	GPIO(C)	L15	GPIO(A)	P10	GPIO(B)
A4	DQ/GPIO(D)	C15	DQ/GPIO(D)	F10	VCC	J5	VCCIO(C)	L16	GPIO(A)	P11	GPIO(B)
A5	DQ/GPIO(D)	C16	DQ/GPIO(D)	F11	DQ/GPIO(D)	J6	GND	M1	GPIO(C)	P12	GPIO(B)
A6	DQ/GPIO(D)	D1	GPIO(C)	F12	CCMVCC(1)	J7	GND	M2	GPIO(C)	P13	GPIO(B)
A7	DQS/GPIO(D)	D2	GPIO(C)	F13	GPIO(A)	J8	VCC	M3	GPIO(B)	P14	GND
A8	DQ/GPIO(D)	D3	GPIO(C)	F14	GPIO(A)	J9	VCC	M4	GPIO(B)	P15	GPIO(B)
A9	DEDCLK(D)	D4	GPIO(C)	F15	GPIO(A)	J10	GND	M5	GPIO(B)	P16	GPIO(B)
A10	DQ/GPIO(D)	D5	VREF(D)	F16	GPIO(A)	J11	TRSTB	M6	VCCIO(B)	R1	GPIO(B)
A11	DQ/GPIO(D)	D6	DQS/GPIO(D)	G1	GPIO(C)	J12	VCCIO(A)	M7	VCCIO(B)	R2	GPIO(B)
A12	DQ/GPIO(D)	D7	DQ/GPIO(D)	G2	GPIO(C)	J13	GPIO(A)	M8	VCCIO(B)	R3	GPIO(B)
A13	DQ/GPIO(D)	D8	DQ/GPIO(D)	G3	GPIO(C)	J14	GPIO(A)	M9	VCCIO(B)	R4	GPIO(B)
A14	DQ/GPIO(D)	D9	DQS/GPIO(D)	G4	GPIO(C)	J15	GPIO(A)	M10	VCCIO(B)	R5	TDO
A15	GPIO(A)	D10	DQCK_P/GPIO(D)	G5	GPIO(C)	J16	CLK(A)/CCMIN(1)	M11	VCCIO(B)	R6	GPIO(B)
A16	GND	D11	DQ/GPIO(D)	G6	VCC	K1	GPIO(C)	M12	GPIO(B)	R7	GPIO(B)
B1	DQ/GPIO(D)	D12	VREF(D)	G7	GND	K2	GPIO(C)	M13	GPIO(A)	R8	GPIO(B)
B2	DQ/GPIO(D)	D13	DQ/GPIO(D)	G8	GND	K3	GPIO(C)	M14	GPIO(A)	R9	GPIO(B)
B3	DQ/GPIO(D)	D14	GPIO(A)	G9	GND	K4	GPIO(C)	M15	GPIO(A)	R10	GPIO(B)
B4	DQ/GPIO(D)	D15	GPIO(A)	G10	GND	K5	GPIO(C)	M16	GPIO(A)	R11	GPIO(B)
B5	DQ/GPIO(D)	D16	GPIO(A)	G11	VCC	K6	VCC	N1	GPIO(B)	R12	GPIO(B)
B6	DQ/GPIO(D)	E1	GPIO(C)	G12	GPIO(A)	K7	GND	N2	GPIO(B)	R13	GPIO(B)
B7	DQCK_N/GPIO(D)	E2	GPIO(C)	G13	GPIO(A)	K8	GND	N3	GPIO(B)	R14	GPIO(B)
B8	DQCK_P/GPIO(D)	E3	GPIO(C)	G14	GPIO(A)	K9	GND	N4	GPIO(B)	R15	GPIO(B)
B9	DQ/GPIO(D)	E4	GPIO(C)	G15	GPIO(A)	K10	GND	N5	GPIO(B)	R16	GPIO(B)
B10	DQ/GPIO(D)	E5	CCMGND(0)	G16	GPIO(A)	K11	VCC	N6	GPIO(B)	T1	GND
B11	DQ/GPIO(D)	E6	VCCIO(D)	H1	CLK(C)/CCMIN(0)	K12	GPIO(A)	N7	GPIO(B)	T2	GPIO(B)
B12	DQ/GPIO(D)	E7	VCCIO(D)	H2	GPIO(C)	K13	GPIO(A)	N8	GPIO(B)	T3	GPIO(B)
B13	DQ/GPIO(D)	E8	VCCIO(D)	H3	GPIO(C)	K14	GPIO(A)	N9	GPIO(B)	T4	GPIO(B)
B14	DQ/GPIO(D)	E9	VCCIO(D)	H4	GPIO(C)	K15	GPIO(A)	N10	GPIO(B)	T5	GPIO(B)
B15	DQ/GPIO(D)	E10	VCCIO(D)	H5	VCCIO(C)	K16	GPIO(A)	N11	GPIO(B)	T6	GPIO(B)
B16	DQS/GPIO(D)	E11	VCCIO(D)	H6	TCK	L1	GPIO(C)	N12	GPIO(B)	T7	CLK(B)
C1	GPIO(C)	E12	CCMGND(1)	H7	GND	L2	GPIO(C)	N13	GPIO(B)	T8	GPIO(B)
C2	GPIO(C)	E13	GPIO(A)	H8	VCC	L3	GPIO(C)	N14	GPIO(B)	T9	CLK(B)
C3	GND	E14	GPIO(A)	H9	VCC	L4	GPIO(C)	N15	GPIO(A)	T10	GPIO(B)
C4	DQ/GPIO(D)	E15	GPIO(A)	H10	GND	L5	GPIO(C)	N16	GPIO(B)	T11	GPIO(B)
C5	DQCK_N/GPIO(D)	E16	GPIO(A)	H11	GND	L6	GND	P1	GPIO(B)	T12	GPIO(B)
C6	DQCK_P/GPIO(D)	F1	GPIO(C)	H12	VCCIO(A)	L7	VCC	P2	GPIO(B)	T13	GPIO(B)
C7	DQ/GPIO(D)	F2	GPIO(C)	H13	GPIO(A)	L8	TDI	P3	GND	T14	GPIO(B)
C8	DQ/GPIO(D)	F3	GPIO(C)	H14	GPIO(A)	L9	GND	P4	GPIO(B)	T15	GPIO(B)
C9	DQ/GPIO(D)	F4	GPIO(C)	H15	GPIO(A)	L10	VCC	P5	GPIO(B)	T16	GND
C10	DQCK_N/GPIO(D)	F5	CCMVCC(0)	H16	GPIO(A)	L11	VCCIO(B)	P6	GPIO(B)		
C11	DQ/GPIO(D)	F6	VCCIO(B)	J1	GPIO(C)	L12	VLP	P7	GPIO(B)		

PolarPro QL1P300 - 132 TFBGA Pinout Table

Table 66: PolarPro QL1P300 - 132 TFBGA

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	VCC	D7	DQ/GPIO(D)	H1	CLK(C)/CCMIN(0)	L9	GPIO(B)
A2	VCC	D8	DQ/GPIO(D)	H3	VCCIO(C)	L10	GPIO(B)
A3	VREF	D9	DQ/GPIO(D)	H4	GPIO(C)	L11	GPIO(A)
A4	DQS/GPIO(D)	D10	VCCIO(D)	H6	GND	L12	GPIO(A)
A5	DQCK_P/GPIO(D)	D11	GPIO(A)	H7	GND	L14	GPIO(A)
A6	DQCK_N/GPIO(D)	D12	VCCIO(A)	H8	GND	M1	VCC
A7	DEDCLK(D)	D14	GPIO(A)	H9	GND	M3	GND
A8	VCCIO(D)	E1	VCCIO(C)	H11	GPIO(A)	M4	GPIO(B)
A9	DQS/GPIO(D)	E3	GPIO(C)	H12	GPIO(A)	M5	GPIO(B)
A10	DQCK_N/GPIO(D)	E4	GPIO(C)	H14	CLK(A)/CCMIN(1)	M6	GPIO(B)
A11	DQCK_P/GPIO(D)	E11	GPIO(A)	J1	GPIO(C)	M7	GPIO(B)
A12	DQ/GPIO(D)	E12	GPIO(A)	J3	TCK	M8	GPIO(B)
A13	VREF	E14	VCCIO(A)	J4	VCCIO(B)	M9	GPIO(B)
A14	VCC	F1	GPIO(C)	J6	GPIO(C)	M10	VCCIO(B)
B1	CCMVCC(0)	F3	GPIO(C)	J7	TDI	M11	GPIO(B)
B14	CCMVCC(1)	F4	GPIO(C)	J8	GND	M12	GPIO(A)
C1	CCMGND(0)	F6	VCCIO(D)	J9	GPIO(A)	M14	VCCIO(A)
C3	GND	F7	TMS	J11	GPIO(A)	N1	GND
C4	DQ/GPIO(D)	F8	GND	J12	VCCIO(A)	N14	VLP
C5	VCC	F9	DQ/GPIO(D)	J14	VCCIO(B)	P1	VCC
C6	DQ/GPIO(D)	F11	GPIO(A)	K1	VCCIO(C)	P2	TDO
C7	DQ/GPIO(D)	F12	GPIO(A)	K3	GPIO(C)	P3	GPIO(B)
C8	DQ/GPIO(D)	F14	GPIO(A)	K4	GPIO(C)	P4	VCCIO(B)
C9	DQ/GPIO(D)	G1	GPIO(C)	K11	TRSTB	P5	GPIO(B)
C10	DQ/GPIO(D)	G3	GPIO(C)	K12	GPIO(A)	P6	CLK(B)
C11	GND	G4	GPIO(C)	K14	GPIO(A)	P7	CLK(B)
C12	CCMGND(1)	G6	GND	L1	VCC	P8	VCCIO(B)
C14	VCC	G7	GND	L3	GPIO(C)	P9	GPIO(B)
D1	GPIO(C)	G8	GND	L4	GPIO(C)	P10	VCC
D3	GPIO(C)	G9	GND	L5	GPIO(B)	P11	VCC
D4	DQ/GPIO(D)	G11	GPIO(A)	L6	GPIO(B)	P12	GPIO(A)
D5	DQ/GPIO(D)	G12	GPIO(A)	L7	GPIO(B)	P13	GND
D6	DQ/GPIO(D)	G14	GPIO(A)	L8	GPIO(B)	P14	VCC

PolarPro QL1P300 - 256 LBGA Pinout Table

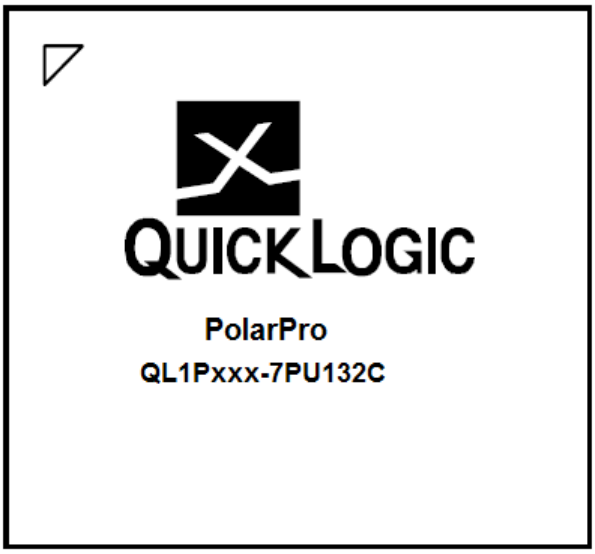
Table 67: QL1P300 – 256 LBGA Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	GND	C12	DQCK_P/GPIO(D)	F7	VCC	J2	GPIO(C)	L13	GPIO(A)	P8	GPIO(B)
A2	DQ/GPIO(D)	C13	DQCK_N/GPIO(D)	F8	GND	J3	GPIO(C)	L14	GPIO(A)	P9	GPIO(B)
A3	DQ/GPIO(D)	C14	GND	F9	TMS	J4	GPIO(C)	L15	GPIO(A)	P10	GPIO(B)
A4	DQ/GPIO(D)	C15	DQ/GPIO(D)	F10	VCC	J5	VCCIO(C)	L16	GPIO(A)	P11	GPIO(B)
A5	DQ/GPIO(D)	C16	DQ/GPIO(D)	F11	DQ/GPIO(D)	J6	GND	M1	GPIO(C)	P12	GPIO(B)
A6	DQ/GPIO(D)	D1	GPIO(C)	F12	CCMVCC(1)	J7	GND	M2	GPIO(C)	P13	GPIO(B)
A7	DQS/GPIO(D)	D2	GPIO(C)	F13	GPIO(A)	J8	VCC	M3	GPIO(B)	P14	GND
A8	DQ/GPIO(D)	D3	GPIO(C)	F14	GPIO(A)	J9	VCC	M4	GPIO(B)	P15	GPIO(B)
A9	DEDCLK(D)	D4	GPIO(C)	F15	GPIO(A)	J10	GND	M5	GPIO(B)	P16	GPIO(B)
A10	DQ/GPIO(D)	D5	VREF(D)	F16	GPIO(A)	J11	TRSTB	M6	VCCIO(B)	R1	GPIO(B)
A11	DQ/GPIO(D)	D6	DQS/GPIO(D)	G1	GPIO(C)	J12	VCCIO(A)	M7	VCCIO(B)	R2	GPIO(B)
A12	DQ/GPIO(D)	D7	DQ/GPIO(D)	G2	GPIO(C)	J13	GPIO(A)	M8	VCCIO(B)	R3	GPIO(B)
A13	DQ/GPIO(D)	D8	DQ/GPIO(D)	G3	GPIO(C)	J14	GPIO(A)	M9	VCCIO(B)	R4	GPIO(B)
A14	DQ/GPIO(D)	D9	DQS/GPIO(D)	G4	GPIO(C)	J15	GPIO(A)	M10	VCCIO(B)	R5	TDO
A15	GPIO(A)	D10	DQCK_P/GPIO(D)	G5	GPIO(C)	J16	CLK(A) CCMIN(1)	M11	VCCIO(B)	R6	GPIO(B)
A16	GND	D11	DQ/GPIO(D)	G6	VCC	K1	GPIO(C)	M12	GPIO(B)	R7	GPIO(B)
B1	DQ/GPIO(D)	D12	VREF(D)	G7	GND	K2	GPIO(C)	M13	GPIO(A)	R8	GPIO(B)
B2	DQ/GPIO(D)	D13	DQ/GPIO(D)	G8	GND	K3	GPIO(C)	M14	GPIO(A)	R9	GPIO(B)
B3	DQ/GPIO(D)	D14	GPIO(A)	G9	GND	K4	GPIO(C)	M15	GPIO(A)	R10	GPIO(B)
B4	DQ/GPIO(D)	D15	GPIO(A)	G10	GND	K5	GPIO(C)	M16	GPIO(A)	R11	GPIO(B)
B5	DQ/GPIO(D)	D16	GPIO(A)	G11	VCC	K6	VCC	N1	GPIO(B)	R12	GPIO(B)
B6	DQ/GPIO(D)	E1	GPIO(C)	G12	GPIO(A)	K7	GND	N2	GPIO(B)	R13	GPIO(B)
B7	DQCK_P/GPIO(D)	E2	GPIO(C)	G13	GPIO(A)	K8	GND	N3	GPIO(B)	R14	GPIO(B)
B8	DQCK_N/GPIO(D)	E3	GPIO(C)	G14	GPIO(A)	K9	GND	N4	GPIO(B)	R15	GPIO(B)
B9	DQ/GPIO(D)	E4	GPIO(C)	G15	GPIO(A)	K10	GND	N5	GPIO(B)	R16	GPIO(B)
B10	DQ/GPIO(D)	E5	CCMGND(0)	G16	GPIO(A)	K11	VCC	N6	GPIO(B)	T1	GND
B11	DQ/GPIO(D)	E6	VCCIO(D)	H1	CLK(C)/ CCMIN(0)	K12	GPIO(A)	N7	GPIO(B)	T2	GPIO(B)
B12	DQ/GPIO(D)	E7	VCCIO(D)	H2	GPIO(C)	K13	GPIO(A)	N8	GPIO(B)	T3	GPIO(B)
B13	DQ/GPIO(D)	E8	VCCIO(D)	H3	GPIO(C)	K14	GPIO(A)	N9	GPIO(B)	T4	GPIO(B)
B14	DQ/GPIO(D)	E9	VCCIO(D)	H4	GPIO(C)	K15	GPIO(A)	N10	GPIO(B)	T5	GPIO(B)
B15	DQ/GPIO(D)	E10	VCCIO(D)	H5	VCCIO(C)	K16	GPIO(A)	N11	GPIO(B)	T6	GPIO(B)
B16	DQS/GPIO(D)	E11	VCCIO(D)	H6	TCK	L1	GPIO(C)	N12	GPIO(B)	T7	CLK(B)
C1	GPIO(C)	E12	CCMGND(1)	H7	GND	L2	GPIO(C)	N13	GPIO(B)	T8	GPIO(B)
C2	GPIO(C)	E13	GPIO(A)	H8	VCC	L3	GPIO(C)	N14	GPIO(B)	T9	CLK(B)
C3	GND	E14	GPIO(A)	H9	VCC	L4	GPIO(C)	N15	GPIO(A)	T10	GPIO(B)
C4	DQ/GPIO(D)	E15	GPIO(A)	H10	GND	L5	GPIO(C)	N16	GPIO(B)	T11	GPIO(B)
C5	DQCK_P/GPIO(D)	E16	GPIO(A)	H11	GND	L6	GND	P1	GPIO(B)	T12	GPIO(B)
C6	DQCK_N/GPIO(D)	F1	GPIO(C)	H12	VCCIO(A)	L7	VCC	P2	GPIO(B)	T13	GPIO(B)
C7	DQ/GPIO(D)	F2	GPIO(C)	H13	GPIO(A)	L8	TDI	P3	GND	T14	GPIO(B)
C8	DQ/GPIO(D)	F3	GPIO(C)	H14	GPIO(A)	L9	GND	P4	GPIO(B)	T15	GPIO(B)
C9	DQ/GPIO(D)	F4	GPIO(C)	H15	GPIO(A)	L10	VCC	P5	GPIO(B)	T16	GND
C10	DQCK_N/GPIO(D)	F5	CCMVCC(0)	H16	GPIO(A)	L11	VCCIO(B)	P6	GPIO(B)		
C11	DQ/GPIO(D)	F6	VCCIO(B)	J1	GPIO(C)	L12	VLP	P7	GPIO(B)		

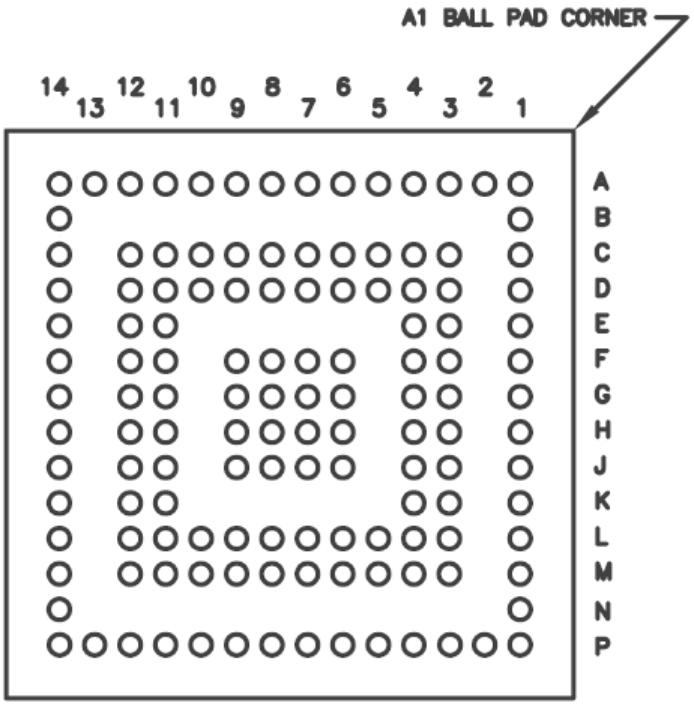
Packaging Pinout Diagrams

PolarPro QL1Pxxx - 132 TFBGA (8 mm x 8 mm) Pinout Diagram

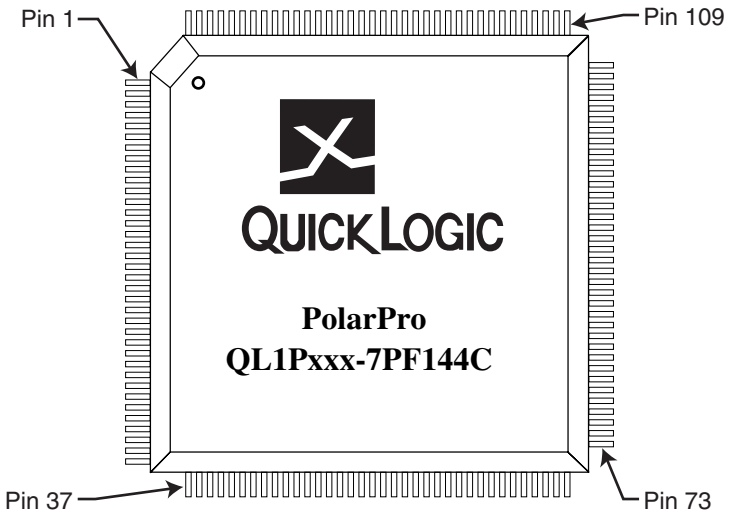
Top



Bottom



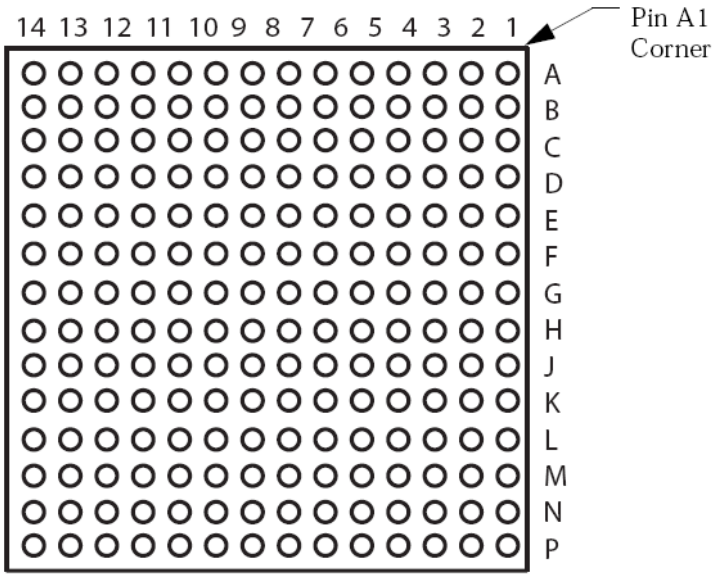
PolarPro QL1Pxxx - 144 TQFP Pinout Diagram



PolarPro QL1Pxxx - 196 TFBGA (12 mm x 12 mm) Pinout Diagram

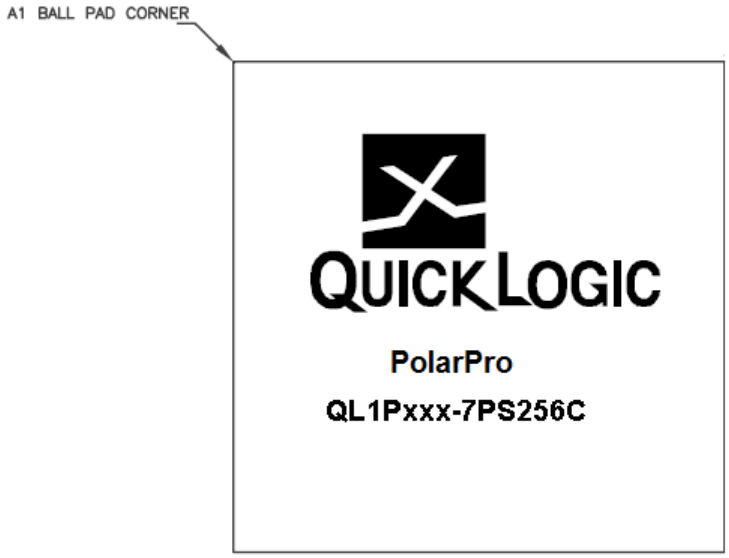
Top

Bottom



PolarPro QL1Pxxx - 256 LBGA Pinout Diagram

Top



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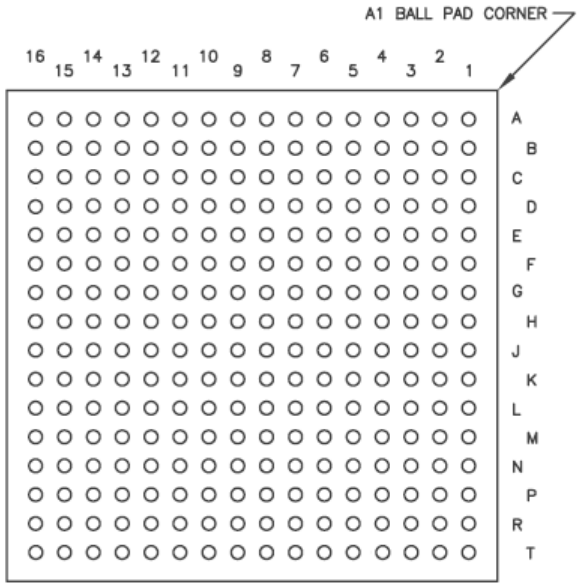
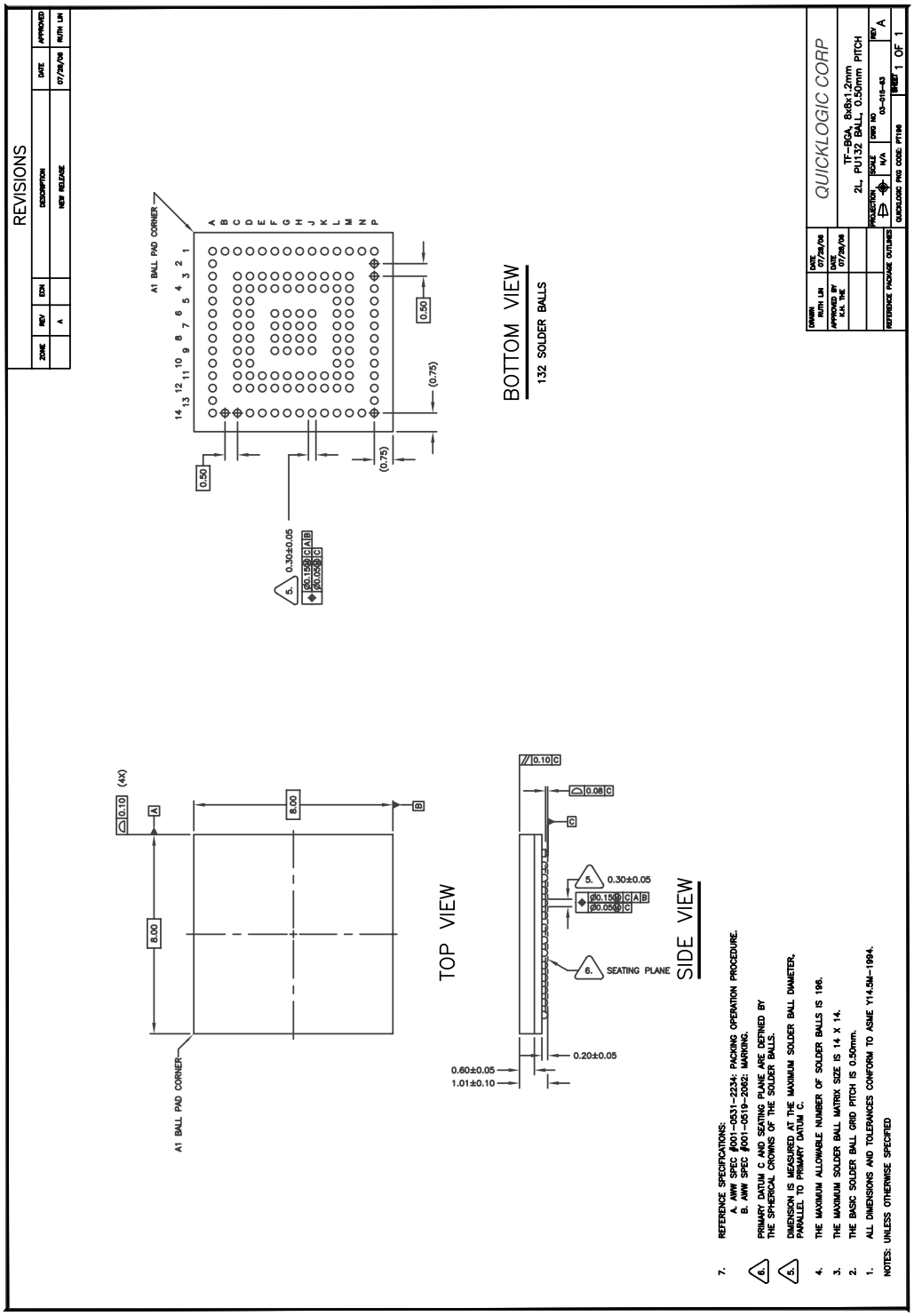
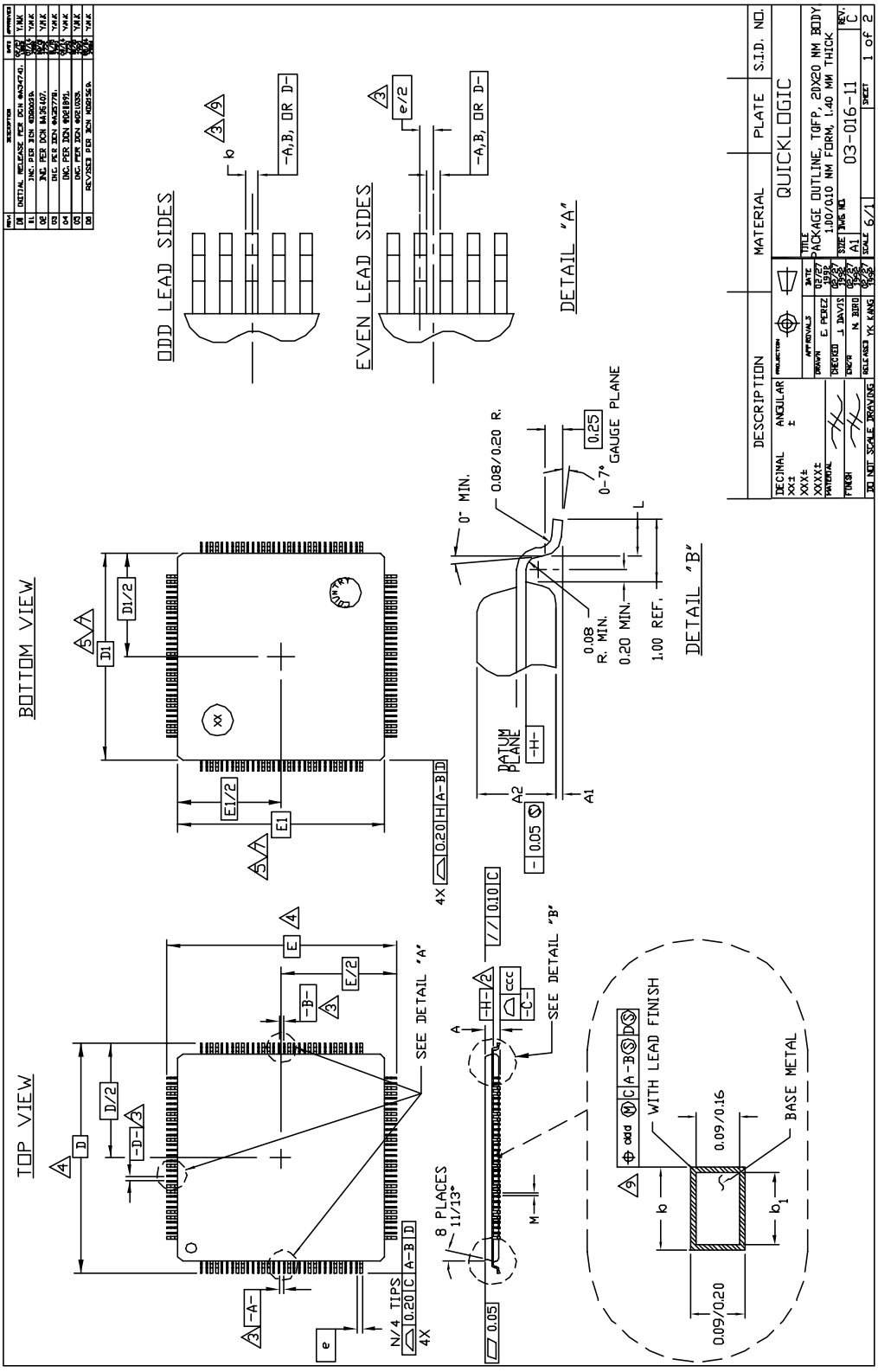


Package Mechanical Drawings

132 TFBGA Packaging Drawing



144 TQFP Packaging Drawing



144 TQFP Packaging Drawing (Continued)

NOTES:

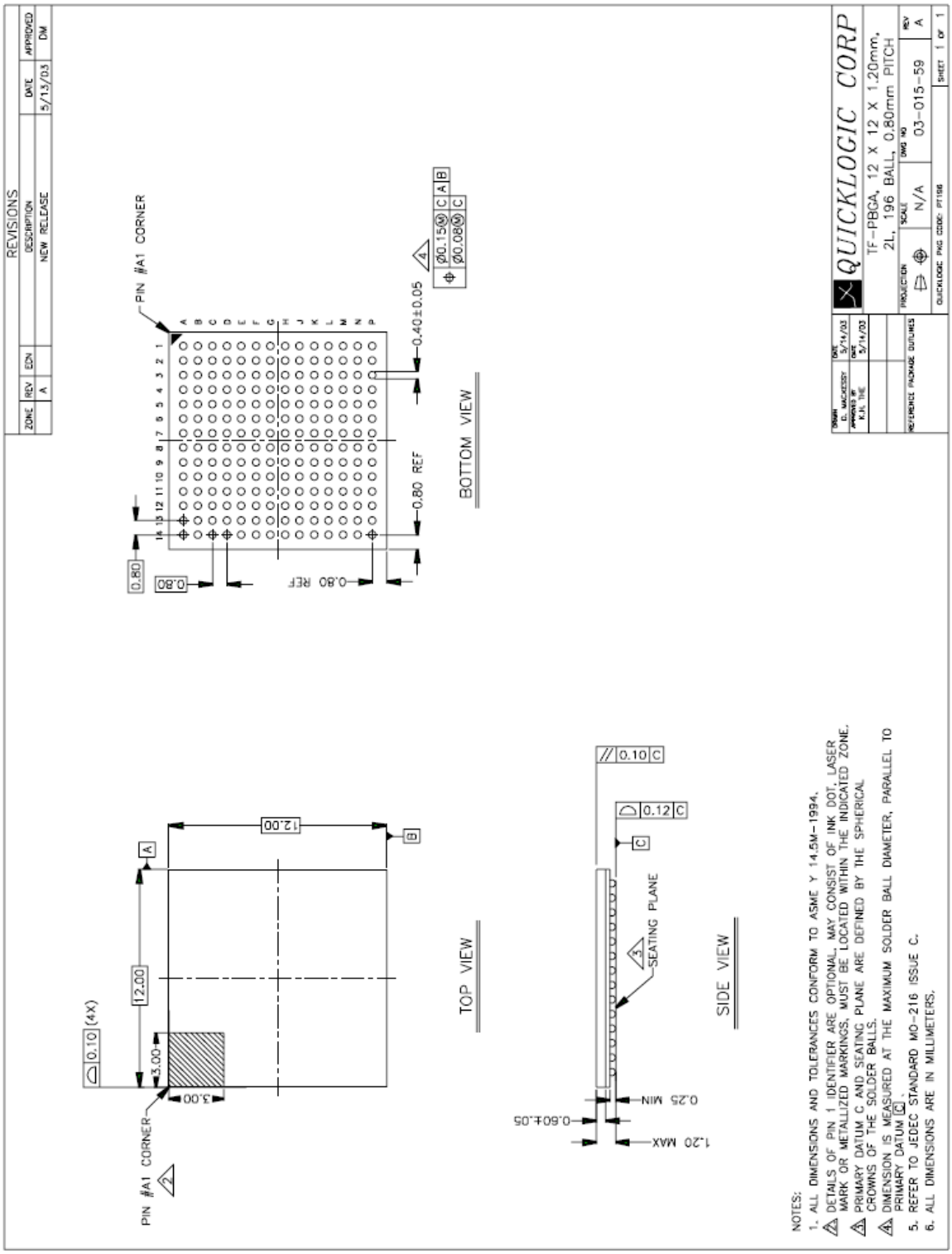
1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5-1982.
2. DATUM PLANE -H- LOCATED AT MOLD PARTING LINE AND COINCIDENT WITH LEAD, WHERE LEAD EXITS PLASTIC BODY AT BOTTOM OF PARTING LINE.
3. DATUMS A-B AND -D- TO BE DETERMINED AT CENTERLINE BETWEEN LEADS WHERE LEADS EXIT PLASTIC BODY AT DATUM PLANE -H- .
4. TO BE DETERMINED AT SEATING PLANE -C- .
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.254 MM ON D1 AND E1 DIMENSIONS.
6. 'N' IS THE TOTAL NUMBER OF TERMINALS.
7. THESE DIMENSIONS TO BE DETERMINED AT DATUM PLANE -H- .
8. THE TOP OF PACKAGE IS SMALLER THAN THE BOTTOM OF PACKAGE BY 0.15 MILLIMETERS, AND THE TOP OF THE PACKAGE WILL NOT OVERHANG THE BOTTOM OF THE PACKAGE.
9. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
10. CONTROLLING DIMENSION: MILLIMETER.
11. MAXIMUM ALLOWABLE DIE THICKNESS TO BE ASSEMBLED IN THIS PACKAGE FAMILY IS 0.38 MILLIMETERS.
12. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-136, VARIATION BT.

SYMBOL	(JEDEC VARIATION) ALL DIMENSIONS IN MILLIMETERS			
	BT			NOTE
	MIN.	NOM.	MAX.	
A			1.60	
A_1	0.05	0.10	0.15	
A_2	1.35	1.40	1.45	
D	22.00 BSC.			4
D_1	20.00 BSC.			7,8
E	22.00 BSC.			4
E_1	20.00 BSC.			7,8
L	0.45	0.60	0.75	
M	0.14			
N	*128, 144			
e	0.50 BSC.			
b	0.17	0.22	0.27	9
b1	0.17	0.20	0.23	
ccc			0.08	
ddd			0.08	

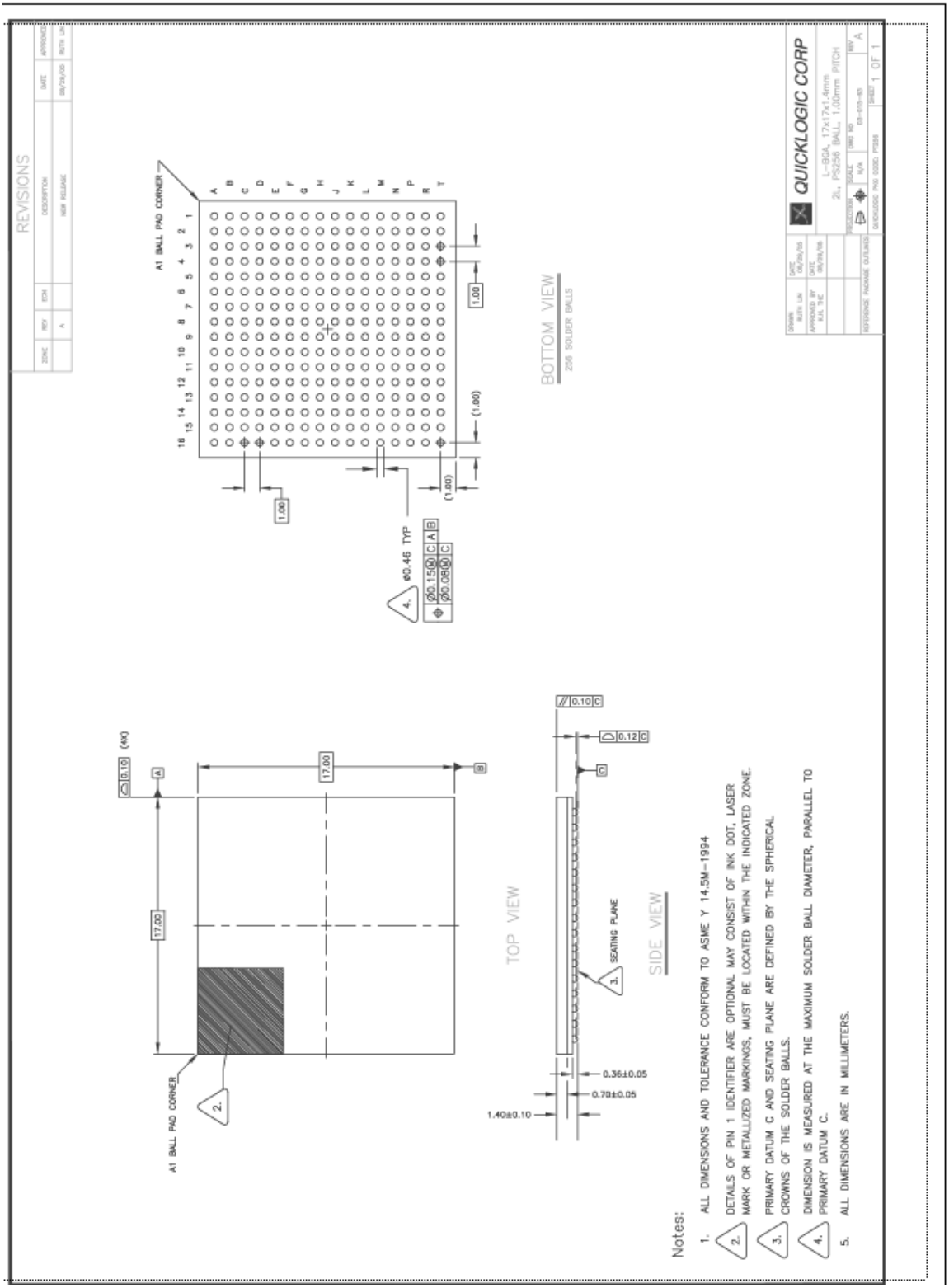
* NOTE: THE 128 LEAD IS A COMPLIANT DEPOPULATION OF THE 144 LEAD MO-136 VARIATION BT.

DRAWING NO.	03-016-11	REV.	C
SCALE	6/1	SHEET	2 OF 2

196 TFBGA (12 mm x 12 mm) Package Drawing



256 LBGA Package Drawing



Packaging Information

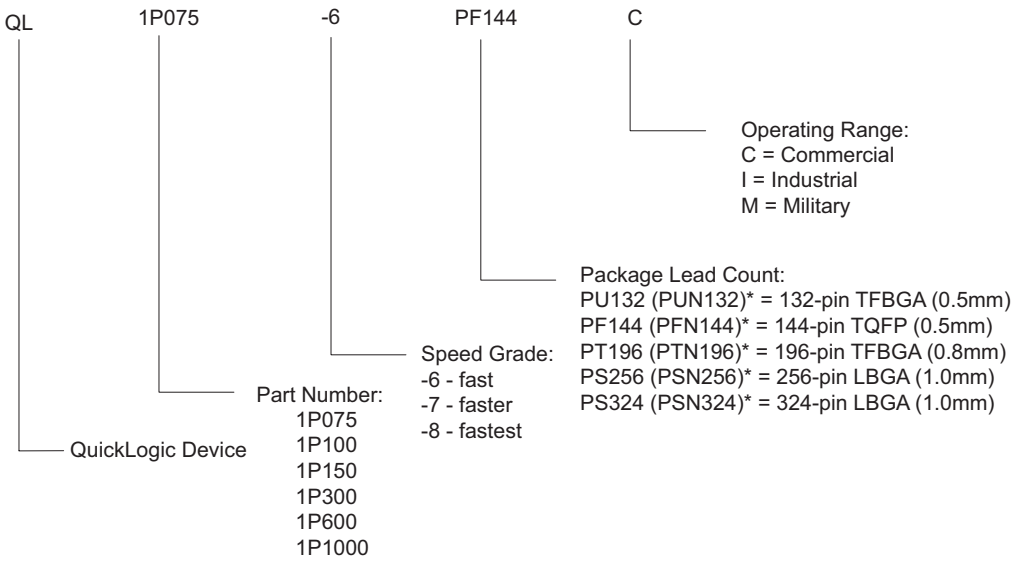
The PolarPro product family packaging information is presented in **Table 68**.

Table 68: Packaging Options

Device Information	Device					
	QL1P075 / QL1P100		QL1P200 / QL1P300		QL1P600 / QL1P1000	
	Pin	Pitch	Pin	Pitch	Pin	Pitch
Package Definitions[a]	132 TFBGA (8 mm x 8mm)	0.50 mm	132 TFBGA (8 mm x 8mm)	0.50 mm	256 LBGA	1.0 mm
	144 TQFP	0.50 mm	256 LBGA	1.0 mm	324 LBGA	1.0 mm
	196 TFBGA (12 mm x 12 mm)	0.80 mm				
	256 LBGA	1.0 mm				

a. TFBGA = Thin Profile Fine Pitch Ball Grid Array
LBGA = Low Profile Ball Grid Array
TQFP = Thin Quad Flat Pack

Ordering Information



* Lead-free packaging is denoted by the character 'N' preceding the number of pins. For availability, contact QuickLogic (see Contact Information).

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Revision History

Revision	Date	Originator and Comments
A	November 2005	Jason Lew and Kathleen Murchek First release
B	March 2005	Jason Lew and Kathleen Murchek
C	March 2005	Jason Lew and Kathleen Murchek
D	June 2006	Senani Gunaratna and Kathleen Murchek
E	August 2006	Jason Lew and Kathleen Murchek
F	August 2006	Jason Lew and Kathleen Murchek
G	September 2006	Jason Lew and Kathleen Murchek

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