SANYO **SANYO Semiconductors**

DATA SHEET

An ON Semiconductor Company

LC749870W — CMOS IC
Silicon gate
NTSC/PAL/SECAM Digital Video Decoder

Overview

The LC749870W is a digital video decoder that converts NTSC, PAL and SECAM video signals into digital component video signals. Digital video data can be output easily by inputting NTSC, PAL and SECAM video signals. The output data format is compatible with ITU-R BT.656.

Features

- Supports NTSC (M, 4.43), PAL (B, D, G, H, I, M, N, 60), and SECAM video signal inputs.
- On-chip video switch that supports 4 video inputs
- 10-bit ADC (sampling at 27MHz)
- Automatic gain control (AGC) function
- Digital clamp circuit
- Digital automatic color control (ACC) circuit
- Sync separation circuit
- Signal-to-noise (S/N) detection capabilities
- Non-standard signal detection function
- No signal detection function
- Adaptive two-dimensional Y/C separation circuit
- NTSC/PAL/SECAM demodulator circuit
- Clock rate conversion circuit
- Picture quality improvement (sharpness, contrast, brightness, CTI, UV gain, HUE)
- 8-bit ITU-R BT.656 output format
  ITU-R BT.656 (8bit YCbCr 4:2:2 with SAV/EAV)
  8bit YCbCr 4:2:2 with Syncs
- I^2C control (100k/400kbps, 2 types of slave address selectable)

SANYO Semiconductor Co., Ltd.
http://semicon.sanyo.com/en/network

IC Specifications
- Power supply voltage   I/O: Analog 3.3V, Digital 1.8V or 3.3V
                                       Core: Analog 1.8V, Digital 1.1V
- Maximum operating frequency: 30MHz
- Package: SQFP64

Applications
- Small-size monitors

Specifications

Absolute Maximum Ratings at $Ta = 25°C$, $DV_{SS} = 0V$, $AV_{SS} = 0V$

Parameter	Symbol	Conditions	Ratings	unit
Maximum supply voltage (I/O)	$DV_{DD}33$ $XV_{DD}33$ $AV_{DD}33$		-0.3 to +3.95	V
Maximum supply voltage (Core)	$DV_{DD}11$ $XV_{DD}11$		-0.3 to +1.8	V
Digital input voltage	V_I		-0.3 to $DV_{DD}33$+0.3	V
Digital output voltage	V_O		-0.3 to $DV_{DD}33$+0.3	V
Operating temperature	Topr		-40 to +85	°C
Storage temperature	Tstg		-55 to +125	°C

Allowable Operation Ranges at $Ta = 25°C$, $DV_{SS} = 0V$, $AV_{SS} = 0V$

Parameter	Symbol	Conditions	min	typ	max	unit
Supply voltage (I/O)	$AV_{DD}33$ $XV_{DD}33$		3.0	3.3	3.6	V
	$DV_{DD}33$		1.7	1.8 or 3.3	3.6	V
Supply voltage (Core)	$DV_{DD}11$ $XV_{DD}11$		1.0	1.1	1.2	V
Input voltage range	V_{IN}		0		$DV_{DD}33$	V

DC Characteristics at $Ta = -30$ to $+70°C$, $DV_{DD}33 = 1.7$ to $3.63V$, $AV_{DD}33 = 3.0$ to $3.63V$, $DV_{DD}11 = 1.0$ to $1.2V$

Parameter	Symbol	Conditions	min	typ	max	unit
Input high-level voltage	V_{IH}	CMOS level inputs	$0.7DV_{DD}33$			V
		CMOS level Schmitt inputs	$0.7DV_{DD}33$			V
Input low-level voltage	V_{IL}	CMOS level inputs	0		$0.3DV_{DD}33$	V
		CMOS level Schmitt inputs	0		$0.3DV_{DD}33$	V
Input high-level current	I_{IH}	$V_I = V_{DD}$			10	μA
		$V_I = V_{DD}$, with pull-down resistance			100	μA
Input low-level current	I_{IL}	$V_I = V_{SS}$	-10			μA
Output high-level voltage	V_{OH}	CMOS (Pin E/G: I_{OH} = -4mA, F: I_{OH} = -6mA)	V_{DD}-0.4			V
Output low-level voltage	V_{OL}	CMOS			0.4	V
Output leakage current	I_{OZ}	When in high-impedance output mode	-10		10	μA
Pull-down register	R_{DN}	$DV_{DD}11 = 1.1V$, $DV_{DD}33 = 3.3V$		159		kΩ
		$DV_{DD}11 = 1.1V$, $DV_{DD}33 = 1.8V$		95		kΩ
Operating current drain	I_{DDOP}	Output open, tck=27MHz, natural image. Ta = 25°C, $DV_{DD}33 = 3.3V$, $AV_{DD}33 = 3.3V$, $DV_{DD}11 = 1.1V$		42		mA
		Output open, tck=27MHz, natural image. Ta = 25°C, $DV_{DD}33 = 1.8V$, $AV_{DD}33 = 3.3V$, $DV_{DD}11 = 1.1V$		38		mA
Static current drain *1	I_{DDST}	Output open, $V_I = V_{SS}$, Ta = 25°C		10		μA

*1: There is an input pin which builds in pull down resistance. Note that there is no guarantee about static consumption current depending on circuit configuration.
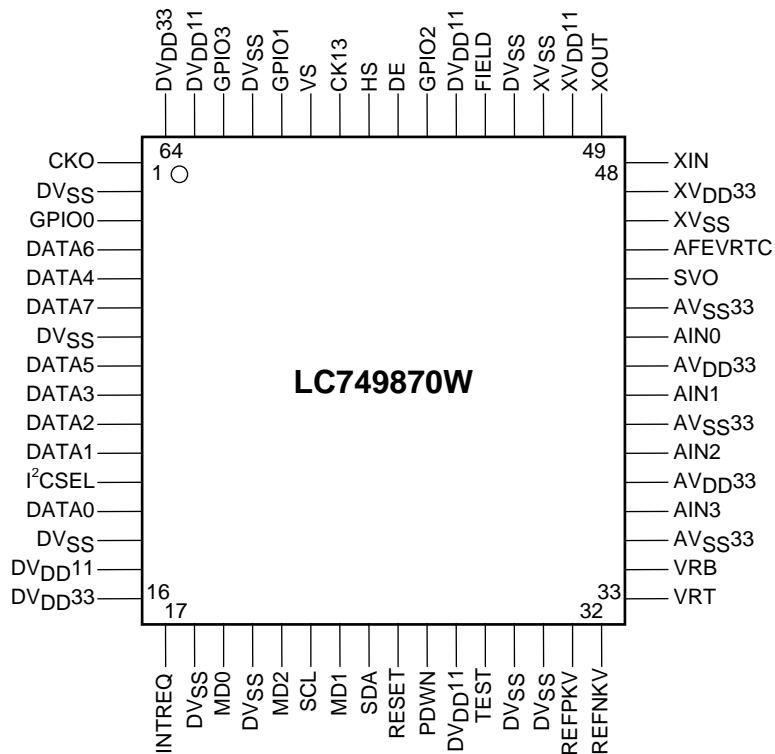
Package Dimensions

unit : mm (typ)

3190A

SANYO : SQFP64(10X10)
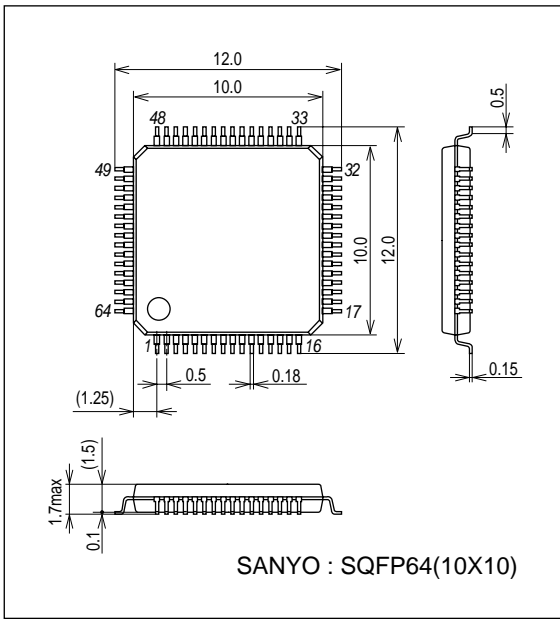
Pin Assignment

Top view

LC749870W

Pin Descriptions

Pin No.	Symbol	I/O	Type	Connected to		Notes
1	CKO	O	F	CMOS	Digital	Data synchronous clock output
2	DV$_{SS}$	P		GND	Digital	
3	GPIO0	I/O	G	CMOS	Digital	For test
4	DATA6	I/O	G	CMOS	Digital	Video signal output
5	DATA4	I/O	G	CMOS	Digital	Video signal output
6	DATA7	I/O	G	CMOS	Digital	Video signal output (MSB)
7	DV$_{SS}$	P		GND	Digital	
8	DATA5	I/O	G	CMOS	Digital	Video signal output
9	DATA3	I/O	G	CMOS	Digital	Video signal output
10	DATA2	I/O	G	CMOS	Digital	Video signal output
11	DATA1	I/O	G	CMOS	Digital	Video signal output
12	I^{2}CSEL	I	C	CMOS	Digital	I^{2}C slave select L = 0x88, H = 0x8A
13	DATA0	I/O	G	CMOS	Digital	Video signal output (LSB)
14	DV$_{SS}$	P		GND	Digital	
15	DV$_{DD}$11	P		Core voltage	Digital	
16	DV$_{DD}$33	P		I/O voltage	Digital	
17	INTREQ	O	E	CMOS	Digital	Interrupt ("H" active)
18	DV$_{SS}$	P		GND	Digital	
19	MD0	I	D	CMOS	Digital	For test (Connect to GND)
20	DV$_{SS}$	P		GND	Digital	
21	MD2	I	D	CMOS	Digital	For test (Connect to GND)
22	SCL	I	D	CMOS	Digital	I^{2}C clock
23	MD1	I	D	CMOS	Digital	For test (Connect to GND)
24	SDA	I/O	G	CMOS	Digital	I^{2}C data input/output
25	RESET	I	B	CMOS	Digital	System reset ("L" active)
26	PDWN	I	B	CMOS	Digital	Power down control
27	DV$_{DD}$11	P		Core voltage	Digital	
28	TEST	I	C	CMOS	Digital	For test (Connect to GND)
29	DV$_{SS}$	P		GND	Digital	
30	DV$_{SS}$	P		GND	Digital	
31	REFPKV	I	A		Analog	ADC top reference buffer-amp input
32	REFNKV	I	A		Analog	ADC bottom reference buffer-amp input
33	VRT	I	A		Analog	ADC top reference voltage input
34	VRB	I	A		Analog	ADC bottom reference voltage input
35	AV$_{SS}$33	P		GND	Analog	
36	AIN3	I	A		Analog	Video signal input (CVBS)
37	AV$_{DD}$33	P		Analog Voltage	Analog	
38	AIN2	I	A		Analog	Video signal input (CVBS)
39	AV$_{SS}$33	P		GND	Analog	
40	AIN1	I	A		Analog	Video signal input (CVBS)
41	AV$_{DD}$33	P		Analog Voltage	Analog	
42	AIN0	I	A		Analog	Video signal input (CVBS)
43	AV$_{SS}$33	P		GND	Analog	
44	SVO	O	A		Analog	AFE SVO output
45	AFEVRTC	I	A		Analog	ADC D-range control voltage external input
46	XV$_{SS}$	P		GND	Digital	
47	XV$_{DD}$33	P		I/O Voltage	Digital	
48	XIN	I	H	CMOS	Digital	X'tal input
49	XOUT	O	H	CMOS	Digital	X'tal output
50	XV$_{DD}$11	P		Core Voltage	Digital	
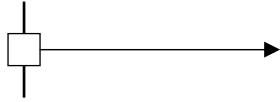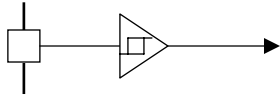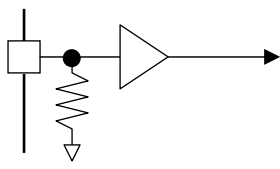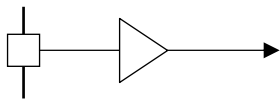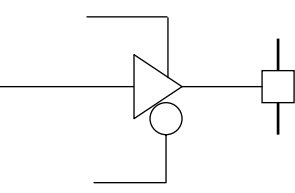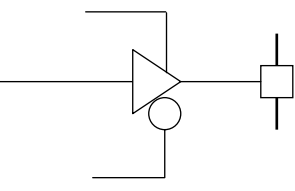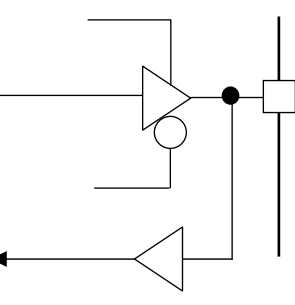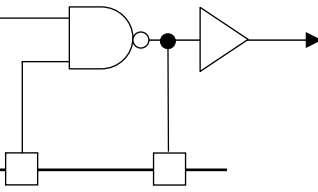
Continued from preceding page.

Pin No.	Pin symbol	I/O Type		Connected to		Notes
		I/O	Type			
51	XV$_{SS}$	P		GND	Digital	
52	DV$_{SS}$	P		GND	Digital	
53	FIELD	I/O	G	CMOS	Digital	Field signal
54	DV$_{DD}$11	P		Core voltage	Digital	
55	GPIO2	I/O	G	CMOS	Digital	For test
56	DE	I/O	G	CMOS	Digital	Data enable signal
57	HS	I/O	G	CMOS	Digital	Horizontal sync signal
58	CK13	O	F	CMOS	Digital	Clock output (13.5MHz)
59	VS	I/O	G	CMOS	Digital	Vertical sync signal
60	GPIO1	I/O	G	CMOS	Digital	For test
61	DV$_{SS}$	P		GND	Digital	
62	GPIO3	I/O	G	CMOS	Digital	For test
63	DV$_{DD}$11	P		Core voltage	Digital	
64	DV$_{DD}$33	P		I/O voltage	Digital	

Pin Circuits

I/O type	Function	Equivalent Circuit	Applicable Pins
A	Analog input/output		AIN0, AIN1, AIN2, AIN3, VRT, VRB, REFPKV, REFNKV, SVO, AFEVRTC
B	Schmitt trigger CMOS input		PDWN, RESET
C	CMOS input with built-in pull-down resistor		I^2CSEL, TEST
D	CMOS input		SCL, MD0, MD1, MD2
E	2mA/4mA switching 3-STATE drive CMOS output		INTREQ
F	4mA/8mA switching 3-STATE drive CMOS output		CKO, CK13
G	2mA/4mA switching 3-STATE drive CMOS input/output		SDA, GPIO0, GPIO1, GPIO2, GPIO3, DATA0, DATA1, DATA2, DATA3, DATA4, DATA5, DATA6, DATA7, FIELD, DE, VS, HS
H	Oscillator		XIN, XOUT

Pin Connection

1) ADC and its peripherals

REFPKV VRT VRB REFNKV

0.1µF

0.1µF — AIN*

10µF   10µF

0.1µF — AFEVRTC
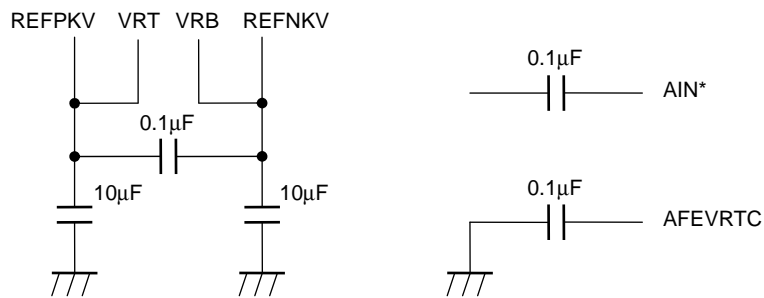
Capacitors must be placed as close as possible to the IC.

2) Unused Pin Handling (Please be sure to perform except input open processing)
   AIN0 to AIN3: Open
   PDWN: Pull up
   TEST, MD0, MD1, MD2: Pull down
   RESET: Must always be configured for input.
   GPIO0 to GPIO3: Open
   DATA0 to DATA7: Open
   FIELD, DE, VS, HS: Open
   CKO, CK13: Open
   INTREQ: Open
   SVO: Open

Block Diagram
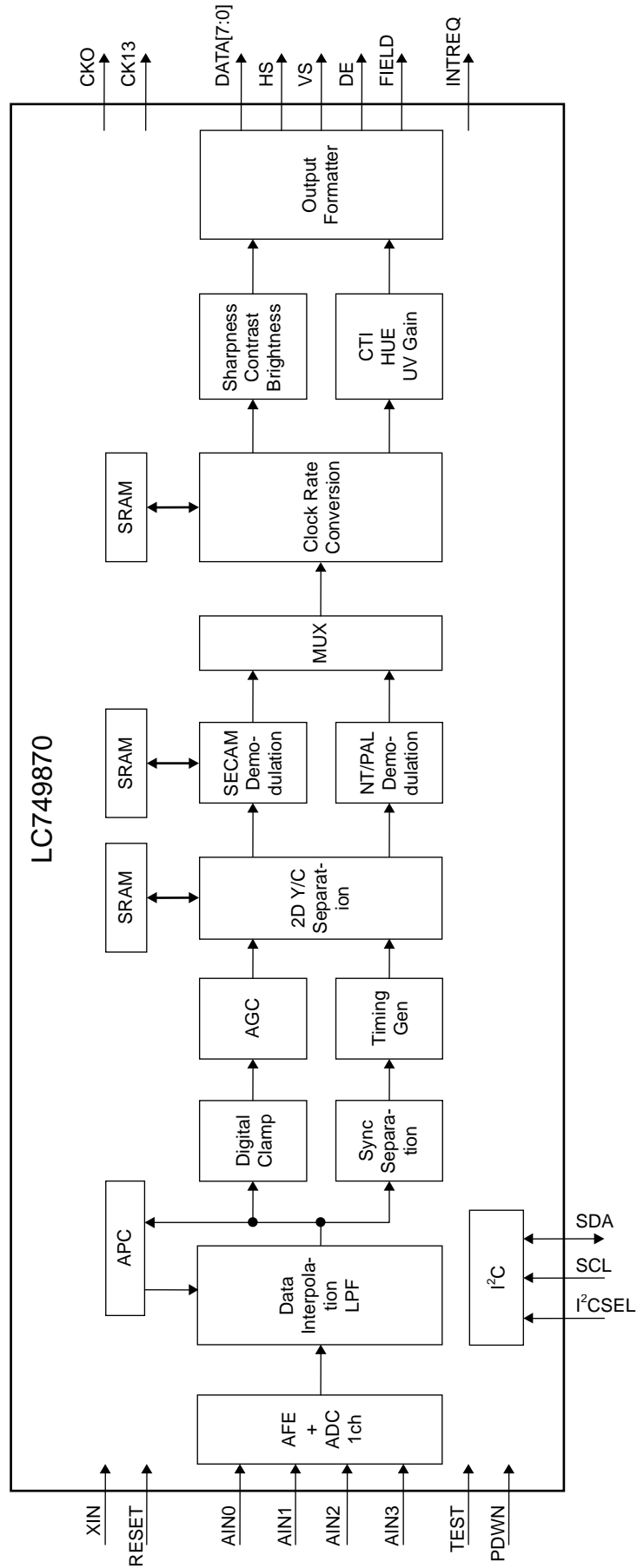
Input/Output Timing

1) Input clock timing
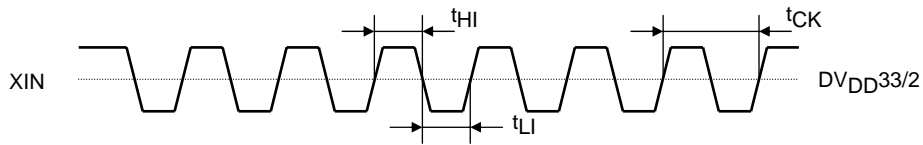
Pin Name	Parameter	Symbol	min	typ	max	unit
XIN	Clock cycle	t_{CK}		37		ns
	Duty			50		%

2) Output data timing
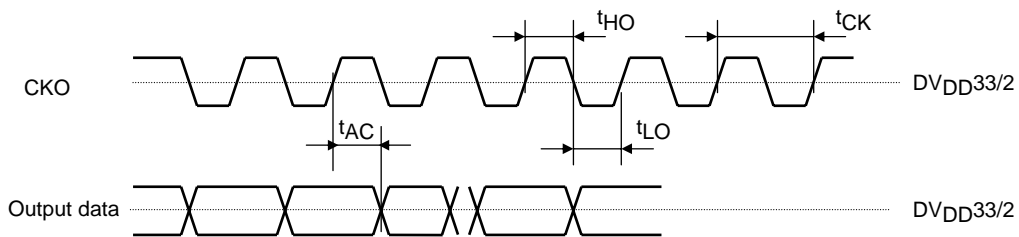
Pin Name	Parameter	Symbol	min	typ	max	unit
CKO	Clock cycle	t_{CK}		37		ns
	Duty			50		%
DATA*, HS,VS,DE,FIELD, INTREQ	Output data delay time ($DV_{DD}33$ = 2.6 to 3.6V) Pins E,G: 4mA setting Pin F: 8mA setting	t_{AC}	-3		3	ns
	Output data delay time ($DV_{DD}33$ = 2.6 to 3.6V) Pins E,G: 2mA setting Pin F: 4mA setting	t_{AC}	-3		6	ns
	Output data delay time ($DV_{DD}33$ = 1.7 to 1.9V) Pins E,G: 4mA setting Pin F: 8mA setting	t_{AC}	-5		4	ns
	Output data delay time ($DV_{DD}33$ = 1.7 to 1.9V) Pins E,G: 2mA setting Pin F: 4mA setting	t_{AC}	-6		9	ns

Register Specifications

BANK0 (AFE + ADC) Register Specification

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
00$_H$	7	I2C_BGRPWDB	1	Power down control	Band gap reference power down control 0: Power down　1: Normal operation	0$_H$
	6	I2C_SVOPWDB	1		AFE SVO AMP power down control 0: SVO AMP circuit OFF　1: SVO AMP circuit ON	0$_H$
	5	I2C_SELFCLPPWDB	1		AFE self clamp circuit power down control 0: Self clamp OFF　1: Self clamp ON	0$_H$
	4	I2C_AFEPWDB	1		AFE power down control 0: AFE power down　1: AFE normal operation	0$_H$
	3	I2C_ADCPWDB	1		×2 AMP circuit and ×2 AMP bias circuit power down control 0: Power down　1: Normal operation	0$_H$
	2		1		Reference voltage generation circuit 1 power down control 0: Power down　1: Normal operation	0$_H$
	1		1		Reference voltage generation circuit 2 power down control 0: Power down　1: Normal operation	0$_H$
	0		1		Clock generation circuit power down control 0: Power down　1: Normal operation	0$_H$
01$_H$	7	I2C_LPFPWDB	1		LPF buffer circuit power down control 0: Power down　1: Normal operation	0$_H$
	6:5	I2C_AINSEL	2	Input switch control	AFE 4-input selector control signal (when in normal operation) 00: AIN0　01: AIN1　10: AIN2　11: AIN3	0$_H$
	4	I2C_CLPLPFON	1	LPF enable control	LPF enable control of AFE self clamp circuit 0: LPF OFF　1: LPF ON	0$_H$
	3:2	-	2	For test	For test Normally set to 0$_H$	0$_H$
	1:0	-	2	For test	For test Normally set to 0$_H$	0$_H$
02$_H$	7	I2C_SCARTON	1	AGC mode control	AFE D-range control voltage external input select control 0: AGC mode　1: Non-AGC mode	0$_H$
	6	-	1	For test	For test Normally set to 0$_H$	0$_H$
	5:0	-	6	For test	For test Normally set to 00$_H$	00$_H$
03$_H$	7	-	1	For test	For test Normally set to 0$_H$	0$_H$
	3:1	-	3	For test	For test Normally set to 0$_H$	0$_H$
	0	-	1	For test	For test Normally set to 0$_H$	0$_H$
04$_H$	5:4	-	2	For test	For test Normally set to 0$_H$	0$_H$
	3	-	1	For test	For test Normally set to 1$_H$	0$_H$
	2:0	-	3	For test	For test Normally set to 4$_H$	0$_H$
05$_H$	7	-	1	For test	For test Normally set to 0$_H$	0$_H$
	6		1		For test Normally set to 0$_H$	0$_H$
	5		1		For test Normally set to 0$_H$	0$_H$
	4		1		Reserved	0$_H$
	3		1		Reserved	0$_H$
	2		1		Reserved	0$_H$
	1		1		Reserved	0$_H$
	0		1		For test Normally set to 0$_H$	0$_H$

LC749870W

Continued from preceding page.

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
06H	7		1		For test Normally set to 0H	0H
	6		1		For test Normally set to 0H	0H
	5		1		For test Normally set to 0H	0H
	4		1		For test Normally set to 0H	0H
	3		1		For test Normally set to 0H	0H
	2		1		For test Normally set to 0H	0H
	1		1		For test Normally set to 0H	0H
	0	-	1	For test	For test Normally set to 0H	0H
07H	7		1		For test Normally set to 0H	0H
	6		1		For test Normally set to 0H	0H
	5		1		For test Normally set to 0H	0H
	4		1		For test Normally set to 0H	0H
	3		1		For test Normally set to 0H	0H
	2		1		For test Normally set to 0H	0H
	1		1		For test Normally set to 0H	0H
	0		1		For test Normally set to 0H	0H
08H	1	I2C_IOSEL2	1	Clock output current drive capability	Clock output current drive capability switching 0: 4mA 1: 8mA	0H
	0	I2C_IOSEL1	1	Signal output current drive capability	Signal output current drive capability switching 0: 2mA 1: 4mA	0H
09H to 0FH	-	-	-	-	-	-
10H	7	I2C_SRST	1	Soft reset	Software reset of digital video signal processing block 0: Reset ON 1: Reset OFF	0H
	0	-	1	For test	For test Normally set to 0H	0H
11H	7:6	-	2	For test	For test Normally set to 0H	0H
	1:0	-	2	For test	For test Normally set to 0H	0H
12H	0	I2C_CKINV	1	Clock output invert	Clock output (CKO) invert control 0: Normal 1: Invert	0H
13H	6:4	-	3		For test Normally set to 0H	0H
	2:0	-	3		For test Normally set to 0H	0H
14H	7:0	-	8	For test	For test Normally set to 0H	00H
15H	7:0	-	8		For test Normally set to 0H	00H
16H	7:0	-	8		For test Normally set to 0H	00H

BANK1 (Digital Video Signal Processing Block 1) Register Specifications

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
00H	5:4	-	2	For test	For test Normally set to 0H	0H
	0	-	1	For test	For test Normally set to 0H	0H
01H	7:6	I2A_ACCON	2	ACC control	ACC ON/OFF switching 00: OFF 01: ON 1x: Amplifier fixed	1H
	5:4	I2A_ACCFRAME	2	Number of update frames	Number of update frame select 00: 1 frame 01: 2 frames 10: 4 frames 11: 8 frames	0H
	3:0	-	4	For test	For test Normally set to 0H	0H
02H	7:3	I2A_ACCSELAMP	5	ACC amplifier fixed mode	ACC amplifier fixed mode Gain adjustment -5 to +26dB	00H
	2:0	I2A_TMCTRL	3	Auto mode switching	Auto/manual mode switching 000: Auto 001: NTSC-M 010: NTSC-4.43 011: PAL 100: PAL-M 101: PAL-N 110: PAL-60 111: SECAM	0H
03H	7:0	-	8	For test	For test Normally set to 20H	20H
04H	7:0	-	8	For test	For test Normally set to 80H	80H
05H	7:0	-	8	For test	For test Normally set to 40H	40H
06H	7:0	-	8		For test Normally set to 10H	10H
07H	7:0	-	8	For test	For test Normally set to 80H	80H
08H	7:0	-	8	For test	For test Normally set to 00H	00H
09H	7:0	-	8	For test	For test Normally set to 80H	80H
0AH	7:5	-	3	For test	For test Normally set to 5H	5H
	4	-	1	For test	For test Normally set to 0H	0H
	3:0	-	4	For test	For test Normally set to 2H	2H
0BH	7:4	-	4	For test	For test Normally set to 3H	3H
	3:0	-	4		For test Normally set to 3H	3H
0CH	7	-	1	For test	For test Normally set to 0H	0H
	6:0	-	7	For test	For test Normally set to 18H	18H
0DH	7:0	-	8	For test	For test Normally set to A0H	A0H
0EH	-	-	-	-	-	-
0FH	7:0	-	8	For test	For test Normally set to 60H	60H
10H	7:0	-	8	For test	For test Normally set to 80H	80H
11H	7:4	-	4	For test	For test Normally set to CH	CH
	3:0		4		For test Normally set to 8H	8H
12H	7:6	-	2	For test	For test Normally set to 3H	3H
	5:4	-	2	For test	For test Normally set to 3H	3H
	3	-	1		For test Normally set to 1H	1H
	2:0	-	3	For test	For test Normally set to 0H	0H

Continued from preceding page.

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
13$_H$	6:4	-	3	For test	For test Normally set to 0$_H$	0$_H$
	1:0	-	2	For test	For test Normally set to 2$_H$	2$_H$
14$_H$	7:0	-	8		For test Normally set to 96$_H$	96$_H$
15$_H$	7:0	-	8	For test	For test Normally set to 64$_H$	64$_H$
16$_H$	7:0	-	8		For test Normally set to 64$_H$	64$_H$
17$_H$	7:4	I2A_ATMODE	4	Video system auto-detect switch	Auto mode switching (It takes effect at I2A_TMCTRL=3'h0.) 0000: Manual mode 0001: Auto0 (NTSC/PAL) 0010: Auot1 (PAL/SECAM) 0011: Auto2 (NTSC/PAL-N/PAL-M) 0100: Auto3 (NTSC/PAL/SECAM) 0101: Auto4 (NTSC/PAL/SECAM/PAL-N/PAL-M) 0110: Auto5 (Auto0+NTSC-443/PAL-60) 0111: Auto6 (Auto1+NTSC-443/PAL-60) 1000: Auto7 (Auto2+NTSC-443/PAL-60) 1001: Auto8 (Auto3+NTSC-443/PAL-60) 1010: Auto9 (Auto4+NTSC-443/PAL-60) 1011 to 1111: Full	F$_H$
	3:2	I2A_FSCSEL	2	Fsc select	Fsc select at manual mode 00: 3.579545MHz 01: 4.43361875MHz 10: 3.57561149MHz 11: 3.58205625MHz	1$_H$
	1	I2A_SCANSEL	1	Scanning line number select	Scanning line number select at manual mode 0: 525i 1: 625i	0$_H$
	0	I2A_NTPALSEL	1	NTSC/PAL select	NTSC/PAL select at manual mode 0: NTSC 1: PAL	0$_H$
18$_H$	7:6	-	2	For test	For test Normally set to 3$_H$	3$_H$
	5:4	-	2		For test Normally set to 0$_H$	0$_H$
	1	-	1	For test	For test Normally set to 1$_H$	1$_H$
	0	I2A_SECAMSEL	1	SECAM select	SECAM select at manual mode 0: not SECAM 1: SECAM	0$_H$
19$_H$	6:0	-	7	For test	For test Normally set to 7F$_H$	7F$_H$
1A$_H$	6:0	-	7		For test Normally set to 00$_H$	00$_H$
1B$_H$	2	I2A_DCON	1	Digital clamp ON/OFF setting	Digital clamp ON/OFF setting 0: OFF 1: ON	1$_H$
	1	I2A_DCLINE	1	Detection level update unit switching	Pedestal level update unit switching 0: Each frame 1: Each line	0$_H$
	0	-	1	For test	For test Normally set to 0$_H$	0$_H$
1C$_H$	6:0	I2A_STDLEVY	7	Pedestal level setting	Target pedestal level setting Level setting range: 236 to 363LSB	40$_H$
1D$_H$	7:5	I2A_TCDC	3	Time constant setting	Digital clamp time constant setting 000: Time constant none 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110: 1/64 111: 1/128	0$_H$
	4:0	I2A_FRAMEDC	5	Update field number setting	Pedestal level update field number setting Setting range: 0 to 31 fields	10$_H$
1E$_H$	6:0	-	7	For test	For test Normally set to 00$_H$	00$_H$
1F$_H$	4:0	-	5	For test	For test Normally set to 17$_H$	17$_H$

Continued from preceding page.

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
20H	7	I2A_FILSEL	1	LPF characteristic switch	LPF characteristic switching for sync separation (It takes effect at I2A_AUTOFIL = 1'b0.) 0: Cutoff frequency 0.35MHz 1: Cutoff frequency 1.4MHz	1H
	6	I2A_AUTOFIL	1	LPF characteristic auto-switching setting	LPF characteristics automatic switching setting for sync separation 0: OFF 1: ON	1H
	5	-	1	For test	For test Normally set to 1H	1H
	4	-	1	For test	For test Normally set to 0H	0H
	3:0	-	4	For test	For test Normally set to FH	FH
21H	7:0	-	8		For test Normally set to 55H	55H
22H	7	-	1	For test	For test Normally set to 1H	1H
	6	-	1		For test Normally set to 0H	0H
	5	I2A_MANMODE	1		Input signal system auto/manual setting 0: Auto setting 1: Manual setting	0H
	4		1		Input signal line number auto/manual setting 0: Auto setting 1: Manual setting	0H
	2:0	I2A_TVMODE	3	Input signal system setting	Input signal system setting (It takes effect at I2A_MANMODE[1] = 1'b1) 000: NTSC-M 001: PAL-M 010: PAL-N 011: PAL-GBI 100: SECAM	0H
23H	6	I2A_INSIG	1		Input signal line number setting (It takes effect at I2A_MANMODE[0] = 1'b0) 0: 625 lines 1: 525 lines	1H
	5:4	-	2	For test	For test Normally set to 1H	1H
	3:0	-	4	For test	For test Normally set to 1H	1H
24H	7	I2A_SLDET	1	Slice level setting	Sync separation slice level auto-setting 0: Manual setting 1: Auto setting	1H
	5:4	I2A_TCLEV	2	Slice level time constant setting	Slice level time constant setting 00: 1/2 01: 1/4 10: 1/8 11: 1/16	1H
	3:2	I2A_LEVAD	2	Initial slice level setting	Slice level initial value setting 00: 60LSB 01: 80LSB 10: 100LSB 11: 120LSB As for an initial value of the slice level, the above value is added to the detected sync tip level.	3H
25H	7:0	I2A_SLST	8	Slice level Level setting range: 236 to 363LSB setting	Slice level setting (It takes effect at I2A_SLDET = 1'b0) Settable in 4 LSB units Setting range: 0 to 1020LSB	08H
26H	7:4	-	4		For test Normally set to 7H	7H
	3:0	-	4	For test	For test Normally set to 9H	9H
27H	7:4	-	4		For test Normally set to 7H	7H
	3:2	-	2	For test	For test Normally set to 3H	3H
	1:0	-	2		For test Normally set to 0H	0H
28H	7:4	-	4	For test	For test Normally set to 3H	3H
	3:0	-	4		For test Normally set to 1H	1H

Continued on next page.

Continued from preceding page.

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
29$_H$	7	-	1	For test	For test Normally set to 1$_H$	1$_H$
	6:4	-	3	For test	For test Normally set to 1$_H$	1$_H$
	2:0	-	3		For test Normally set to 7$_H$	7$_H$
2A$_H$	7:0	-	8	For test	For test Normally set to 04$_H$	04$_H$
2B$_H$	7:0	-	8		For test Normally set to 14$_H$	14$_H$
2C$_H$	7:0	-	8		For test Normally set to 00$_H$	00$_H$
2D$_H$	7:0	-	8		For test Normally set to 03$_H$	03$_H$
2E$_H$	6:4	-	3	For test	For test Normally set to 4$_H$	4$_H$
2F$_H$	5:0	-	6		For test Normally set to 02$_H$	02$_H$
30$_H$	5:0	-	6		For test Normally set to 01$_H$	01$_H$
31$_H$	7:0	I2A_HSPAD	8	H-sync positioning	H-sync position adjustment	05$_H$
32$_H$	7	-	1	For test	For test Normally set to 0$_H$	0$_H$
	6	-	1	For test	For test Normally set to 1$_H$	1$_H$
	5	-	1		For test Normally set to 1$_H$	1$_H$
	4	-	1	For test	For test Normally set to 1$_H$	1$_H$
	3:0	-	4		For test Normally set to 0$_H$	0$_H$
33$_H$	7:0	-	8	For test	For test Normally set to CB$_H$	CB$_H$
34$_H$	7:0	-	8	For test	For test Normally set to CA$_H$	CA$_H$
35$_H$	7:0	-	8	For test	For test Normally set to CD$_H$	CD$_H$
36$_H$	6	-	1	For test	For test Normally set to 1$_H$	1$_H$
	5	-	1	For test	For test Normally set to 0$_H$	0$_H$
	4	I2A_FIXLN	1	Line number fixed mode ON/OFF setting	Line number fixed mode ON/OFF setting 0: OFF 1: ON	1$_H$
	2:0	I2A_VSTART	3	V-sync positioning	V-sync position adjustment	3$_H$
37$_H$	7:5	I2A_VBSTART	3	V-blank positioning	V-blank position adjustment	3$_H$
	4:0	I2A_HBSTART	5	H-blank rising positioning	H-blank rising position adjustment	0F$_H$
38$_H$	7:5	I2A_VBWIDTH	3	V-blank width adjustment	V-blank width adjustment	3$_H$
	4:0	I2A_HBEND	5	H-blank falling positioning	H-blank falling position adjustment	0F$_H$

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
39$_H$	7:0	-	8	For test	For test Normally set to 50$_H$	50$_H$
3A$_H$	7:0	-	8	For test	For test Normally set to 10$_H$	10$_H$
3B$_H$	7:0	-	8	For test	For test Normally set to 24$_H$	24$_H$
3C$_H$	7:0	-	8	For test	For test Normally set to F1$_H$	F1$_H$
3D$_H$	7:0	-	8	For test	For test Normally set to 93$_H$	93$_H$
3E$_H$	7:0	-	8	For test	For test Normally set to 50$_H$	50$_H$
3F$_H$	7:0	-	8	For test	For test Normally set to 30$_H$	30$_H$
40$_H$	7:0	-	8	For test	For test Normally set to 18$_H$	18$_H$
41$_H$	7:0	-	8	For test	For test Normally set to 25$_H$	25$_H$
42$_H$	7:0	-	8	For test	For test Normally set to 23$_H$	23$_H$
43$_H$	7:0	-	8	For test	For test Normally set to C8$_H$	C8$_H$
44$_H$	7	I2A_NSDON	1	No signal detection ON/OFF setting	No signal detection ON/OFF setting 0: OFF 1: ON	1$_H$
	6		1		Forced no signal mode ON/OFF setting (It takes effect at I2A_NSDON[1] = 1'b0) 0: OFF 1: ON	1$_H$
	4	-	1	For test	For test Normally set to 0$_H$	0$_H$
	3:2	I2A_NSDTHH	2	No signal detection threshold setting	Threshold setting where signals can be measured	0$_H$
	1:0	I2A_NSDTHL	2		Threshold setting where no signal can be measured	1$_H$
45$_H$	5	-	1	For test	For test Normally set to 0$_H$	0$_H$
	3:2	-	2	For test	For test Normally set to 1$_H$	1$_H$
	1:0	-	2	For test	For test Normally set to 1$_H$	1$_H$
46$_H$	4:0	-	5	For test	For test Normally set to 10$_H$	10$_H$
47$_H$	5:0	-	6		For test Normally set to 3F$_H$	3F$_H$
48$_H$	5	-	1	For test	For test Normally set to 0$_H$	0$_H$
	3	-	1	For test	For test Normally set to 0$_H$	0$_H$
	2	-	1	For test	For test Normally set to 0$_H$	0$_H$
	1	I2A_EXAGCON	1	External AGC ON/OFF setting	External AGC ON/OFF setting 0: OFF 1: ON	0$_H$
49$_H$	7:0	-	8	For test	For test Normally set to 00$_H$	00$_H$
4A$_H$	7:0	-	8		For test Normally set to 00$_H$	00$_H$
4B$_H$	7:0	I2A_SYNLEV	8	Sync level setting	AGC target sync level setting Setting range: 158 to 413LSB	80$_H$
4C$_H$	6:4	I2A_FRMCNT	3	Update field number setting	AGC update field number setting	0$_H$
	3:0	I2A_FIXGAIN	4	Fixed gain setting	Fixed gain setting Setting range: -6 to +9dB	6$_H$

Continued from preceding page.

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
4D$_H$	7:6	I2A_TCAGC	2	Time constant setting	AGC time constant setting 00: No time constant 01: 1/2 10: 1/4 11: 1/8	0$_H$
	4:0	I2A_EXAGCINIT	5	External AGC gain value setting	External AGC initial gain value setting	0F$_H$
4E$_H$	7:6	I2A_AMPLIMIT	2	Amplifier limit switching	AGC amplifier limit switching 00: ±3dB 01: ±6dB 10: ±9dB 11: ±12dB	0$_H$
	4:0	-	5	For test	For test Normally set to 00$_H$	00$_H$
4F$_H$	7:5	I2A_NLFIELD	3	Update field number setting	Noise detection results update field number setting 000: 1 field 001: 2 fields 010: 4 fields 011: 8 fields 100: 16 fields 101: 32 fields 110: 64 fields 111: 128 fields	0$_H$
	4:0	-	5	For test	For test Normally set to 0F$_H$	0F$_H$
50$_H$	5:4	-	2	For test	For test Normally set to 2$_H$	2$_H$
	3:0	-	4	For test	For test Normally set to 0$_H$	0$_H$
51$_H$ 52$_H$	6:0 7:0	I2A_NLTH	15	Noise detection threshold setting	Threshold value setting of noise detection	0C80$_H$
53$_H$	5:4	I2A_SELNTPAL	2	System detection select	System detection select 00: Both NTSC/PAL (Line number is distinguished.) 01: Only NTSC 10: Only PAL 11: Both NTSC/PAL	0$_H$
	2	I2A_AUTODET	1	System auto-detection ON/OFF setting	System auto-detection ON/OFF setting 0: OFF 1: ON	0$_H$
	0	I2A_NOSTDDET	1	Non-standard detection ON/OFF setting	Non-standard detection ON/OFF setting 0: OFF 1: ON	0$_H$
54$_H$	1:0	I2A_HSELFORMAT	2	System designation	Input signal system designation (It takes effect at I2A_AUTODET = 1'b0) 00: 576i 01: 480i 10: 576i (Non-standard) 11: 480i (Non-standard)	1$_H$
55$_H$	5	-	1	For test	For test Normally set to 0$_H$	0$_H$
	4	-	1	For test	For test Normally set to 0$_H$	0$_H$
	3:2	-	2	For test	For test Normally set to 0$_H$	0$_H$
	1:0	-	2	For test	For test Normally set to 3$_H$	3$_H$
56$_H$	6:4	-	3	For test	For test Normally set to 0$_H$	0$_H$
	2:0	-	3	For test	For test Normally set to 0$_H$	0$_H$
57$_H$	6:4	-	3	For test	For test Normally set to 5$_H$	5$_H$
	3	-	1	For test	For test Normally set to 1$_H$	1$_H$
	2	-	1	For test	For test Normally set to 0$_H$	0$_H$
	1:0	-	2		For test Normally set to 2$_H$	2$_H$

Continued from preceding page.

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
58$_H$	7:0	-	8	For test	For test Normally set to 0C$_H$	0C$_H$
59$_H$	5:0	-	6		For test Normally set to 32$_H$	32$_H$
5A$_H$	7:0	-	8		For test Normally set to F0$_H$	F0$_H$
5B$_H$	5:0	-	6		For test Normally set to 05$_H$	05$_H$
5C	7:0	-	8		For test Normally set to 28$_H$	28$_H$
5D$_H$	6:4	-	3		For test Normally set to 4$_H$	4$_H$
	2:0	-	3		For test Normally set to 3$_H$	3$_H$
5E$_H$	7:0	-	8		For test Normally set to 0A$_H$	0A$_H$
5F$_H$	7:6	-	2	For test	For test Normally set to 3$_H$	3$_H$
	5:4	-	2		For test Normally set to 3$_H$	3$_H$
	3:2	-	2		For test Normally set to 3$_H$	3$_H$
	1:0	-	2		For test Normally set to 3$_H$	3$_H$
60$_H$	7:6	-	2		For test Normally set to 3$_H$	3$_H$
	5:4	-	2		For test Normally set to 3$_H$	3$_H$
	3:2	-	2		For test Normally set to 3$_H$	3$_H$
	1:0	-	2		For test Normally set to 3$_H$	3$_H$
61$_H$	7:4	-	4	For test	For test Normally set to 0$_H$	0$_H$
	3:0	-	4		For test Normally set to 0$_H$	0$_H$
62$_H$ to 6F$_H$	-	-	-	-	-	-
70$_H$	1:0	-	10	For test	Read only	-
71$_H$	7:0					
72$_H$	0	NOSIG	1	No signal detection	No signal detection result Read only	-
73$_H$ to 74$_H$	-	-	-	-	-	-
75$_H$	7	NLDOUT	1	S/N detection	S/N detection result Read only	-
	6:0	NLDET	15		Noise level Read only	-
76$_H$	7:0					
77$_H$	0	-	1	For test	Read only	-
78$_H$	5:4	HSYSFORMAT	2	System detection	System detection result Read only	-
	1	-	1	For test	Read only	-
	0	-	1	For test	Read only	-

Continued from preceding page.

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
79H	3	DOUTH	1	Non-standard detection	Non-standard detection result (H) When non-standard is detected in field-blanking period 0: Normal 1: Special reproduction Read only	-
	2	DOUTH2	1		Non-standard detection result (H) 0: Standard 1: Non-standard Read only	-
	1	DOUTV	1		Non-standard detection result (V) 0: Standard 1: Non-standard Read only	-
	0	DOUTSTA	1		Stability judgment result 0: Stable 1: Unstable Read only	-
7AH	4:0	-	5	For test	Read only	-
7BH to 8AH	-	-	-	-	-	-
8BH	0	-	1	For test	For test Normally set to 0H	0H
8CH	0	-	1	For test	For test Normally set to 0H	0H
8DH	-	-	-	-	-	-
8EH	0	-	1	For test	For test Normally set to 0H	0H

BANK2 (Digital Video Signal Processing Block 2) Register Specification

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
00$_H$	7	-	1	For test	For test Normally set to 0$_H$	0$_H$
	6	I2BYC_SOFTRESET	1	Soft reset	Soft reset Y/C separation is initialized on the rising edge of the register clock	0$_H$
	5:3	I2BYC_SEL_FORMAT	3	Input switching setting	Input switching (It takes effect at I2BYC_INSEL[0] = 0) 000: NTSC 010: PAL-M 100: PAL 110: PAL-N xx1: SECAM	0$_H$
	2		1	For test	For test Normally set to 1$_H$	1$_H$
	1	I2BYC_INSEL	1	For test	For test Normally set to 1$_H$	1$_H$
	0		1	Input switching setting	Input switching setting 0: I2BYC_SEL_PAL[7:6] 1: INSEL(input port)	1$_H$
01$_H$	7:0	-	8	For test	For test Normally set to 16$_H$	16$_H$
02$_H$	7:0	-	2	For test	For test Normally set to 16$_H$	16$_H$
03$_H$	7:6	-	2	For test	For test Normally set to 3$_H$	3$_H$
	5		1		For test Normally set to 0$_H$	0$_H$
	4		1		For test Normally set to 1$_H$	1$_H$
	3:0		4		For test Normally set to 4$_H$	4$_H$
04$_H$	7:4	-	4	For test	For test Normally set to 4$_H$	4$_H$
	3		1		For test Normally set to 0$_H$	0$_H$
	2		1		For test Normally set to 0$_H$	0$_H$
	1		1		For test Normally set to 0$_H$	0$_H$
	0				For test Normally set to 0$_H$	0$_H$
05$_H$	7	I2BYC_2DCOMB2	1	For test	For test Normally set to 0$_H$	0$_H$
	6:5		2	Vertical high region line comb setting	Line comb vertical high region element BSF coefficient select 00: BSF1 01: BSF2 10: BSF3 11: BSF4	3$_H$
	4		1	For test	For test Normally set to 0$_H$	0$_H$
	3		1	Dot interference reduction setting	Dot interference reduction BSF 0: OFF 1: ON	1$_H$
	2		1	For test	For test Normally set to 1$_H$	1$_H$
	1:0		2		For test Normally set to 2$_H$	2$_H$
06$_H$	7:5	-	3	For test	For test Normally set to 2$_H$	2$_H$
	3		1		For test Normally set to 0$_H$	0$_H$
	1		1		For test Normally set to 0$_H$	0$_H$
	0		1		For test Normally set to 0$_H$	0$_H$

Continued from preceding page.

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
07H	7	I2BYC_2DCOMB4	1	For test	For test Normally set to 1H	1H
	6		1		For test Normally set to 1H	1H
	5		1		For test Normally set to 1H	1H
	4		1	Cross color reduction ON/OFF	Cross color reduction 0: OFF 1: ON	0H
	3		1	For test	For test Normally set to 1H	1H
	2		1		For test Normally set to 1H	1H
	1		1	For test	For test Normally set to 1H	1H
	0		1	For test	For test Normally set to 0H	0H
08H	7	-	1	For test	For test Normally set to 0H	0H
	6		1	For test	For test Normally set to 1H	1H
	5		1		For test Normally set to 1H	1H
	4		1		For test Normally set to 1H	1H
	3:2		2	For test	For test Normally set to 1H	1H
	1		1		For test Normally set to 1H	1H
	0		1		For test Normally set to 1H	1H
09H	7	-	1	For test	For test Normally set to 1H	1H
	6		1	For test	For test Normally set to 1H	1H
	5		1		For test Normally set to 1H	1H
0AH	7	I2BYC_2DCOMB8	1	One dimensional filter setting	Adaptive two dimensional filter enable/disable setting 0: Two dimensional 1: Adaptive two dimensional	1H
	6		1		For test Normally set to 1H	1H
	5		1		For test Normally set to 1H	1H
	4		1	For test	For test Normally set to 1H	1H
	3:2		2		For test Normally set to 3H	3H
	1		1		For test Normally set to 1H	1H
	0		1		For test Normally set to 1H	1H
0BH	7:4	-	4	For test	For test Normally set to 4H	4H
	3:0		4		For test Normally set to 4H	4H
0CH	7:4	-	4	For test	For test Normally set to 7H	7H
	3:0		4		For test Normally set to 8H	8H
0DH	7:0	-	8	For test	For test Normally set to 0CH	0CH
0EH	7:0	-	8	For test	For test Normally set to 14H	14H

Continued from preceding page.

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
0F$_H$	7:4	I2BYC_2DVENH	4	Vertical enhancer setting	Vertical enhancer gain setting 000: OFF 001: 2/8 times to 0111: 8/8 times to 1111: 16/8 times	0$_H$
	3:0		4		Vertical enhancer coring setting	0$_H$
10$_H$	7:0	-	8	For test	For test Normally set to 4B$_H$	4B$_H$
11$_H$	7	-	1	For test	For test Normally set to 0$_H$	0$_H$
	6		1		For test Normally set to 0$_H$	0$_H$
	5		1		For test Normally set to 0$_H$	0$_H$
	4		1		For test Normally set to 0$_H$	0$_H$
	2		1		For test Normally set to 0$_H$	0$_H$
	1		1		For test Normally set to 0$_H$	0$_H$
	0		1		For test Normally set to 0$_H$	0$_H$
12$_H$	7	-	1	For test	For test Normally set to 0$_H$	0$_H$
	6		1		For test Normally set to 0$_H$	0$_H$
	5		1		For test Normally set to 0$_H$	0$_H$
	4		1		For test Normally set to 0$_H$	0$_H$
	2		1		For test Normally set to 0$_H$	0$_H$
	1		1		For test Normally set to 0$_H$	0$_H$
	0		1		For test Normally set to 0$_H$	0$_H$
13$_H$	7	-	1	For test	For test Normally set to 0$_H$	0$_H$
	5		1		For test Normally set to 0$_H$	0$_H$
	4		1		For test Normally set to 0$_H$	0$_H$
	3		1		For test Normally set to 0$_H$	0$_H$
	2		1		For test Normally set to 0$_H$	0$_H$
	1		1		For test Normally set to 1$_H$	1$_H$
	0		1		For test Normally set to 1$_H$	1$_H$
14$_H$	0	-	1	For test	For test Normally set to 0$_H$	0$_H$

Continued from preceding page.

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
15$_H$	7	-	1	For test	For test Normally set to 0$_H$	0$_H$
	6		1	For test	For test Normally set to 0$_H$	0$_H$
	5:4		2	For test	For test Normally set to 0$_H$	0$_H$
	3		1		For test Normally set to 0$_H$	0$_H$
	2		1		For test Normally set to 0$_H$	0$_H$
	1		1		For test Normally set to 0$_H$	0$_H$
16$_H$	7:4	I2BYC_1DFIL	4	One dimensional BPF select	One dimensional BPF select 000: BPF0 to 1011: BPF11	4$_H$
	3:1		3	BPF for SECAM select	One dimensional BPF select for SECAM 000: BPF0 to 111: BPF7	2$_H$
	0		1	One dimensional filter ON	One dimensional filter ON/OFF setting 0: Line comb filter 1: One dimension filter	0$_H$
17$_H$ to 1F$_H$	-	-	-	-	-	-
20$_H$	7:0	-	8	For test	For test Normally set to 2C$_H$	2C$_H$
21$_H$	5	-	1	For test	For test Normally set to 0$_H$	0$_H$
	4	-	1	For test	For test Normally set to 1$_H$	1$_H$
	3	-	1	For test	For test Normally set to 1$_H$	1$_H$
	2:0	-	3	For test	For test Normally set to 0$_H$	0$_H$
22$_H$ to 25$_H$	-	-	-	-	-	-
26$_H$	7:0	I2BCD_UGAIN	8	Cb gain setting	Gain control of Cb signal	80$_H$
27$_H$	7:0	I2BCD_VGAIN	8	Cr gain setting	Gain control of Cr signal	80$_H$
28$_H$	-	-	-	-	-	-
29$_H$	4:3	-	2	For test	For test Normally set to 0$_H$	0$_H$
	2:0	-	3	For test	For test Normally set to 0$_H$	0$_H$
2A$_H$	7:0	-	8		For test Normally set to 80$_H$	80$_H$
2B$_H$	-	-	-	-	-	-
2C$_H$	7:0	-	8	For test	For test Normally set to 80$_H$	80$_H$
2D$_H$ to 2F$_H$	-	-	-	-	-	-
30$_H$	3	-	1	For test	For test Normally set to 0$_H$	0$_H$
	2	I2BAC_ SW_ACC_NTPAL	1	ACC NTSC/PAL setting	0: NTSC = 286LSB 1: PAL = 300LSB (when ACC_BSTLV is center value)	0$_H$
	1:0	I2BAC_ACC_ON	2	ACC ON	ACC ON/OFF setting 00: OFF 01: ON 1x: Gain fix	1$_H$
31$_H$	7:0	I2BAC_ ACC_BSTLV	8	ACC setting	ACC target value setting 158 to 413LSB	80$_H$
32$_H$	3:0	I2BAC_ ACC_TIMCON	4		Maximum value of time constant, characteristics select Setting range: 1 time to 16 times	3$_H$
33$_H$	1:0	-	2	For test	For test Normally set to 0$_H$	0$_H$

Continued from preceding page.

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
34H	3:0	I2BAC_CKILL_ON	4	Color killer setting	Color killer ON/OFF setting 0000: OFF 0001: ON by APC 0010: ON by ACC 0011: ON by APC + ACC 0100: ON at the time of noncompliant signal input 0101: ON by APC and at the time of noncompliant signal input 0110: ON by ACC and at the time of noncompliant signal input 0111: ON by APC + ACC and at the time of noncompliant signal input 1xxx: Forced ON	7H
35H	4:0	I2BAC_CKILL_LV	5		Threshold value killer is turned on by burst-amplitude	3H
36H	4:0	I2BAC_CKILL_HYST	5		Threshold value killer is turned off by burst-amplitude	0H
37H	1:0	-	2	For test	For test Normally set to 1H	1H
38H to 3AH	-	-	-	-	-	-
3BH	4:0	-	5	For test	For test Normally set to 0H	0H
3CH	2:0	-	3		For test Normally set to 0H	0H
3DH	1:0	-	2	For test	For test Normally set to 0H	0H
3EH	4:0	I2BAC_ACC_SELAMP	5	ACC setting	Gain setting at ACC_ON = 2'b1x Setting range: -6 to 32dB	0H
3FH	-	-	-	-	-	-
40H	5	-	1	For test	For test Normally set to 1H	1H
	4	-	1	For test	For test Normally set to 0H	0H
	3:0	I2BSE_BELLF0	4	Bell filter setting	Bell filter f0 select	8H
41H	7:4	I2BSE_BELLQ	4		Bell filter Q select	8H
	3:2	I2BSE_BELLAMP	2		Bell filter amplifier select 0: 1 time 1: 2 times	1H
42H	2	-	1	For test	For test Normally set to 1H	1H
	1:0	I2BSE_CLPFSEL	2	LPF setting after FM demodulation	LPF select after FM demodulation	2H
43H	5:0	-	6	For test	For test Normally set to 28H	28H
44H	7:0	-	8		For test Normally set to 40H	40H
45H	3:2	-	2		For test Normally set to 3H	3H
	1:0	-	2		For test Normally set to 3H	3H

Continued from preceding page.

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
46$_H$	6:4	-	3	For test	For test Normally set to 1$_H$	1$_H$
	3	-	1		For test Normally set to 1$_H$	1$_H$
	2:1	-	2		For test Normally set to 3$_H$	3$_H$
	0	-	1		For test Normally set to 0$_H$	0$_H$
47$_H$	5:0	-	6	For test	For test Normally set to 1$_H$	1$_H$
48$_H$	3:0	-	4		For test Normally set to 1$_H$	1$_H$
49$_H$	6:0	-	7		For test Normally set to 40$_H$	40$_H$
4A$_H$	6:0	-	7		For test Normally set to 40$_H$	40$_H$
4B$_H$	5:0	-	6	For test	For test Normally set to 3$_H$	3$_H$
4C$_H$	5:0	-	6	For test	For test Normally set to A$_H$	A$_H$
4D$_H$ to 4F$_H$	-	-	-	-	-	-
50$_H$	2	-	1	For test	For test Normally set to 1$_H$	1$_H$
	1	-	1		For test Normally set to 0$_H$	0$_H$
	0	-	1		For test Normally set to 0$_H$	0$_H$
51$_H$	7:0	I2BSE_UGAIN	8	SECAM chroma adjustment	Cb/Cr gain control 0 to 3.984375 0 = 0 64 = 1 128 = 2 255 = 3.984375	80$_H$
52$_H$	7:0	I2BSE_VGAIN	8			80$_H$
53$_H$	7:0	I2BSE_UOFFSET	8		Cb/Cr offset adjustment -128 to 127 0 = -128 128 = 0 255 = 127	80$_H$
54$_H$	7:0	I2BSE_VOFFSET	8			80$_H$
55$_H$	5	-	1	For test	For test Normally set to 0$_H$	0$_H$
	4:3	I2BSE_DEIIR	2	De-emphasis filter setting	De-emphasis filter select	0$_H$
	2:0	-	3	For test	For test Normally set to 0$_H$	0$_H$
56$_H$ to 5F$_H$	-	-	-	-	-	-
60$_H$	7:0	-	8	For test	For test Normally set to F$_H$	F$_H$
61$_H$	7:0	-	8	For test	For test Normally set to 64$_H$	64$_H$

Continued from preceding page.

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
62H	7	-	1	For test	For test Normally set to 0H	0H
	6		1	For test	For test Normally set to 1H	1H
	5		1	For test	For test Normally set to 0H	0H
	4		1	For test	For test Normally set to 0H	0H
	3		1	For test	For test Normally set to 0H	0H
63H	-	-	-	-	-	-
64H	7	I2BCV_TVMODE	1	For test	For test Normally set to 0H	0H
	6		1	For test	For test Normally set to 0H	0H
	3		1	TV mode select	0: Auto setting 1: Manual setting with TVMODE[2: 0]	0H
	2		1	Frequency select	0: 50Hz (625 lines) 1: 60Hz (525 lines)	0H
	1:0		2	System setting	0: NTSC 1: PAL-M 2: PAL 3: PAL-N	0H
65H	7:6	-	2	For test	For test Normally set to 0H	0H
	2:0		3	For test	For test Normally set to 1H	1H
66H	-	-	-	-	-	-
67H	7:6	-	2	For test	For test Normally set to 0H	0H
	5		1	For test	For test Normally set to 0H	0H
	4		1	For test	For test Normally set to 0H	0H
	3:1		3	For test	For test Normally set to 0H	0H
	0		1	For test	For test Normally set to 0H	0H
68H to 69H	-	-	-	-	-	-
6AH	7:0	-	8	For test	For test Normally set to 10H	10H
6BH to 70H	-	-	-	-	-	-
71H	5:0	I2BSR_GAIN	6	Sub contrast/ brightness setting	Contrast adjustment	20H
72H	5:0	I2BSR_OFST	6		Brightness adjustment	20H
73H to 7BH	-	-	-	-	-	-
7CH	1	-	1	For test	For test Normally set to 0H	0H
	0	I2BSR_SETUP	1	Setup	Setup processing	1H
7DH to 7FH	-	-	-	-	-	-
80H	0	-	1	For test	For test Normally set to 1H	1H
81H	0	-	1		For test Normally set to 0H	0H
82H to 9FH	-	-	-	-	-	-

Continued from preceding page.

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
A0$_H$	2:0	-	3	For test	For test Normally set to 0$_H$	0$_H$
A1$_H$	2:0	-	3		For test Normally set to 0$_H$	0$_H$

| | | | | | For test
Normally set to 0$_H$ | |

BANK3 (Digital Video Signal Processing Block 3) Register Specification

Sub-address	Bit	Name	Bit-Size	Function Name	Functions	Initial value
00$_H$	2	I2DSH_LPFOFF	1	Sharpness setting	Sharpness LPF ON/OFF setting 0: ON 1: OFF	0$_H$
	1	-	1	For test	For test Normally set to 0$_H$	0$_H$
	0	I2DSH_ON	1		Sharpness ON/OFF setting 0: OFF 1: ON	0$_H$
01$_H$	5:0	I2DSH_ATT	6	Sharpness setting	Sharpness ATT value setting Setting range: -47.5 to 12dB	10$_H$
02$_H$	2:0	I2DSH_CORR	3		Sharpness coring threshold	0$_H$
03$_H$	3:0	I2DSH_FILTER	4		Sharpness characteristic select	1$_H$
04$_H$	2	-	1	For test	For test Normally set to 0$_H$	0$_H$
	1	-	1		For test Normally set to 0$_H$	0$_H$
	0	-	1		For test Normally set to 1$_H$	1$_H$
05$_H$	0	-	1	For test	For test Normally set to 0$_H$	0$_H$
06$_H$	7:0	I2DCB_CONT	8	Contrast/ Brightness setting	Contrast adjustment	80$_H$
07$_H$	7:0	I2DCB_BRIGHT	8		Brightness adjustment	80$_H$
08$_H$	6:0	I2DHU_HUE	7	HUE setting	HUE adjustment	40$_H$
09$_H$	7:0	I2DUV_UGAIN	8	U/V gain setting	Cb gain control	B4$_H$
0A$_H$	7:0	I2DUV_VGAIN	8		Cr gain control	B4$_H$
0B$_H$ to 0E$_H$	-	-	-	-	-	-
0F$_H$	1:0	-	2	For test	For test Normally set to 1$_H$	1$_H$
10$_H$	3:1	I2DCT_SMP	3	CTI setting	CTI correction tap coefficient	0$_H$
	0	I2DCT_CTIEN	1		CTI ON/OFF setting 0: OFF 1: ON	0$_H$
11$_H$	7:4	I2DCT_CORR	4		CTI Coring threshold	0$_H$
	3:0	I2DCT_GAIN	4		CTI gain GAIN=C_GAIN/8 (0 ≤ C_GAIN ≤ 15)	6$_H$
12$_H$	7:4	-	4	For test	For test Normally set to 0$_H$	0$_H$
	3:0	-	1		For test Normally set to 0$_H$	0$_H$
13$_H$	5:4	I2D65_AUTOBBACK	2	656 conversion setting	No signal output mode 00: Black background 01: Blue background 10: OFF 11: BL	0$_H$
	3	I2D65_SEPIA	1		0: Normal output 1: Sepia output	0$_H$
	2	I2D65_601LIM	1		0: Signal level 1 to 254 1: Y level 16 to 235, C level 16 to 240	0$_H$
	1	I2D65_AVOFF	1		0: 656 with SAV,EAV 1: No SAV, EAV	1$_H$
	0	-	1	For test	For test Normally set to 0$_H$	0$_H$
14$_H$ to 1F$_H$	-	-	-	-	-	-
20$_H$	1:0	-	2	For test	For test Normally set to 0$_H$	0$_H$
21$_H$	1:0	-	2		For test Normally set to 0$_H$	0$_H$

Function Descriptions

1. CPU I/F
   The LC749870W registers are controlled by I^2C.

1) I^2C
   The LC749870W supports high-speed mode slave operation (400 kHz) and the slave address is as follows.

bit[7] (MSB)	bit[6]	bit[5]	bit[4]	bit[3]	bit[2]	bit[1]	bit[0] (LSB)
1	0	0	0	1	0	I^2CSEL	R/W

   *Note: The bit 1 is decided according to the I^2CSEL pin condition.
   bit 0 R/W: 0 = write, 1 = read

■Write Mode
• Auto address increment.
• As shown below, after the start condition, the settings must be made in the following order: slave address (W), ACK waiting, write start sub address, ACK waiting, write data. The stop condition must be set last. Data can be transmitted continuously from the write start sub address using the auto address increment function.

   [ST] [Slave Address(W)] [A̲] [Sub address] [A̲] [Data] [A̲] [Data] • • • [SP]

■Read Mode
• Auto address increment.
• The read start sub address must be assigned in write mode.
• As shown below, after the start condition, first set the slave address (W), ACK waiting and read start sub address. Next, set the start condition again or set the start condition after setting the stop condition. Next set the slave address (R) and ACK waiting in read mode. The data for each sub address is output continuously from the read start sub address data using the auto address increment function. After receiving the data for each sub address, return the ACK. Finally, set the stop condition.

   [ST] [Slave Address (W)] [A̲] [Sub address] [ST] [Slave Address(R)] [A̲] [Data̲] [A] [Data̲] [A] [Data̲] • • • [SP]

   or

   [ST] [Slave Address (W)] [A̲] [Sub address] [SP] [ST] [Slave Address(R)] [A̲] [Data̲] [A] [Data̲] [A] [Data̲] • • • [SP]

   [ST]: Start condition
   [SP]: Stop condition
   [A]: ACK
   [A̲]: ACK waiting
   [Data]: Data transmission
   [Data̲]: Data reception

2) BANK

Each register is allocated to the BANK depending on its function (Refer to Table 1). After the BANK is specified, the register can be controlled. The BANK is specified by setting the BANK code to sub address FF_H. Note that the register cannot be transmitted or received if codes other than the BANK codes in Table1 are specified.

Table 1 Allocation of BANK

BANK	BANK Code	Controlled Function
0	01_H	AFE + ADC
1	02_H	Digital video signal processing block 1 (Data interpolator, APC, AGC, digital clamp, sync separator, timing generator, video system detection, S/N detection, non-standard signal detection, No-signal detection)
2	04_H	Digital video signal processing block 2 (Y/C separator, color demodulator, clock rate converter)
3	08_H	Digital video signal processing block 3 (Sharpness, contrast/brightness, CTI, HUE, UV gain)

• Auto address increment.

[ST] [Slave address (W)] [A] [FF$_H$] [A] [BANK Code] [SP]

[ST]: Start condition
[SP]: Stop condition
[A]: ACK
[Data]: Data transmission

2. AFE and ADC
   This IC (LC749870W) incorporates 1-channel of video AFE and 10-bit 30MHz ADC.

• Analog clamp (Self-clamp circuit)
  The self clamp circuit clamps the sync-tip without supplying clamp pulses to AFE module. When the self-clamp function is not used, it can be placed in power down mode using $I^2C\_SELFCLPPWDB$.

• Sync-tip clamp specifications

Analog input	Digital output	ADC output code

```
1.55V ─────────────────────────────────────── 1023
1.35V ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ 878
          1.0Vp
0.85V
(ADC-input reference) ────────────────────────── 512
0.65V ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ 356

0.35V ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ ─ 147
0.15V ─────────────────────────────────────── 1
```

1.4Vp-p range
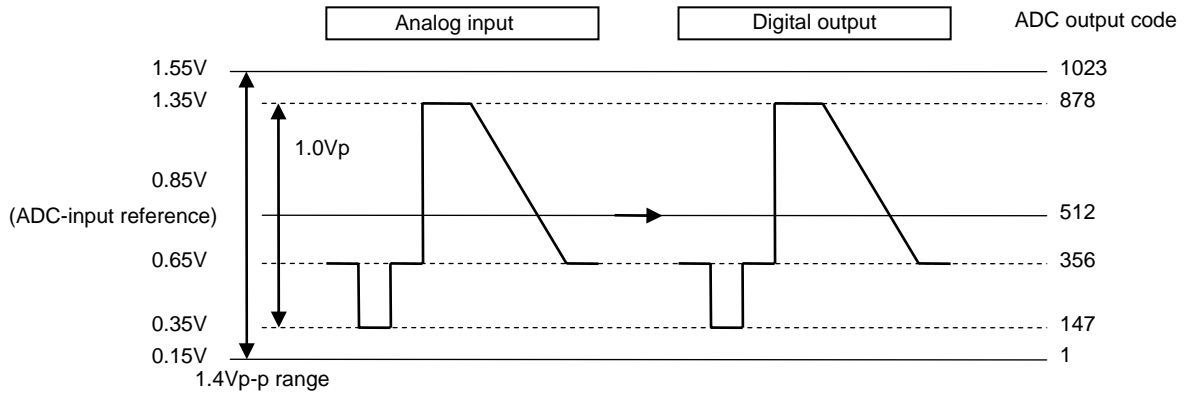
* The figures represent the values under ideal conditions.

Clamp Setting

Self Clamp Setting
SELFCLPPWDB   1: Self Clamp enable

Main Clamp Level Setting
MAINCLPLVCNT [1:0]   00: Main Clamp Level 0.35V

• Low pass filter before self-clamp
  A primary LPF with a 1MHz cutoff frequency has been inserted in the stage before the self-clamp circuit as a measure to deal with the high-frequency noise that is present in weak electric fields. The LPF function is for minimizing shifts in the clamp levels of the self-clamp when high-frequency noise components are present in the video signals. The LPF can be set to ON or OFF using $I^2C\_CLPLPFON$.

Input video signal (SD)	Sync tip clamp when LPF is OFF	Sync tip clamp when LPF is ON

High frequency noise of 1MHz or more

0V

0.35V

Clamping is performed at the lower limit level of the noise components. Due to the effect of the noise, the clamp level shifts.

Clamping is performed at the level at which the noise components are removed.
It is clamped at its original position.
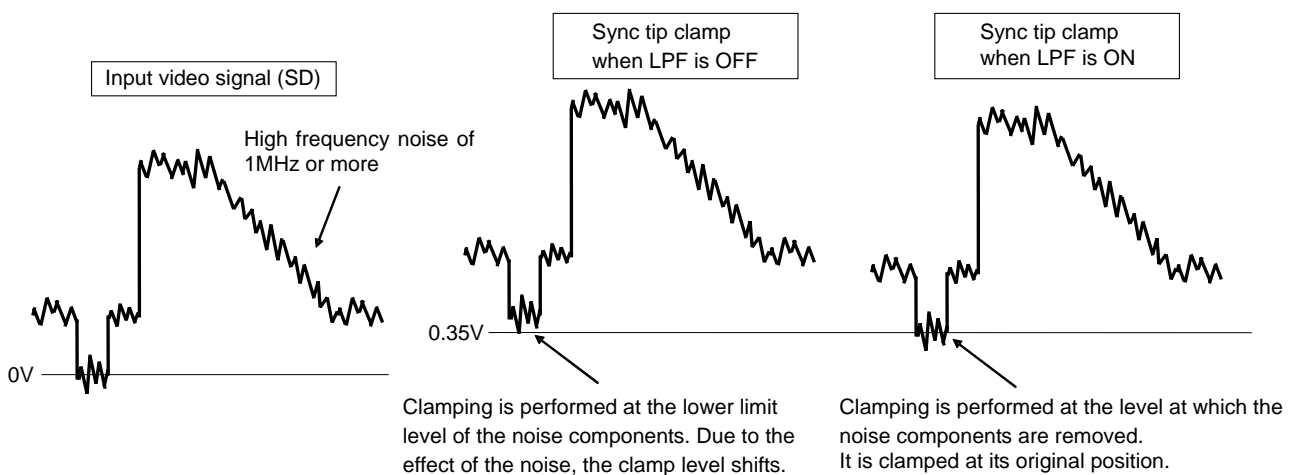
Fig.1 Self Clamp in Weak Electric Fields

• AGC Mode and Non-AGC Mode

Switch between non-AGC mode and AGC mode using I^{2}C_SCARTON.

Non-AGC mode is used when the amplitude of the video signal is steady in the environment of a strong electric field. The maximum of the sync tip clamped analog video input amplitude assumes 1.0Vp-p in non-AGC mode. The ADC full-scale input range is fixed at 1.4Vp-p.

AGC mode is used when the amplitude of the video signal is unsteady in the environment of a weak electric field. The maximum of the sync tip clamped analog video input amplitude assumes a value no greater than from 0.7Vp-p (-3dB) to 1.4Vp-p (+3dB) in AGC mode. Because the AFEVRTC is controlled according to the amplitude of SYNC detected by the decoder, AGC mode is enabled by varying the ADC full-scale input range.

3. Data Interpolator

Data interpolator converts the input video signal sampled at 27MHz into 4fsc data. Supported video systems are shown in the following table.

Table 2: Supported Video System

| Video System | Input | Output | |
	Sampling clock	Data transfer rate	Clock lock method
NTSC	27MHz	14.318180MHz	Burst Lock
PAL-B, G, D, K, I	27MHz	17.734476MHz	Burst Lock
PAL-M	27MHz	14.302444MHz	Burst Lock
PAL-N	27MHz	14.328224MHz	Burst Lock
NTSC4.43	27MHz	17.734476MHz	Burst Lock
PAL-60	27MHz	17.734476MHz	Burst Lock
SECAM	27MHz	13.5MHz	H Lock

4. APC (Auto Phase Control)

In order to burst lock input video signals, the APC circuit detects the color burst phase error. The data interpolation coefficient is calculated using the detected phase error, and is then output to the data interpolator circuit. It is equipped with a function to turn on the color killer when not burst-locked, and also has an ACC circuit to maintain the amplitude of the carrier chrominance signal at a constant level.

5. AGC (Auto Gain Control)

The AGC keeps the sync level constant by automatically calculating an appropriate gain value from the input video signal sync level and amplifying the input video signal. Because the AGC circuit includes a time constant circuit, following rapid changes in the input video signal can be suppressed.
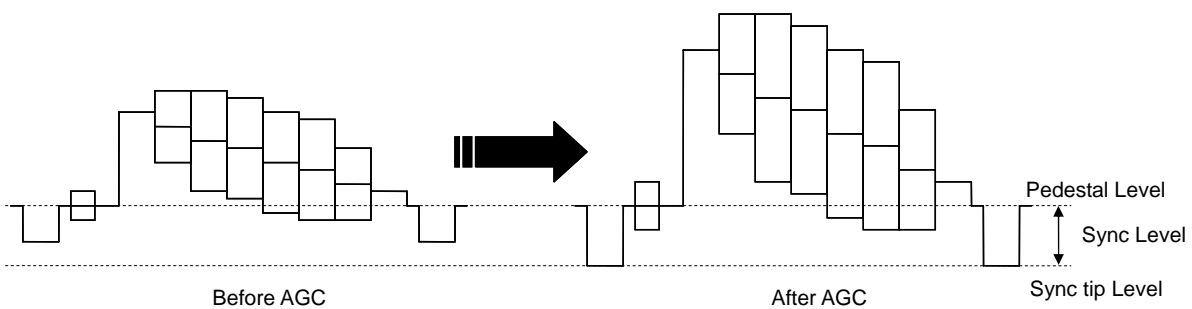
Fig.2 Waveform Change Before and After AGC

6. Digital Clamp

The digital clamp circuit detects the pedestal level of the input video signal, and keeps the level constant. Because the digital clamp includes a time constant circuit, following rapid changes in the input video signal can be suppressed.
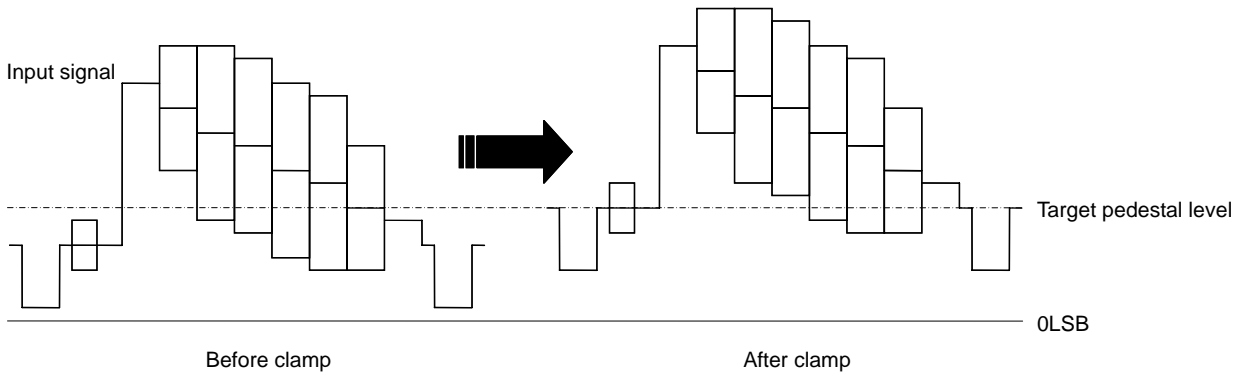
Fig.3 Waveform Change Before and After Digital Clamp

7. Sync Separator

The sync separator circuit separates horizontal and vertical sync signals out of the input video signals. Because an LPF is built in, the sync signal can be separated even in a weak electric field. The weak electric field is detected using the S/N detection result. Moreover, the stability of the sync signal in the weak electric field is improved by the internal AFC circuit. Fig. 4 shows the LPF characteristics for the sync separator. "FILSEL = 1'b0" is the characteristic of an LPF for a weak electric field, and "FILSEL = 1'b1" is the characteristic of an LPF for a strong electric field.
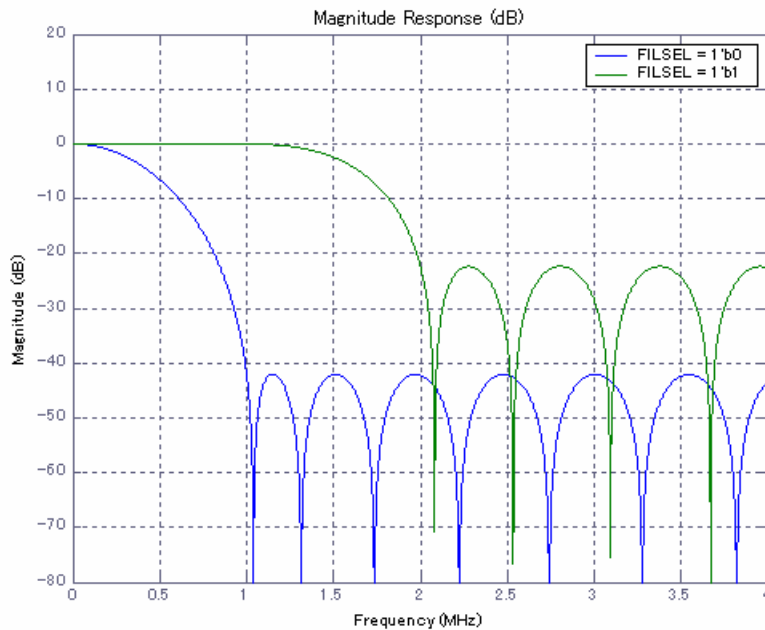
Fig.4 LPF Characteristic for Sync Separator

8. Timing Generator

Using the sync signal separated by the sync separator circuit, the timing generator generates various timing signals to be used for each module as well as for horizontal and vertical blanking signals.
The adjustments of timing signals are possible by setting the corresponding register (s) as follows:
Positioning of horizontal sync signal: I2A_HSPAD
Positioning of vertical sync signal: I2A_VSTART
Positioning of horizontal blanking signal: I2A_HBSTART, I2A_HBEND
Positioning and width adjustment of vertical blanking signal: I2A_VBSTART, I2A_VBWIDTH

9. Two-dimensional Y/C Separation

The Y/C separator switches adaptive two-dimensional Y/C separation and one-dimensional Y/C separation according to the input video system. The table below shows the relationship between input video system and Y/C separation method.

Table 3 Relationship Between Input Video System and Y/C Separation Method

Video System	Y/C Separation Filter
NTSC	Adaptive two-dimensional Y/C separation
NTSC-4.43	One-dimensional Y/C separation
PAL-B, G, D, K, I, M, N	Adaptive two-dimensional Y/C separation
PAL-60	One-dimensional Y/C separation
SECAM	One-dimensional Y/C separation

1) Adaptive Two-dimensional Y/C Separation

The correlation between lines is detected in the vertical LPF and BPF, and the system switches between upper two line processing and lower two or three line processing, based on the results. The adaptive two-dimensional Y/C separation and two-dimensional Y/C separation can be switched using I2BYC_2DCOMB8 [7]. Note that the Y/C separation filter is switched to one-dimensional Y/C separation when I2BYC_1DFIL [0] is set to 1'b1 (I2BYC_1DFIL [0] = 1'b1).

- Y signal = (Vertical low frequency component) + (Horizontal low frequency component of vertical high frequency component)
- C signal = Horizontal high frequency component of vertical high frequency component
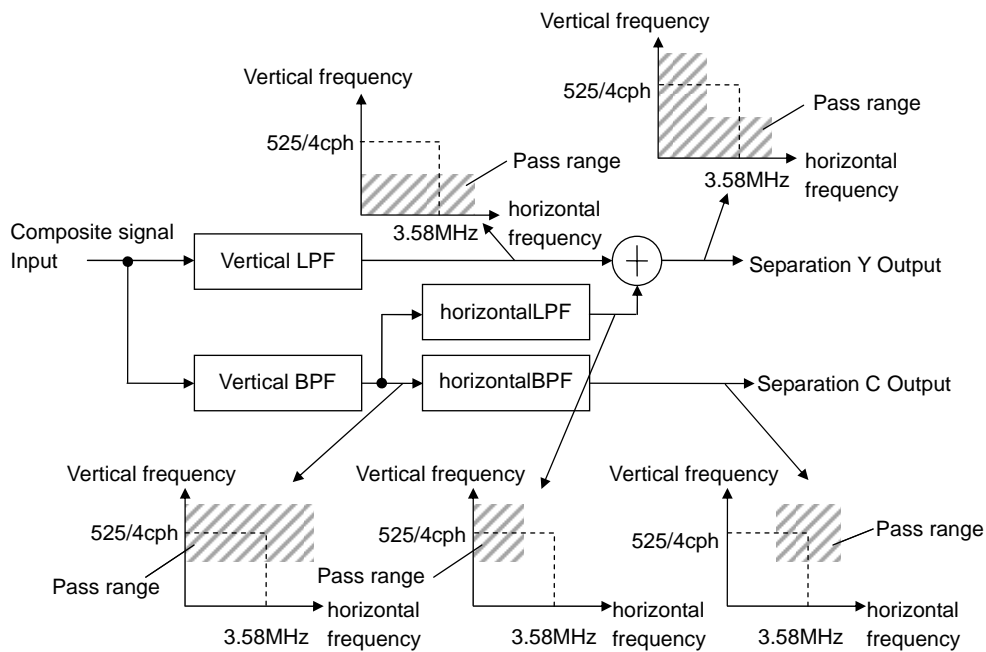
Fig.5 Basic Block Diagram of Two-dimensional Y/C Separation (Line Comb Filter)

- 1 Line Chroma Detector

When 1 line chroma is separated with the two-dimensional Y/C separation, the dot interference is generated because there is no correlation between lines. Therefore, 1 line chroma is detected and dot interference reduction is attempted by subtracting chroma components.

When the following conditions exist, it is judged to be 1 line chroma.

(1) No chroma changes in the line (horizontal direction).
(2) Chroma changes between lines (vertical direction).
(3) Luminance changes between lines (vertical direction).

- 3 Line Median Processing

When the vertical color in the DVD color bar changes and blurs, dot interference may be generated. Dot interference reduction is attempted by detecting this location and removing the chroma components.
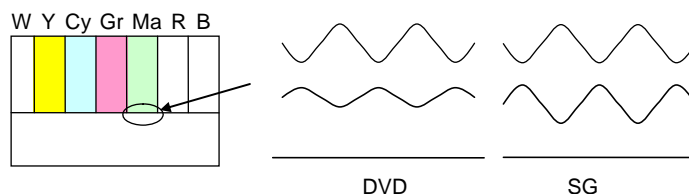
Fig.6 Dot interference

When the following conditions exist as a result of comparing the BPF values for each line, the chroma components must be removed.
(1) When there is a match between the median value of each line and the pixel of the line at the center.
(2) When there is a change between lines.

- Y Signal Bypass Processing

If the chroma band component of the separated Y signal is compared with the chroma band component of the signal before separation, and if the chroma band of the signal before separation is smaller, the signal is output as a Y signal.

- C Signal Bypass Processing

If a C signal processed by the comb filter is compared with the result processed by the BPF, and if the result of the BPF is smaller, the BPF processing result is output as a C signal.

- Dot Interference Reduction

The line comb filter need not add HLVH[*1] to the Y signal if there is a complete line correlation, such as with the Color Bar. Such an addition will only increase the dot interference shown in Fig. 6 above. Therefore, when a location with strong line correlation is detected, the horizontal BSF pass band of HLVH to be added to the Y signal is narrowed, and the dot interference is reduced. The dot interference reduction BSF can be set to ON or OFF using I2BYC_2DCOMB2[3].

*1: Horizontal low frequency component of vertical high frequency component

- Cross Color Reduction

When a location with weak line correlation is detected, the BPF pass band in the subsequent stage of the C signal is narrowed, and the cross color is reduced. cross color reduction can be set to ON or OFF using I2BYC_2DCOMB4 [4].

2) One-dimensional Y/C separation (BPF)

Y/C separation is performed by using BPF. The BPF characteristics for NTSC/PAL and for SECAM are selected by I2BYC_1DFIL [7:1]. It is forced to one-dimensional Y/C separation when I2BYC_1DFIL [0] is set to 1'b1 (I2BYC_1DFIL [0] = 1'b1). When performing adaptive two-dimensional Y/C separation, I2BYC_1DFIL [0] must be set to 1'b0 (I2BYC_1DFIL [0] = 1'b0) . Fig.7 and 8 show the characteristics of BPF.
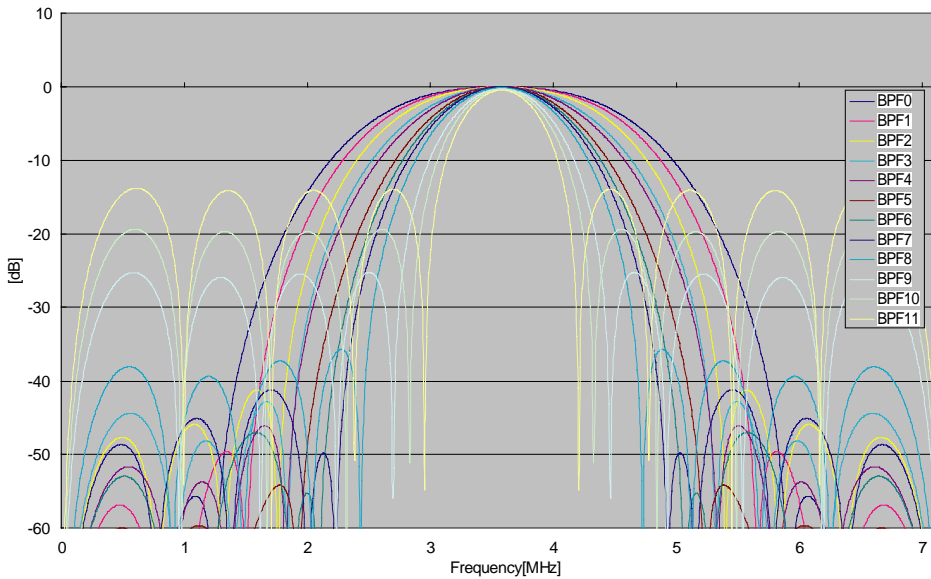
Fig.7 BPF Characteristic for NTSC/PAL
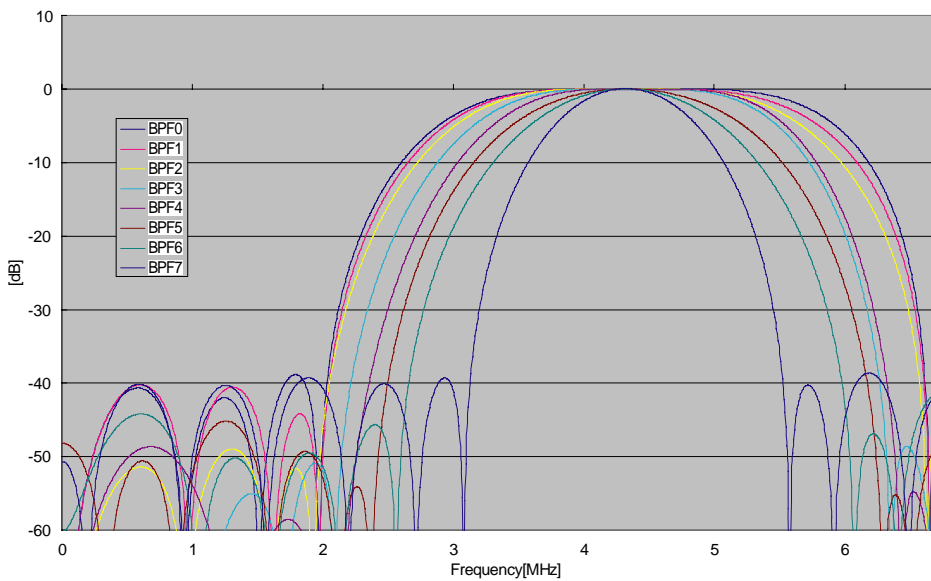
Fig.8 BPF characteristic for SECAM

10. Chrominance Signal Processing

In chrominance signal processing, U/V axial demodulation is performed on the carrier chrominance signal after Y/C separation, and the UV signal is output.

1) ACC (Auto Color Control)

ACC maintains a constant carrier chrominance signal amplitude for NTSC and PAL. The amplitude is kept constant by observing the color burst amplitude of the input carrier chrominance signal, and controlling the amplifier according to the amplitude level. It can also turn on the color killer when the color burst amplitude is small. I2BAC_ACC_ON switches between ACC ON and OFF.

2) Color Killer

The color killer masks the carrier chrominance signal so that a monochrome image is output. When entering the detection results from APC or ACC circuits or an incompatible signal, the color killer is turned on and off. The color killer can be set using I2BAC_CKILL_ON.

3) NTSC/PAL Color Decoder

The NTSC/PAL color decoder demodulates the carrier chrominance signal into color component signals (U/V).

- Color Demodulator and Low Pass Filter
  The Cb/Cr signal is demodulated by multiplying the chrominance signal and phase-controlled color sub-carrier (4Fsc). Fig. 9 shows the block diagram.
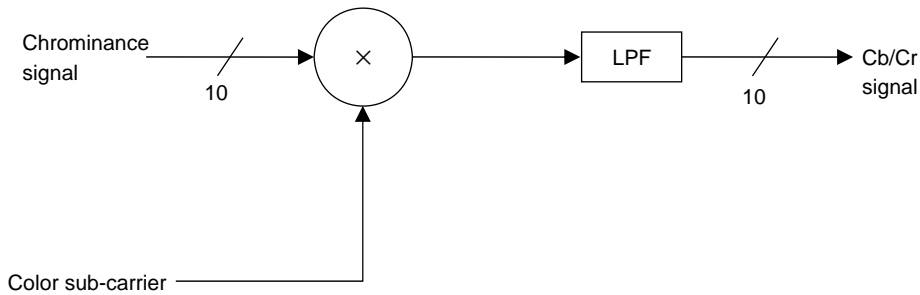
Fig.9 Color Demodulator

The LPF characteristic after demodulation is shown in Fig.10.
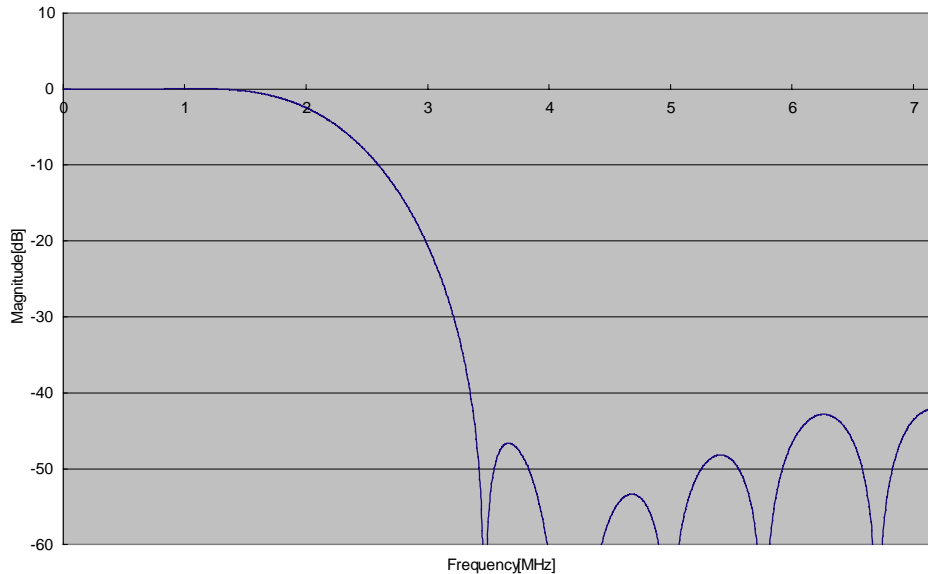
Fig.10 LPF Characteristic after Demodulation

- UVGAIN (Cb/Cr Gain Control)
  The UVGAIN adjustment changes the Cb/Cr signal gain based on a center value. Fig.11 shows the block diagram.
  The gain can be controlled using I2BCD_UGAIN and I2BCD_VGAIN.
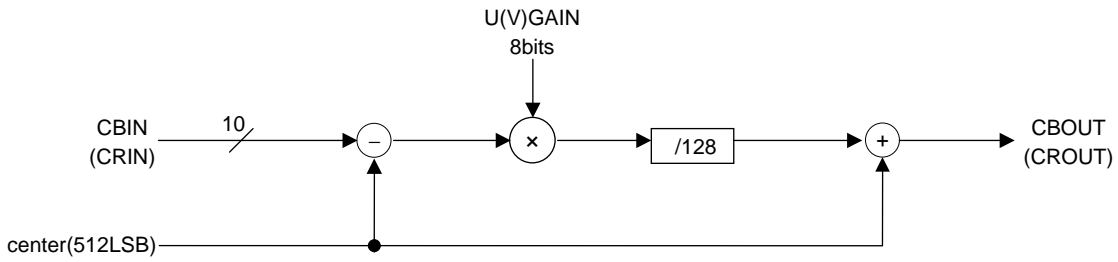
Fig.11 UVGAIN Block Diagram

4) SECAM Color Decoder
  The SECAM color decoder demodulates the carrier chrominance signal into color difference signals (U/V).

- Bell Filter
  The bell filter is used to maintain the color sub-carrier amplitude of the Y/C-separated chrominance signal constant.
  The f0 parameter can be selected using I2BSE_BELLF0, and the Q parameter using I2BSE_BELLQ.
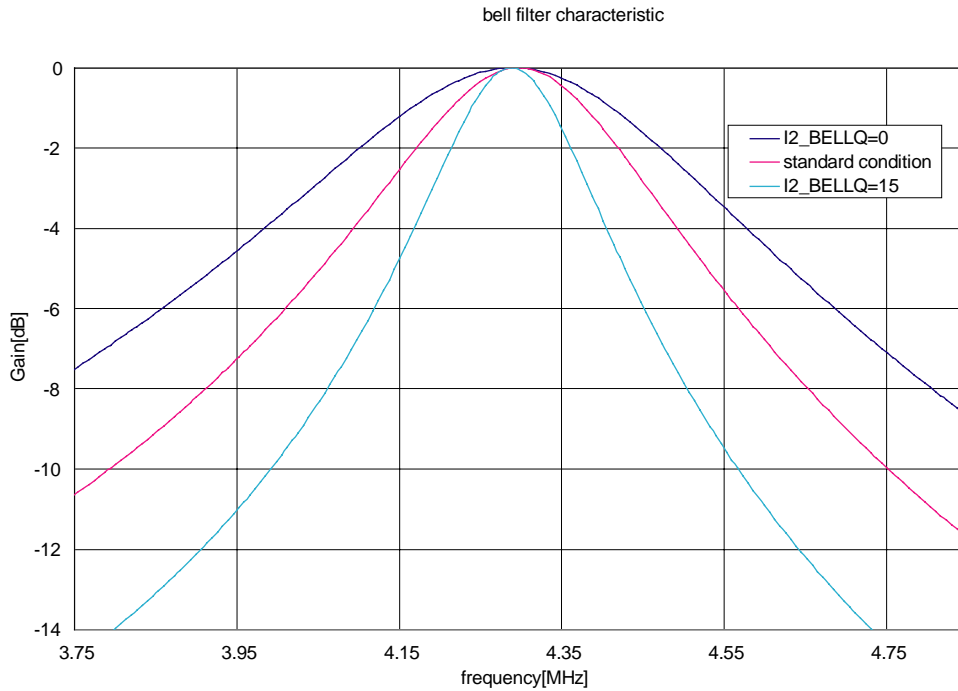
Fig.12 Bell Filter characteristics

- Low Pass Filter
  The LPF is used to reduce noise in FM demodulated DB/DR signals. The characteristics of the LPF can be selected using I2BSE_CLPFSEL.

LPF characteristic
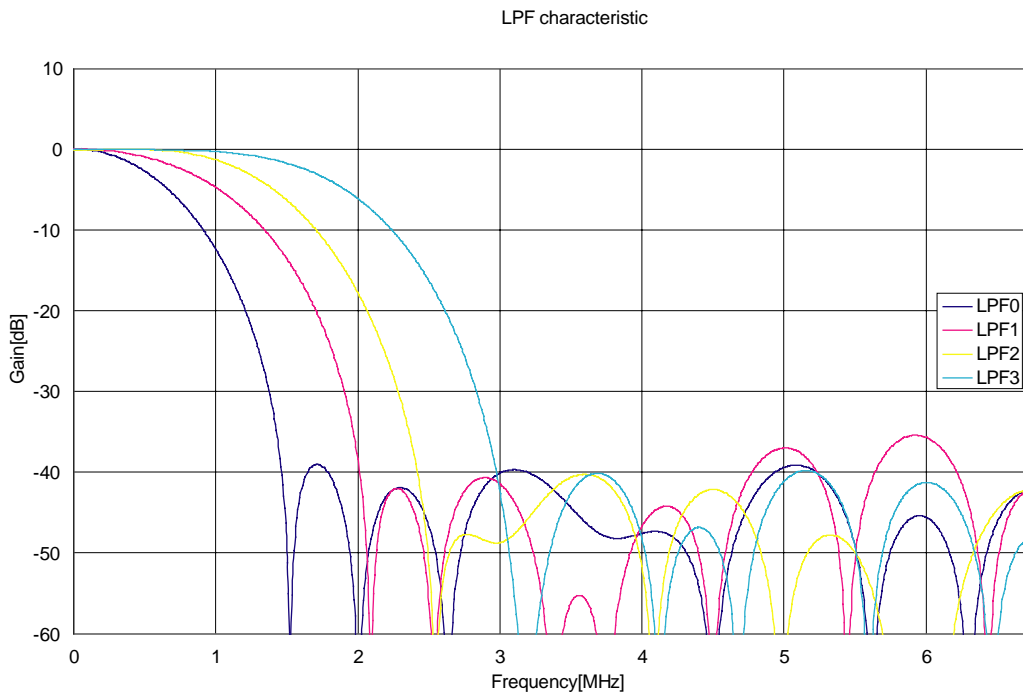
Fig.13 LPF Characteristics

- UV Gain and Offset Adjustment
  The UV gain adjustment is performed to convert DB/DR to CB/CR, and the UV offset fine adjustment is also performed. The UV gain can be adjusted by changing I2BSE_UGAIN and I2BSE_VGAIN, and the UV offset can be adjusted by I2BSE_UOFFSET and I2BSE_VOFFSET.
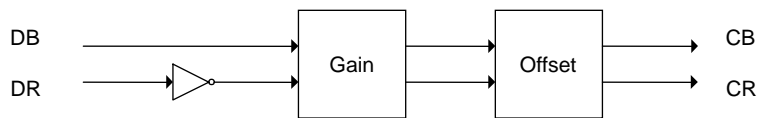
Fig.14 UV Gain and Offset Adjustment

- De-emphasis Filter
  The de-emphasis filter characteristics can be selected using I2BSE_DEIIR.

de-emphasis filter characteristic
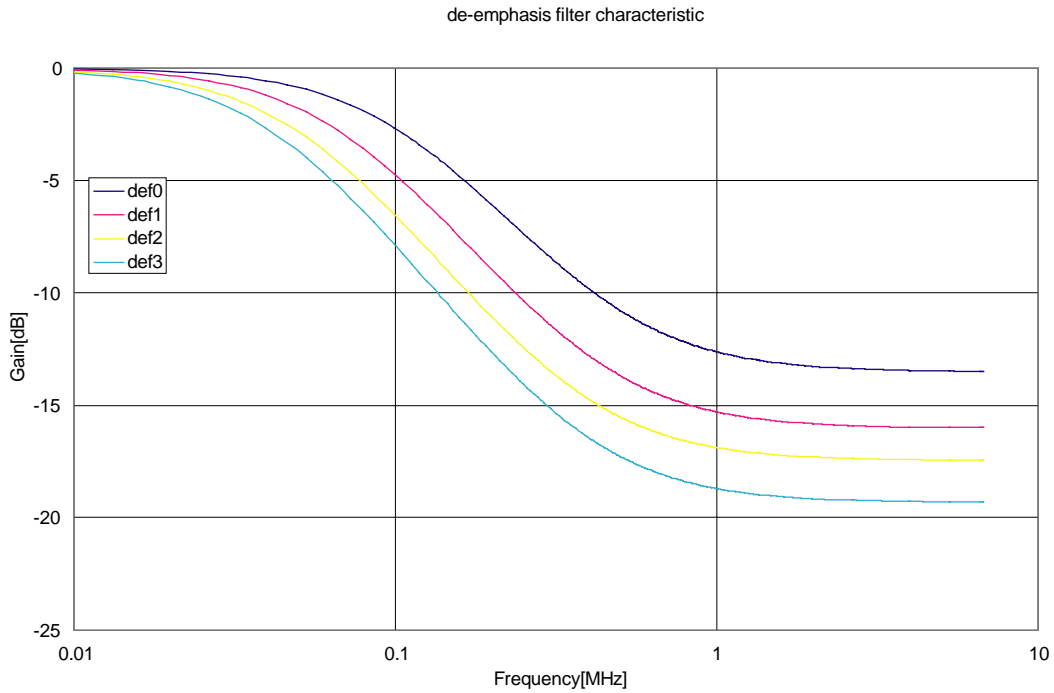
Fig.15 De-emphasis Filter Characteristics

11. Automatic Video Standard Recognition
   The video input standard is recognized automatically. Automatic video standard recognition can be set to ON or OFF using I2A_AUTODET.

12. S/N Detection
   S/N detection determines the video input noise level. During a vertical blanking period, the detection of noise is processed while the detection enable signal is high. The level of S/N detection can be controlled using I2A_NLTH.
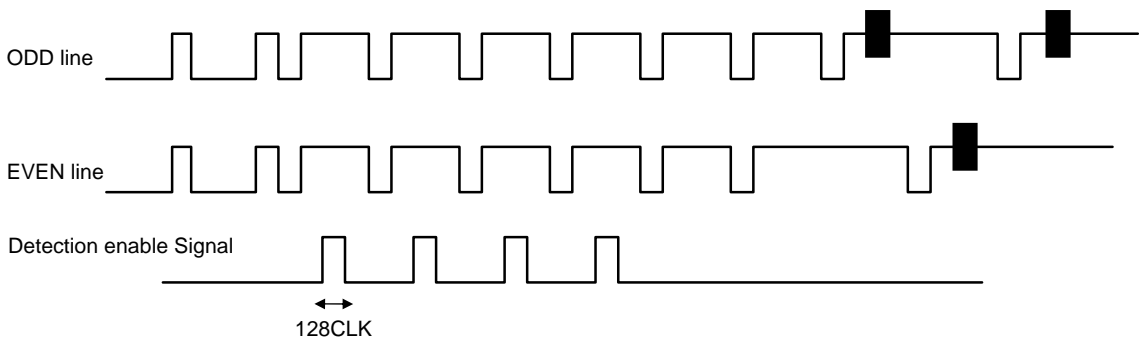
Fig.16 S/N Detection

13. Non-standard Detectionn
   This function determines whether the video input is non-standard. The video input is judged standard/non-standard by observing any variation from the standard VSYNC cycle.

14. No Signal Detection

This function detects no signal state.

The result of no signal detection is output to the INTREQ pin.

No signal detection function can be turned ON or OFF using I2A_NSDON [1]. Note that I2A_NSDON [0] is available when no signal detection is OFF.

15. Clock Rate Conversion

The sampling rate converter converts an input video signal sampled at 4fsc into 13.5MHz, and outputs synchronized signals with video data.

16. Sharpness

Sharpness of the image can be adjusted by detecting and forcibly correcting the edge of the luminance signal when the image is scanned horizontally. Adjustments to the enhancing frequency range and level of enhancement are possible. Sharpness can be turned ON or OFF using I2DSH_ON.The enhancing frequency range can be selected using I2DSH_FILTER, and the level of enhancement can be adjusted using I2DSH_ATT.

17. Contrast/Brightness

Brightness adjusts the brightness of the entire screen and Contrast adjusts the brightness gain.

1) Contrast

Contrast can be controlled using I2DCB_CONT.

00_H: × 0 to 80_H: × 1 to FF_H: × 2

2) Brightness

Brightness can be controlled using I2DCB_BRIGHT.

00_H: -128 to 80_H: ±0 to FF_H: +127

18. CTI (Color Transient Improvement)

The color transient can be improved by steepening the slope of the input signal. Processed video without overshoot or undershoot can provide more natural video images. The CTI can be switched between ON and OFF using I2DCT_CTIEN. The gain can be controlled using I2DCT_GAIN. The higher the I2DCT_GAIN is set, the more effective the CTI will be. CTI coring can be controlled using I2DCT_CORR. The higher the I2DCT_CORR is set, the less effective coring will be for extremely small amounts of noise. The CTI's tap parameter can be selected using I2DCT_SMP. The higher the I2DCT_SMP is set, the more the CTI characteristics shift toward lower frequencies.

19. HUE

The hue of the screen as a whole can be adjusted. (Refer to Fig.17.)

The phase angle can be selected using I2DHU_HUE.

0_H: -45° to 80_H: 0° to FF_H: 44° (with approx. 0.7° increments)
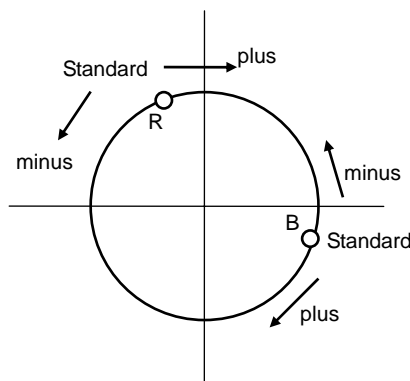
Fig.17 HUE

20. U/ V Gain

The saturation (color density) is adjusted by varying the Cb and Cr gain. The Cb gain can be adjusted using I2DUV_UGAIN, and the Cr gain using I2DUV_VGAIN.

21. 8-bit output format conversion

The 8-bit output format is converted to a format that is compatible with the ITU-R BT.656 format output.
Blue back color can be output in non-signal mode using I2D65_AUTOBBACK. Sepia color can be output using I2D65_SEPIA.
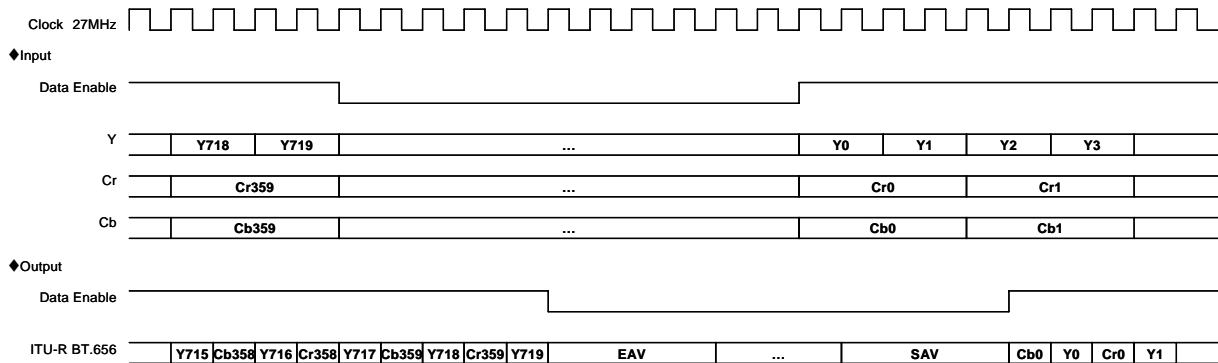
Fig.18 Timing Chart (ITU-R BT.656)

* The processing is being performed by a 27MHz free-run clock, and so the number of pixels in one line cannot be guaranteed. The data in the period from SAV to EAV can be guaranteed, so read the data using the SAV standard. (Data cannot be read using the EAV standard.)
* If equipment without an ITU-R BT.656 interface is connected, connect the HS and VS, or DE and read the data.
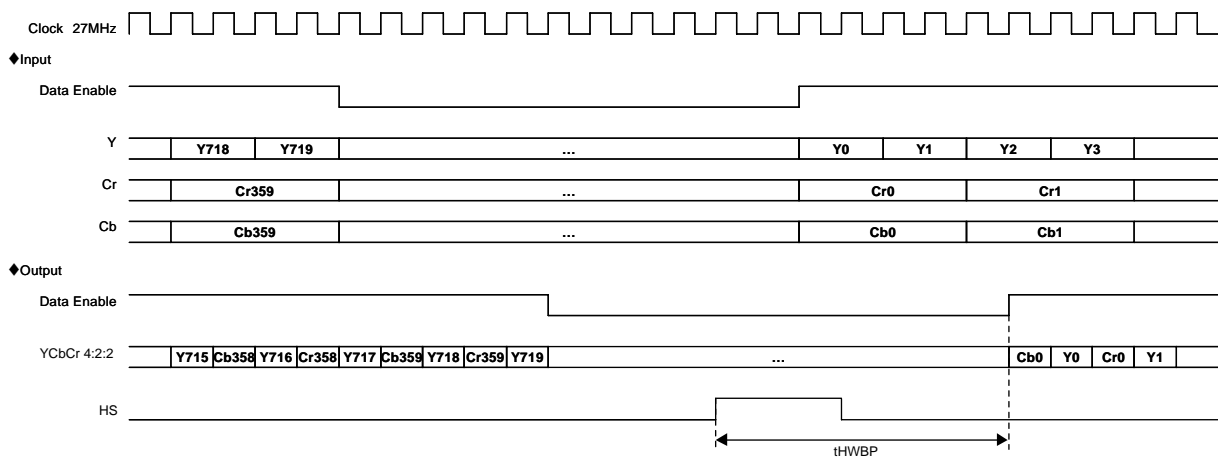
Figure 19 Timing Chart (YCbCr 4:2:2)

* tHWBP shown in Figure 19 has the same value for each format. It can be adjusted by registers.

Application Example
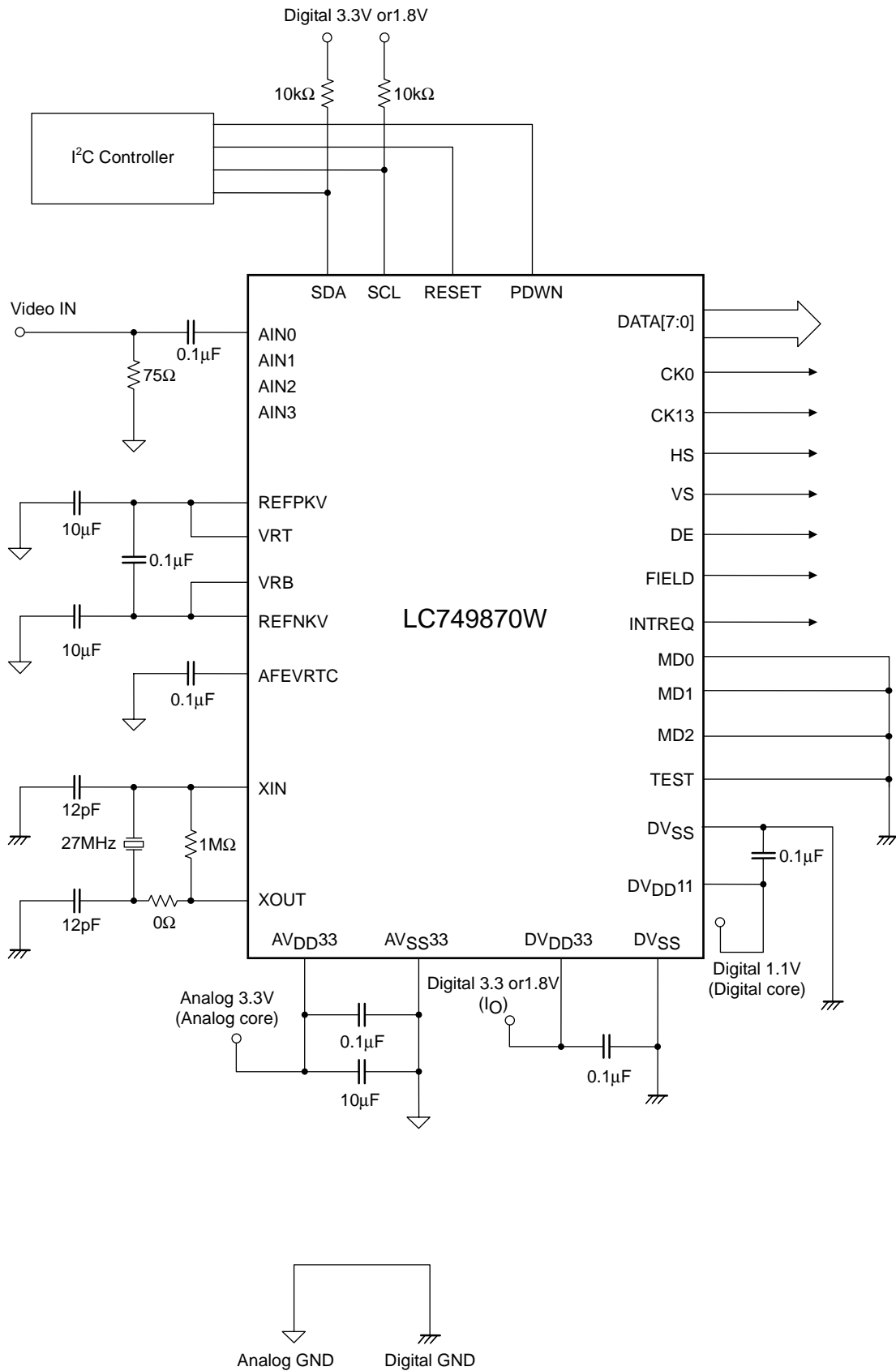
Other (usage precautions)

1. Precaution when turning-on the power

   As shown in the figure below, start transfer of the I^2C bus command after factoring in the power-on time (A), RST operation time (B) and command transfer start time (C).
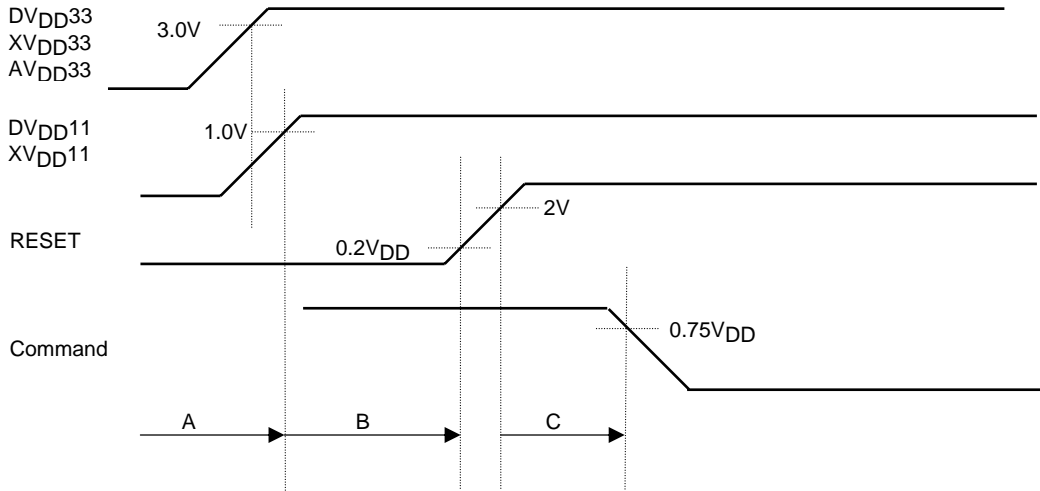
A: Power-on time

   This is the time taken from power-on to when the $*V_{DD}11$ operating voltage has reached the lowest level (0.99V) and operation has stabilized. The power-on-time depends on the characteristics of the power ICs and other components, so it must be checked separately.

   With regard to $*V_{DD}33$ and $*V_{DD}11$, $*V_{DD}11$ must be turned on after $*V_{DD}33$ has turned on.

B: RESET operation time

   This is the time during which the "L"level must be applied continuously for a period of 10ms or more to the RESET pin after the PDWN is released ("H" level).

C: Command transfer start time

   At least an interval of 10ms is required from the time RESET pin is released ("H" level) to the start of command transfer.

2. Precaution when turning-off the power
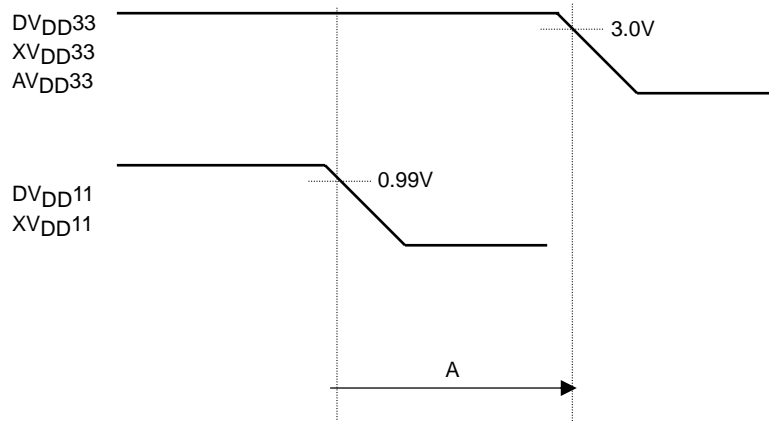
As a basic rule, power-off must be performed in the reverse sequence of power-on. However, no problems are posed if there is no wait time.

A: Power-off time

This is the time it takes to reach the I_O supply voltage and for operation to stabilize from the lowest level (0.99V) of the *$V_{DD}11$ operating supply voltage. With regard to *$V_{DD}33$ and *$V_{DD}11$, *$V_{DD}33$ must be turned off after *$V_{DD}11$ has been turned off or they must be turned off at the same time.