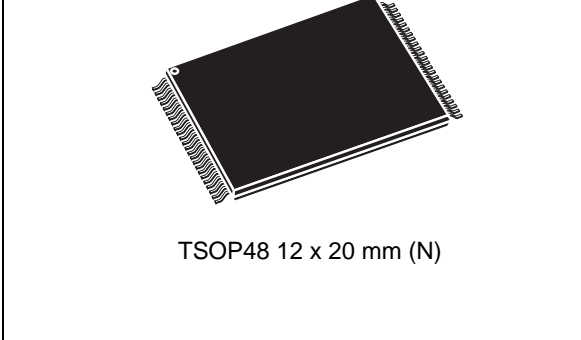


## Features

- High density multilevel cell (MLC) flash memory
    - 32 Gbits of memory array
    - 1 Gbit of spare area
    - Cost-effective solutions for mass storage applications
  - NAND interface
    - x8 bus width
    - Multiplexed address/data
  - Supply voltage:  $V_{DD} = 2.7$  to  $3.6$  V
  - Page size: (4096 + 128 spare) bytes
  - Block size: (512K + 16K spare) bytes
  - Multiplane architecture
    - Array split into two independent planes
    - All operations can be performed on both planes simultaneously
  - Memory cell array:
    - (4 K + 128) bytes x 128 pages x 8192 blocks (2 dice x16 Gbits, 2 Chip Enable)
  - page read/program
    - Random access: 60  $\mu$ s (max)
    - Sequential access: 25 ns (min)
    - Page program operation time: 800  $\mu$ s (typ)
  - Multipage program time (2 pages): 800  $\mu$ s (typ)
  - Copy-back program
    - Fast page copy
  - Fast block erase
    - Block erase time: 2.5 ms (typ)
- 
- TSOP48 12 x 20 mm (N)
- Multiblock erase time (2 blocks): 2.5 ms (typ)
  - Status register
  - Electronic signature
  - Serial number option
  - Chip enable 'don't care'
  - Data protection
    - Hardware program/erase locked during power transitions
  - Development tools
    - Error correction code models
    - Bad block management and wear leveling algorithm
    - HW simulation models
  - Data integrity
    - 10,000 program/erase cycles (with ECC)
    - 10 years data retention
  - ECOPACK® packages available

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# 1 Description

The NAND32GW3D4A is a multilevel cell (MLC) device from the NAND flash 4224-byte page family of non-volatile flash memories. The NAND32GW3D4A has a density of 32 Gbits and combines two 16-Gbit dice in a stacked device. Each dice has its own Chip Enable and Ready/Busy pin so that it can be driven independently using the relative Chip Enable pin. Moreover, each dice has its own maximum number of bad blocks and its own electronic signature code. The device operates from a 3 V power supply.

This document must be read in conjunction with the NAND16GW3D2A datasheet, which fully details all the specifications required to operate the 16-Gbit flash memory component.

The device is available in TSOP48 (12 × 20 mm) package and is shipped from the factory with block 0 always valid and the memory content bits, in valid blocks, erased to '1'.

Refer to the list of available part numbers and to [Table 8: Ordering information scheme](#) for information on how to order these options.

**Table 1. Device summary**

Part number	Density	Bus width	Page size	Block size	Memory array	Operating voltage (V <sub>DD</sub> )	Timings				Package
							Random access time (max)	Sequential access time (min)	Page program (typ)	Block erase (typ)	
NAND32GW3C4A	32 Gbits	x8	4096+ 128 bytes	512K + 16K bytes	128 pages x 8192 blocks	2.7 to 3.6 V	25 ns	60 μs	800 μs	2.5 ms	TSOP48

Figure 1. Functional block diagram

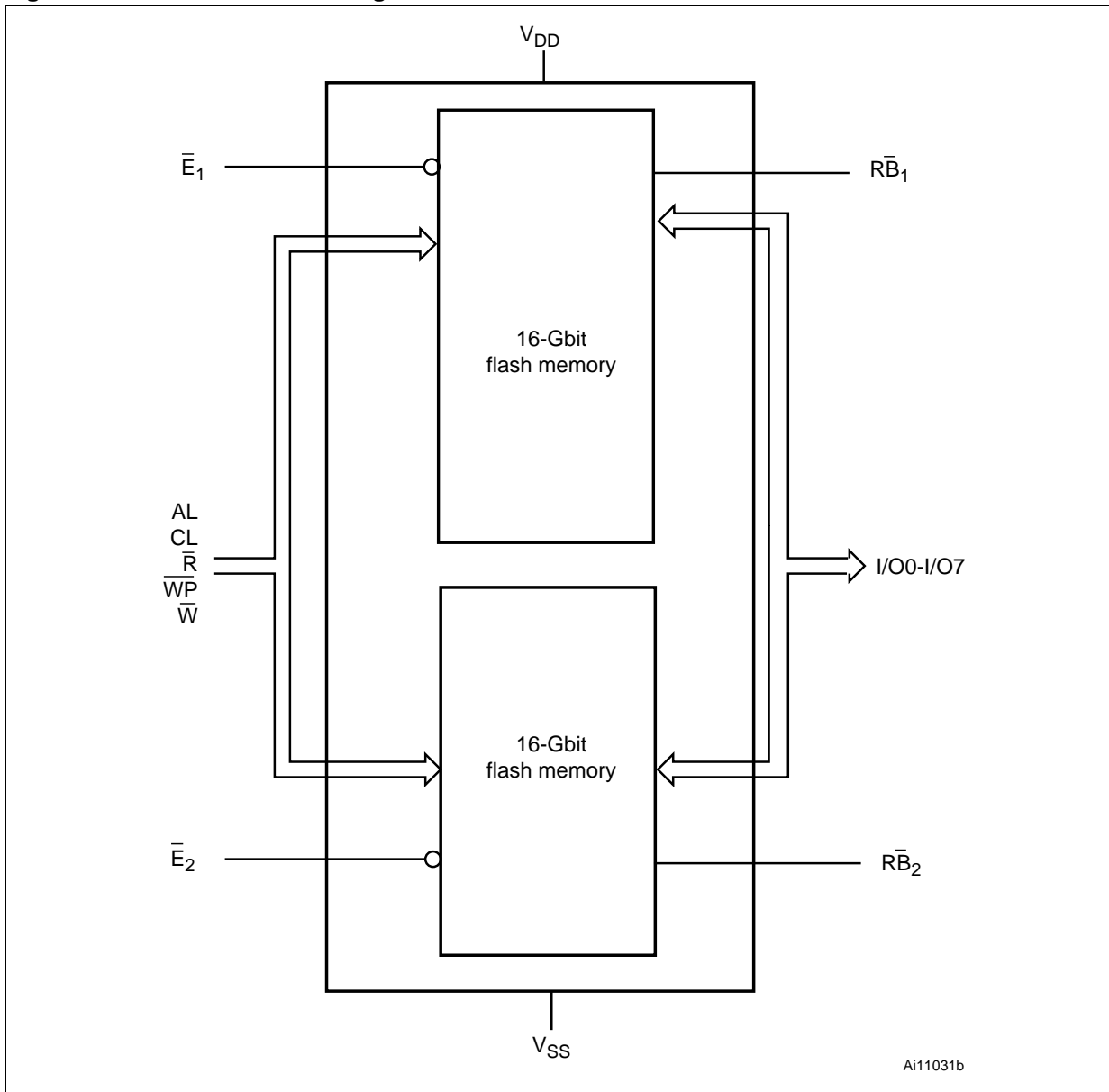


Figure 2. Logic diagram

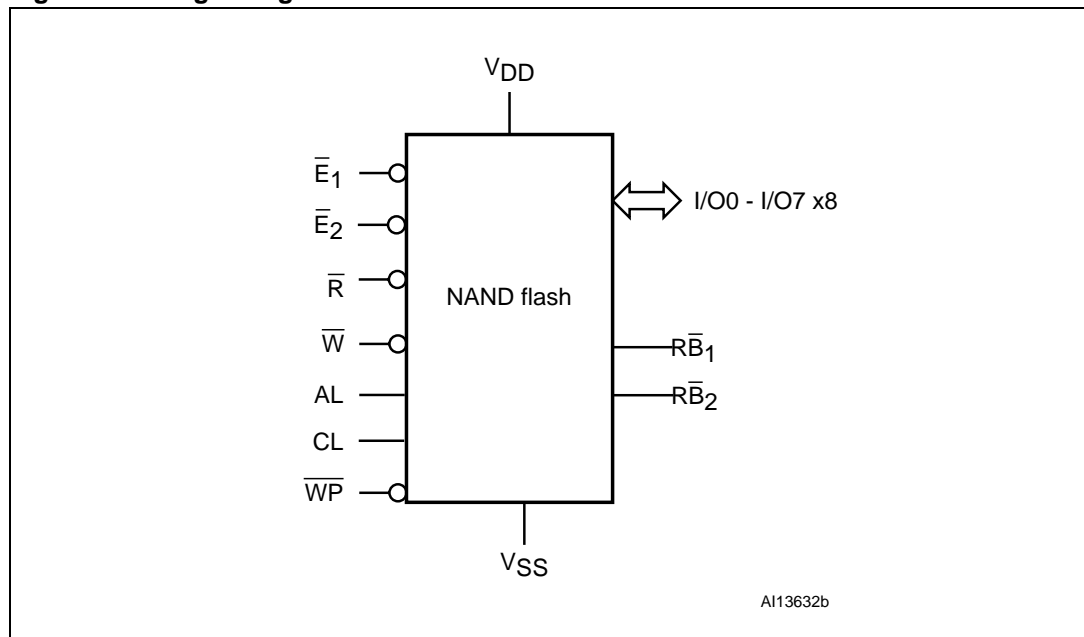
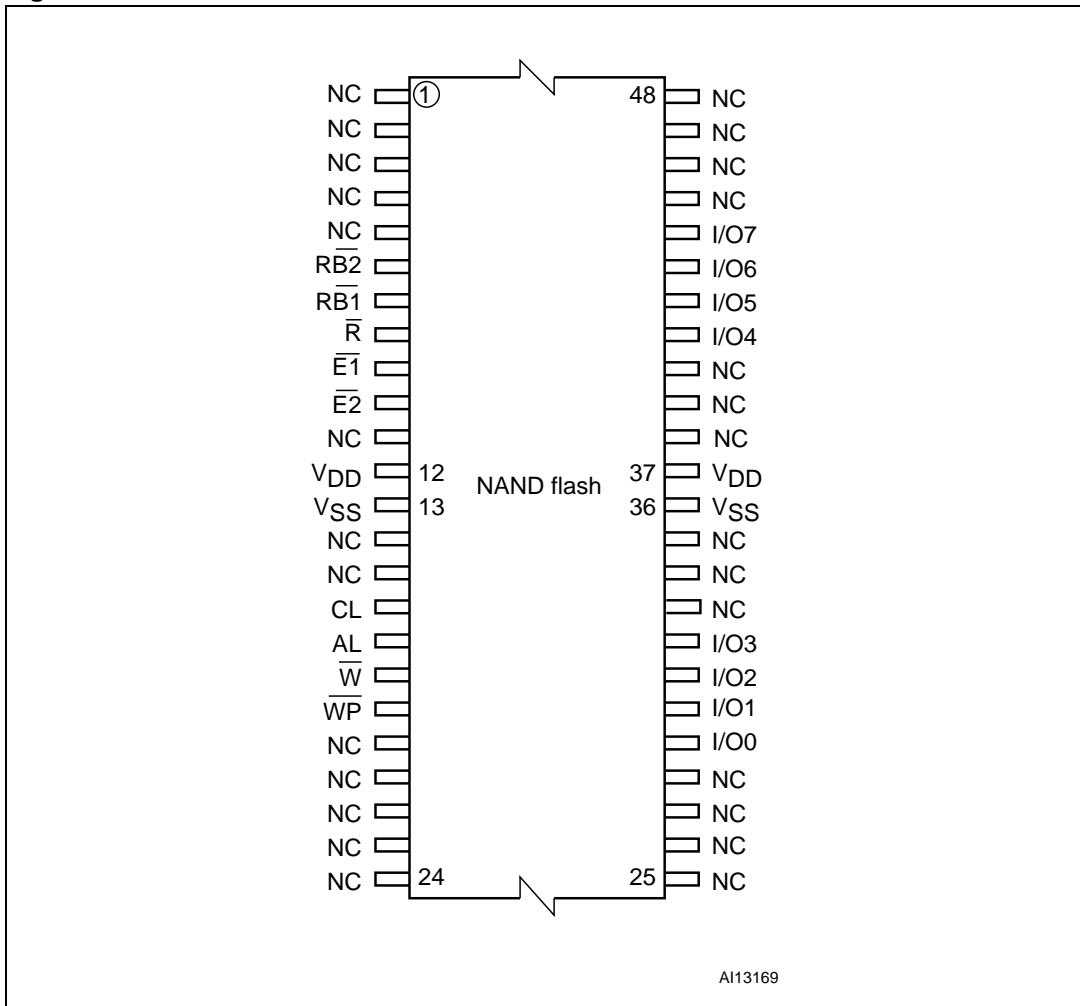


Table 2. Signal names

Signal	Function	Direction
I/O0 - I/O7	Data input/outputs	Input/output
CL	Command Latch Enable	Input
AL	Address Latch Enable	Input
E <sub>1</sub> -bar, E <sub>2</sub> -bar	Chip Enable	Input
R-bar	Read Enable	Input
W-bar	Write Enable	Input
WP-bar	Write Protect	Input
RB <sub>1</sub> -bar, RB <sub>2</sub> -bar	Ready/Busy (open drain output)	Output
V <sub>DD</sub>	Power supply	Power supply
V <sub>SS</sub>	Ground	Ground
NC	No connection	-
DU	Do not use	-

Figure 3. TSOP48 connections



A113169



## 2 Memory array organization

The memory array is split into two dice. Each dice is comprised of NAND structures where 32 cells are connected in series.

It is organized into blocks where each block contains 128 pages. The array is split into two areas, the main area and the spare area. The main area of the array stores data, whereas the spare area typically stores software flags or bad block identification.

The pages are split into a 4096-byte main area and a spare area of 128 bytes.

### 2.1 Bad blocks

The NAND32GW3D4A device may contain bad blocks, where the reliability of blocks that contain one or more invalid bits is not guaranteed. Additional bad blocks may develop during the lifetime of the device.

The bad block information is written prior to shipping (refer to the bad block management section of the NAND16GW3D2A datasheet for more details).

*Table 3: Valid blocks* shows the minimum number of valid blocks. The values shown include both the bad blocks that are present when the device is shipped and the bad blocks that could develop later on.

Each dice can have the same maximum number of bad blocks.

These blocks need to be managed using bad blocks management and block replacement (refer to the software algorithms section of the NAND16GW3D2A datasheet).

**Table 3. Valid blocks**

Density of device	Minimum	Maximum
32 Gbits	7992	8192

### 2.2 Parallel operation

The NAND32GW3D4A is composed of two dice, each one driven by its Chip Enable pin ( $\bar{E}_1$  and  $\bar{E}_2$ , respectively). It is possible to drive the two dice in parallel, thus increasing the throughput in Mbyte/s.

When one of the two dice is in a busy state, every operation can be issued on the other available dice.

## 3 Signal descriptions

See [Figure 1: Functional block diagram](#), and [Table 2: Signal names](#) for a brief overview of the signals connected to this device.

### 3.1 Inputs/outputs (I/O0-I/O7)

Input/outputs 0 to 7 are used to input the selected address, output the data during a read operation, or input a command or data during a write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

### 3.2 Address Latch Enable (AL)

The Address Latch Enable activates the latching of the address inputs in the command interface. When AL is High, the inputs are latched on the rising edge of Write Enable.

### 3.3 Command Latch Enable (CL)

The Command Latch Enable activates the latching of the command inputs in the command interface. When CL is High, the inputs are latched on the rising edge of Write Enable.

### 3.4 Chip Enable ( $\bar{E}_1$ , $\bar{E}_2$ )

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is Low,  $V_{IL}$ , the device is selected. If Chip Enable goes High,  $V_{IH}$ , while the device is busy, the device remains selected and does not go into standby mode.

### 3.5 Read Enable ( $\bar{R}$ )

The Read Enable pin,  $\bar{R}$ , controls the sequential data output during read operations. Data is valid  $t_{RLQV}$  after the falling edge of  $\bar{R}$ . The falling edge of  $\bar{R}$  also increments the internal column address counter by one.

### 3.6 Write Enable ( $\bar{W}$ )

The Write Enable input,  $\bar{W}$ , controls writing to the command interface, input address, and data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10  $\mu$ s (min) is required before the command interface is ready to accept a command. It is recommended to keep Write Enable High during the recovery time.

### 3.7 Write Protect ( $\overline{\text{WP}}$ )

The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low,  $V_{\text{IL}}$ , the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low,  $V_{\text{IL}}$ , during power-up and power-down.

### 3.8 Ready/Busy ( $\overline{\text{RB}}_1$ , $\overline{\text{RB}}_2$ )

The Ready/Busy output,  $\overline{\text{RB}}_1$  and  $\overline{\text{RB}}_2$ , is an open-drain output that can identify if the P/E/R controller is currently active.

When Ready/Busy is Low,  $V_{\text{OL}}$ , a read, program or erase operation is in progress. When the operation completes, Ready/Busy goes High,  $V_{\text{OH}}$ .

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low indicates that one, or more, of the memories is busy.

During power-up and power-down a minimum recovery time of 10  $\mu\text{s}$  is required before the command interface is ready to accept a command. During this period the Ready/Busy signal is Low,  $V_{\text{OL}}$ .

Refer to [Section 6: Package mechanical](#) for details on how to calculate the value of the pull-up resistor.

### 3.9 $V_{\text{DD}}$ supply voltage

$V_{\text{DD}}$  provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

An internal voltage detector disables all functions whenever  $V_{\text{DD}}$  is below  $V_{\text{LKO}}$  to protect the device from any involuntary program/erase during power transitions.

Each device in a system should have  $V_{\text{DD}}$  decoupled with a 0.1  $\mu\text{F}$  capacitor. The PCB track widths should be sufficient to carry the required program and erase currents.

### 3.10 $V_{\text{SS}}$ ground

Ground,  $V_{\text{SS}}$ , is the reference for the power supply. It must be connected to the system ground.

## 4 Maximum ratings

Stressing the device above the ratings listed in [Table 4: Absolute maximum ratings](#) may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value		Unit
		Min	Max	
$T_{BIAS}$	Temperature under bias	- 50	125	°C
$T_{STG}$	Storage temperature	- 65	150	°C
$V_{IO}^{(1)}$	Input or output voltage	- 0.6	4.6	V
$V_{DD}$	Supply voltage	- 0.6	4.6	V

1. Minimum voltage may undershoot to -2 V for less than 20 ns during transitions on input and I/O pins. Maximum voltage may overshoot to  $V_{DD} + 2$  V for less than 20 ns during transitions on I/O pins.

## 5 DC and AC parameters

This section summarizes the operating and measurement conditions as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristics tables are derived from tests performed under the measurement conditions summarized in [Table 5: Operating and AC measurement conditions](#). Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

**Table 5. Operating and AC measurement conditions**

Parameter	Min	Max	Units
Supply voltage ( $V_{DD}$ )	2.7	3.6	V
Ambient temperature ( $T_A$ )	0	70	°C
	-40	85	°C
Load capacitance ( $C_L$ ) (1 TTL GATE and $C_L$ )	50		pF
Input pulses voltages	0	$V_{CC}$	V
Input and output timing ref. voltages	1.5		V
Output circuit resistor $R_{ref}$	8.35		k $\Omega$
Input rise and fall times	5		ns

**Table 6. Capacitance<sup>(1)</sup>**

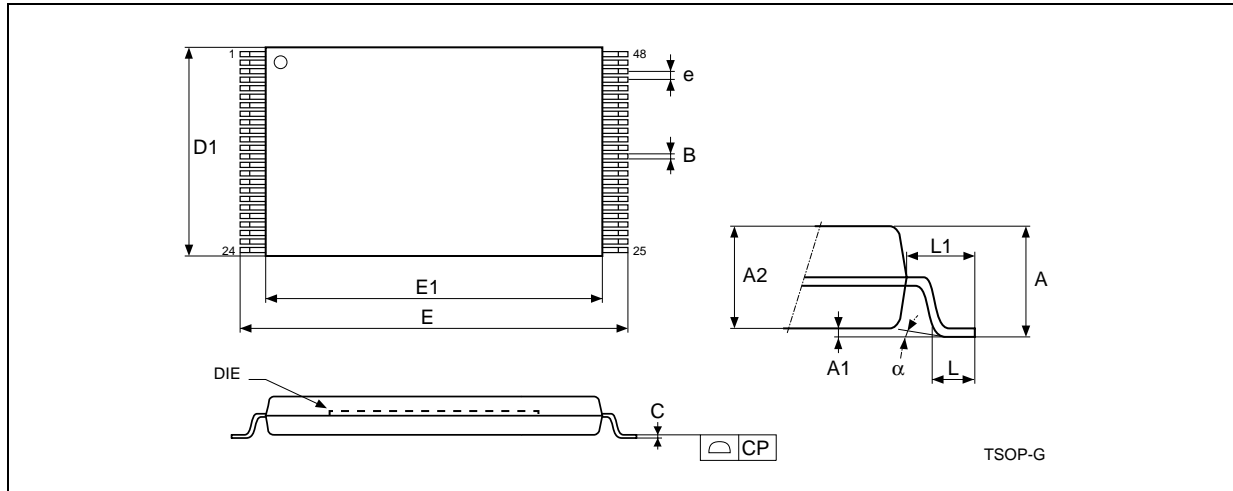
Symbol	Parameter	Test condition	Typ	Max	Unit
$C_{IN}$	Input capacitance	$V_{IN} = 0\text{ V}$		10	pF
$C_{I/O}$	Input/output capacitance	$V_{IL} = 0\text{ V}$		10	pF

1.  $T_A = 25\text{ °C}$ ,  $f = 1\text{ MHz}$ .  $C_{IN}$  and  $C_{I/O}$  are not 100% tested.

## 6 Package mechanical

To meet environmental requirements, Numonyx offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

**Figure 4. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package outline**



1. Drawing is not to scale.

**Table 7. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package mechanical data**

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1	0.10	0.05	0.15	0.004	0.002	0.006
A2	1.00	0.95	1.05	0.039	0.037	0.041
B	0.22	0.17	0.27	0.009	0.007	0.011
C		0.10	0.21		0.004	0.008
CP			0.08			0.003
D1	12.00	11.90	12.10	0.472	0.468	0.476
E	20.00	19.80	20.20	0.787	0.779	0.795
E1	18.40	18.30	18.50	0.724	0.720	0.728
e	0.50	–	–	0.020	–	
L	0.60	0.50	0.70	0.024	0.020	0.028
L1	0.80			0.031		
a	3°	0°	5°	3°	0°	5°

# 7 Ordering information

**Table 8. Ordering information scheme**

Example:	NAND32G	W 3	D 4	A	N 1	E
<b>Device type</b> NAND flash memory						
<b>Density</b> 32G = 32 Gbits						
<b>Operating voltage</b> W = $V_{DD} = 2.7$ to $3.6$ V						
<b>Bus width</b> 3 = x8						
<b>Family identifier</b> D = 4 Kbyte-page MLC						
<b>Device options</b> 4 = Chip Enable 'don't care' enabled with 2 Chip Enable and 2 Ready/Busy signals						
<b>Product version</b> A = first version						
<b>Package</b> N = TSOP48 12 x 20 mm						
<b>Temperature range</b> 1 = 0 to 70 °C 6 = -40 to 85 °C						
<b>Option</b> E = ECOPACK® package, standard packing F = ECOPACK® package, tape and reel packing						

*Note: Devices are shipped from the factory with the memory content bits, in valid blocks, erased to '1'. For further information on any aspect of this device, please contact your nearest Numonyx sales office.*

## 8 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
05-Jun-2008	1	Initial release.
09-Jul-2008	2	Modified: density of spare area – on page 1, <i>Figure 1: Functional block diagram</i> , and <i>Section 3.9: VDD supply voltage</i> .



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