

Divide by: 64/65/72 triple modulus low power ECL prescaler

NE/SA702

DESCRIPTION

The NE702 triple modulus (Divide By 64/65/72) low power ECL prescaler is used in synthesizer systems to achieve low phase lock time, broad operating range, high reference frequency and small frequency step sizes. The minimum supply voltage is 2.5V for compatibility with the new CMOS UMF1005 and UMF1009 synthesizers from Philips and other logic circuits. The maximum supply current is 2.8mA allowing application in battery operated low-power equipment. Maximum input signal frequency is 1.2GHz for cellular and other land mobile applications. There is no lower frequency limit due to a fully static design. The circuit is implemented in ECL technology on the HS4+ process (the bipolar portion of the QUBiC process). The circuit will be available in an 8 pin SO package with 150 mil package width.

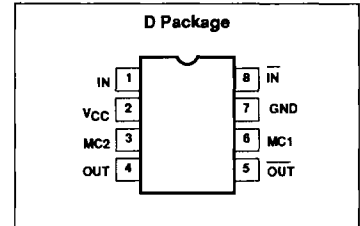
FEATURES

- Low voltage operation
- Low current consumption
- Operation up to 1.2GHz

APPLICATIONS

- Cellular phones
- Cordless phones
- RF LANs
- Test and measurement
- Military radio
- VHF/UHF mobile radio
- VHF/UHF hand-held radio

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE
8-Pin Plastic SO (Surface-mount)	0 to +70°C	NE702D
8-Pin Plastic SO (Surface-mount)	-40 to +85°C	SA702D

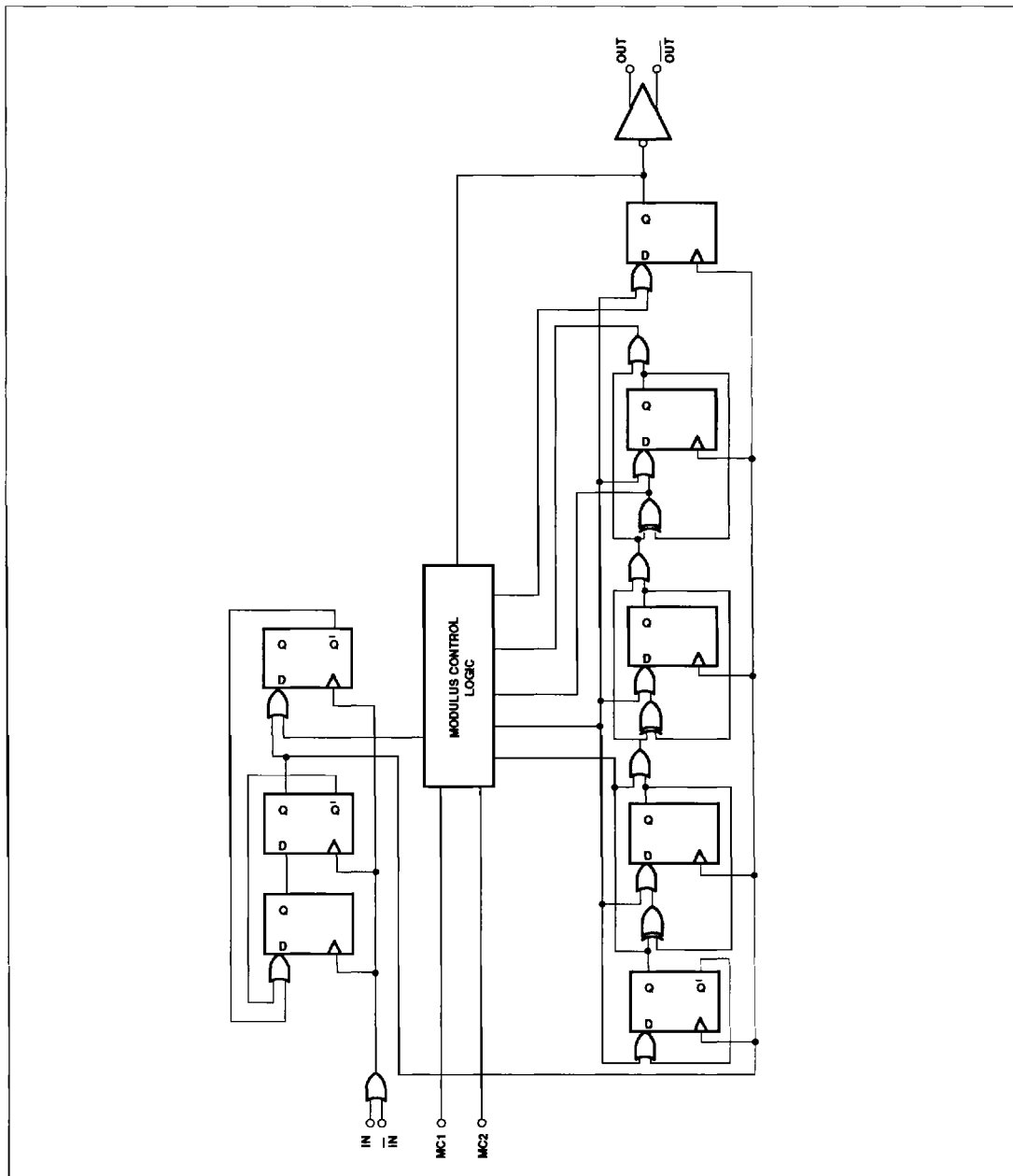
ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Maximum operating voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to V_{CC}	V
I_O	Output current	10	mA
T_{STG}	Storage temperature range	-65 to +125	°C
T_A	Operating ambient temperature range	-55 to +125	°C
θ_{JA}	Thermal impedance	90	°C/W

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BLOCK DIAGRAM



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DC ELECTRICAL CHARACTERISTICS

The following DC specifications are valid for $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply voltage range		2.5		6.0	V
I_{CC}	Supply current				2.8	mA
V_{OH}	Output high level	$I_{OUT} = 1.2\text{mA}$	$V_{CC}-1.4$			V
V_{OL}	Output low level	$V_{CC} \geq 3.2\text{V}$			$V_{CC}-3.0$	V
		$V_{CC} < 3.2\text{V}$			0.2	V
V_{IH}	MC1,2 input high threshold	$I_{MC} = 60\mu\text{A}$	2.0			V
V_{IL}	MC1,2 input low threshold	$I_{MC} = 20\mu\text{A}$			0.8	V
I_I	MC1,2 input current	$V_{MC} = V_{CC} = 5.0\text{V}$			150	μA

AC ELECTRICAL CHARACTERISTICS

The following AC specifications are valid for $V_{CC} = 3.0\text{V}$, $-40^{\circ}\text{C} < T_A < +85^{\circ}\text{C}$; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{IN}	Input signal amplitude	1000pF input coupling	0.1		2.0	$V_{p,p}$
f_{IN}	Input signal frequency	Direct coupled input	0		1.2	GHz
		1000pF input coupling			1.2	GHz
R_{ID}	Differential input resistance	DC measurement	5			k Ω
C_I	Input capacitance				TBD	pF
V_O	Output voltage	$V_{CC} = 5.0\text{V}$	1.6			$V_{p,p}$
		$V_{CC} = 3.0\text{V}$	1.2			$V_{p,p}$
t_S	Modulus set-up time	$f_{IN} = 1.2\text{GHz}$		TBD		ns
t_H	Modulus hold time	$f_{IN} = 1.2\text{GHz}$		TBD		ns
t_{PD}	Propagation time			TBD		ns

DESCRIPTION OF OPERATION

The NE702 comprises a frequency divider circuit implemented using a divide by 4 or 5 synchronous prescaler followed by a 5 stage synchronous counter, see BLOCK DIAGRAM. The normal operating mode is for MC1 (Modulus Control) to be set high and MC2 input to be set low in which case the circuit comprises a divide by 64. For divide by 65 the MC1 signal is forced low, causing the prescaler circuit to switch into divide by 5 operation for the last cycle of the synchronous counter. For divide by 72, MC2 is set high configuring the prescaler to divide

by 4 and the counter to divide by 18. A truth table for the modulus values is given below:

Table.

Modulus	MC1	MC2
64	1	0
65	0	0
72	0	1
72	1	1

For minimization of propagation delay effects, the second divider circuit is synchronous to the divide by 4/5 stage output.

The prescaler input is positive edge sensitive, and the output at the final count is a falling edge with propagation delay t_{PD} relative to the input. The rising edge of the output occurs at the count 32 with delay t_{PD} .

The MC1 and MC2 inputs are TTL compatible threshold inputs operating at a reduced input current. CMOS and low voltage interface capability are allowed.

The prescaler input is differential and ECL compatible. The output is differential ECL compatible.

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AC TIMING CHARACTERISTICS

