SUN MICROELECTRONICS

STP5212

July 1997

UltraSPARC™-II CPU Module

DATA SHEET — Complete 296 MHz CPU, 2.0 MB E-Cache, UDB-II

DESCRIPTION

The UltraSPARC-II module is a high performance, SPARC V9 compliant, small form factor processor module. It interfaces to the UltraSPARC Port Architecture (UPA) interconnect bus.

The module consists of one UltraSPARC-II microprocessor, two UltraSPARC-II Data Buffer chips, one 32 K x 36 tag SRAM, four 128k K x 36 data SRAMs, and an MC100LVE210 clock buffer.

Components on the module operate at 3.3 V and 2.6 V. All signal levels to and from the module are 3.3V LVTTL compatible, except for the differential clock inputs, which are at 3.3V PECL levels. The module runs synchronously with the system interface at a 3:2 frequency ratio. The processor always doubles the clock it receives which yields a 3:1 ratio to the UPA frequency.The module is available with the UltraSPARC-II running at 296MHz. The interface to the module is through a high-speed standard edge connector.

Features	*Benefits*
• High performance UltraSPARC-II CPU Module	• Deliver 12.1 SPECint95 (est.), 15.5 SPECfp95 (est.) at 296MHz
• Programmable UPA bus speed	• Easy upgrade to a faster Processors
• SPARC V9 Compliant	
• Implements Visual Instruction Set (VIS)	• Comprehensive hardware support for 3D graphics, H-261 compression/decompression, and MPEG2 decompression
• 128-Bit wide data bus	• Peak bandwidth of 1.3 Gigabytes/sec
• Cache coherency support for multiprocessing	• Range of scalable systems can be built
• 2.0 Megabyte E-Cache	• UltraSPARC-II Pipelined E-Cache Interface delivering high performance
• Operates at 3.3 and 2.6 V LVTTL	• Allows very high bus speeds and power savings, thus reducing the generated heat
• 158.75 mm x 107.95 mm form factor	• Small footprint
• Implemented on a 330-pin dual high-speed card; edge connector to connect the Module with the UPA Interconnect Bus	• High performance impedance controlled Connector provides reliable signal integrity.

Block Diagram

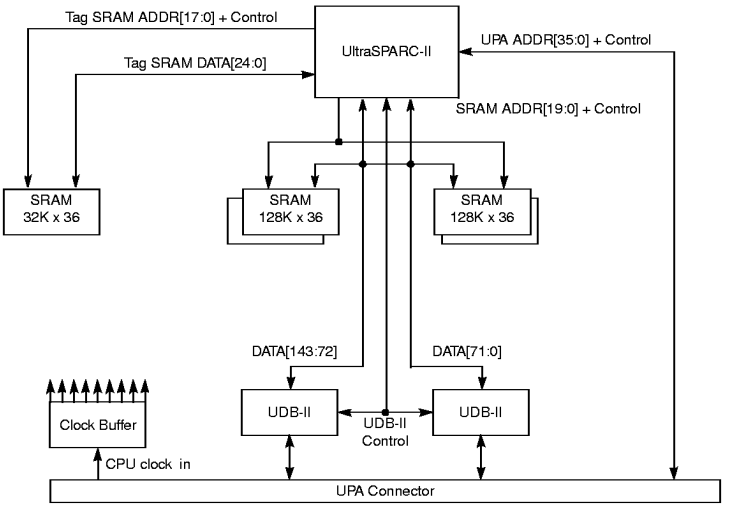


Figure 1. Module Block Diagram

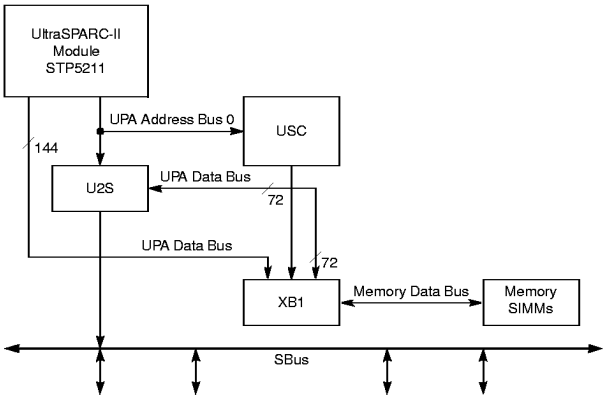


Figure 2. Uniprocessor System Configuration

Component Overview

The STP5211, UltraSPARC-II CPU Module consists of the following components:

- UltraSPARC-II Processor
- UltraSPARC-II Data Buffer (UDB-II)
- 2.0 Megabyte E-Cache, made up of four (128 Kilobyte X 36) SRAM microchips
- 32 Kilobyte X 36 Tag SRAMs

UltraSPARC-II CPU

The UltraSPARC-II processor is a high-performance, highly integrated, superscalar processor implementing the SPARC V9 64-bit RISC architecture. UltraSPARC-II is capable of sustaining the execution of up to four instructions per cycle even in the presence of conditional branches and cache misses. It supports a 44-bit virtual address space and a 41-bit physical address space. The instruction set also includes the Visual Instruction Set (VIS) that accommodates the following functions:

- the most common operations related to two-dimensional image processing
- three-dimensional graphics
- video compression and decompression algorithms and other pixel-based algorithms
- support for high-bandwidth bcopy through block load and block store instructions

All signals that interface with the system are compatible with LVTTL levels. All signals that interface with SRAMS and the UDBs are 2.6V swing LVCMOS levels.

The UltraSPARC-II CPU is packaged in a ceramic 787 pin 1.0 mm pitch LGA (land grid array) package. The package dimension is 35mm by 35 mm.

The UltraSPARC-II CPU LGA package requires the use of a 787 pin high speed socket. (Sun part Number - 190-1398-01, UltraSPARC-II SOCKET ASSY 787 POSITION CINAPSE.)

UltraSPARC-II Data Buffer (UDB-II)

The UltraSPARC-II module uses two UltraSPARC-II Data Buffer (UDB-II) (128 Data + 16 ECC) microchips. The UDB-II connects UltraSPARC-II and its external cache to the 144-bit UPA interconnect data bus. All data that moves between the UltraSPARC-II module and the system passes through the UDB-II, including cache fill requests, writeback data for dirty displaced cache lines, copyback data for cache entries requested by the system, non-cacheable loads and stores, and interrupt vectors going to and from the CPU.

Each UDB-II has a 64-bit interface plus 8 parity bits on the CPU side, and a 64-bit interface plus 8 error correction code (ECC) bits on the system side.

The UDB-II has two frequency domains. The system bus side is clocked with the UPA bus clock (1/3 of the CPU pipeline frequency). The processor side is clocked with the same clock delivered to UltraSPARC-II (1/2 of the CPU pipeline frequency). All signals that interface with the system are compatible with LVTTL levels. All signals that interface with the SRAMs and the CPU are 2.6 V swing LVCMOS levels. The clock is a differential low-voltage PECL input.

The UDB-II is packaged in a plastic, 256-pin (187 signals and 69 power/gnd pins), 1.27mm (50 mil) pitch BGA (ball grid array) package. The package dimension is 30 mm by 30 mm.

External Cache

The External Cache is connected to the E-Cache data bus. Five SRAM chips are used to implement the 2.0 Megabyte cache. One SRAM is used as the tag SRAM and four are used as data SRAMs. The tag SRAM is 32 K x 36, while the data SRAMS are 128 K x 36. All five SRAMs are synchronous register-latch SRAM chips.

The SRAM interface to the CPU runs at one-half of the frequency of the CPU pipeline. The SRAM signals operate at 2.6 V swing LVCMOS levels. The SRAM clock is a differential low-voltage PECL input.

The SRAMs are packaged in a plastic 119 pin 1.27 mm (50 mil) BGA (ball grid array) package. The package is 22 mm by 14 mm.

System

As shown in *Figure 2*, the system I/O controller (U2S) interfaces between the UPA and I/O Sbus. The system controller-uniprocessor chip (USC) has many of the functions required to manage the UPA bus. And the bus multiplexer chip (XB1) functions as a crossbar between the UPA data bus and main memory.

The system interface signals run at one-third the rate of the internal CPU frequency. All signals that interface with the system are compatible with LVTTL levels. The on-module SRAM cache interface runs at one-half of the CPU pipeline frequency. All external signals that interface with the SRAMs and the UDB-II are 2.6 V swing LVCMOS levels. The module clocks from the system are differential low-voltage PECL-input.

UPA Interconnect Pin Assignments

The UltraSPARC-II module supports full master or slave functionality with the 128-bit data bus.

The UPA_PORT_ID[4:2] are hardwired on the module to "0" in this profile. UPA_PORT_ID[1:0] are brought out to the connector pins, and have to be hardwired in the system. This feature optimizes this profile for systems with four or fewer processors. Systems that need to support more than 4 modules map the limited set of UPA_PORT_IDs from this module to the range of required UPA_PORT_IDs by implementation-specific means in the system.

Two types of power are required on this module: V_{DD} at 3.3V, and V_{DD_CORE}. V_{DD_CORE} supplies the core of the processor chip, the UDB external cache interface I/O, and the SRAM I/O on the module, and is driven by a programmable system power supply. A resistor located on the module sets sends the program value to power supply and the V_{DD_CORE} to 2.6 V.

Figure 3 and *Figure 4* show the pin assignments of the module interconnect.

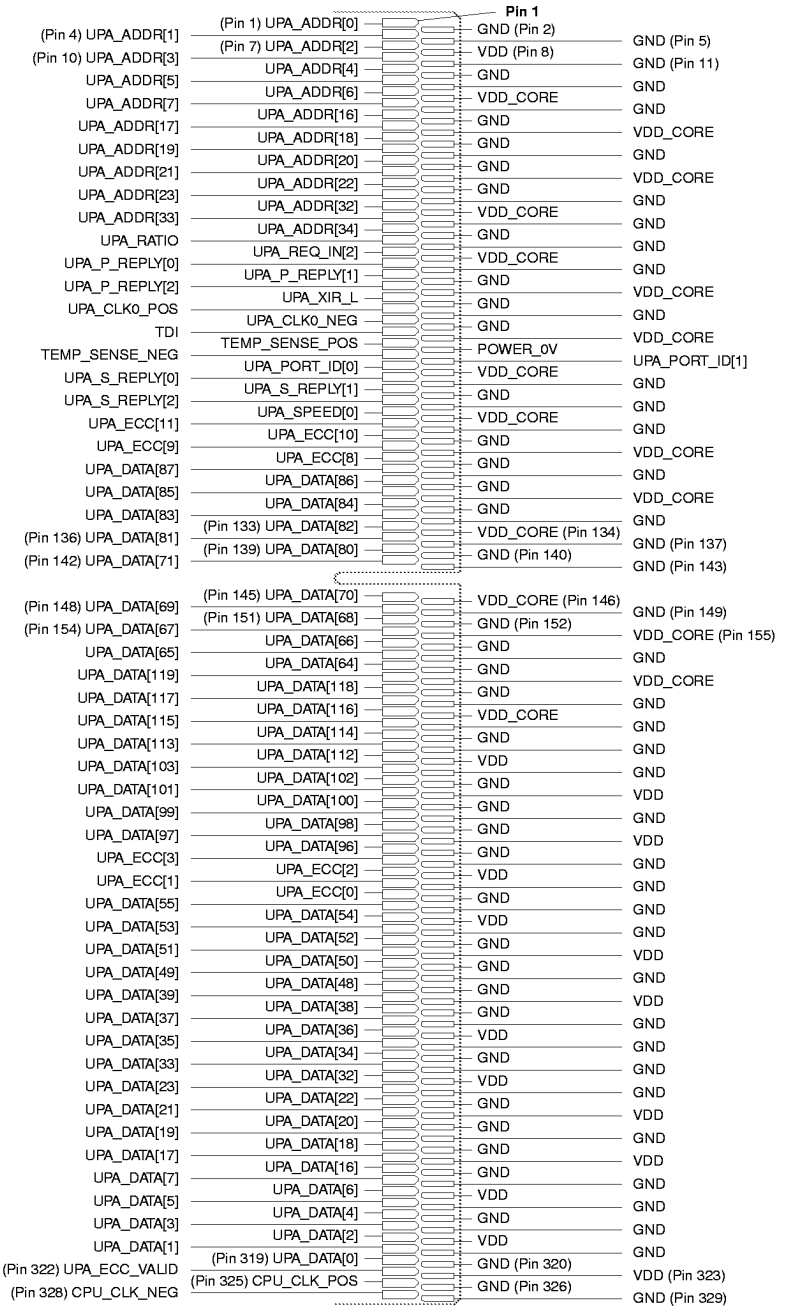


Figure 3. UPA Connector Pin-Out Assignment (Top)

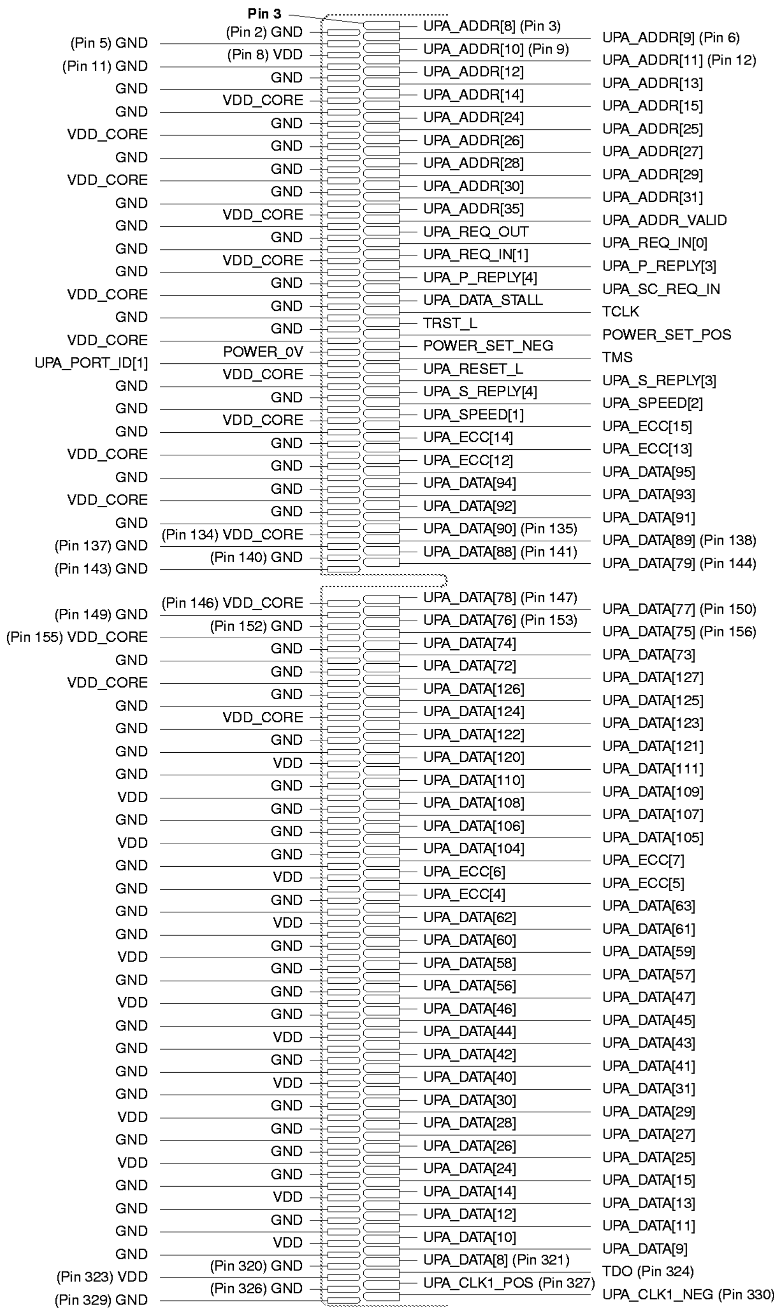


Figure 4. UPA Connector Pin-Out Assignment (Bottom)

SIGNAL DESCRIPTION

System Interface

Signal	Type	Name and Function
UPA_ADDR[35:0]	I/O	Packet switched transaction request bus. Maximum of three other masters and one system controller can be connected to this bus. Includes 1-bit odd-parity protection. Synchronous to UPA_CLK.
UPA_ADDR_VALID	I/O	Bidirectional radial UltraSPARC-II Bus signal between UltraSPARC-II and the System. Driven by UltraSPARC-II to initiate UPA_ADDR transactions to the System. Driven by System to initiate Coherency, Interrupt or Slave transactions to UltraSPARC-II. Synchronous to UPA_CLK. Active high.
UPA_REQ_IN[2:0]	I	UltraSPARC-II system address bus arbitration request from up to 3 other UltraSPARC-II Bus ports that might be sharing the UPA_ADDR. Used by UltraSPARC-II for the distributed UPA_ADDR arbitration protocol. Connection to other UltraSPARC-II Bus ports is strictly dependent on the Master ID allocation. Synchronous to UPA_CLK. Active high.
UPA_SC_REQ_IN	I	UltraSPARC-II system address bus arbitration request from the system. Used by UltraSPARC-I for the distributed UPA_ADDR arbitration protocol. Synchronous to UPA_CLK. Active high.
UPA_S_REPLY[4:0]	I	UltraSPARC-II system Reply packet, driven by System Controller to the UPA port. Synchronous to UPA_CLK. Active high.
UPA_DATA_STALL	I	Driven by System Controller to indicate whether there is a data stall. Active high.
UPA_P_REPLY[4:0]	O	UltraSPARC-II system reply packet, driven by UltraSPARC-II to the system. Synchronous to UPA_CLK. Active high.
UPA_DATA[127:0]	I/O	UPA Interconnect Data bus.
UPA_ECC[15:0]	I/O	ECC bits for the data bus. 8-bit ECC per 64-bits of data.
UPA_ECC_VALID	I	Driven by System Controller to indicate ECC is valid for the data on the UPA interconnect data bus. Active high.
UPA_REQ_OUT	O	Arbitration request from this module. Active high.
UPA_PORT_ID[1:0]	I	Module's identification signals. Active high.

Clock Interface

Signal	Type	Name and Function
UPA_CLK[1:0]_POS UPA_CLK[1:0]_NEG	I	UPA Interconnect Clock. Two copies are provided, one for the CPU and one for the UDBs.
CPU_CLK_POS CPU_CLK_NEG	I	Differential Clock inputs to the clock buffer on the module.
UPA_RATIO	I	Not used.
UPA_SPEED[2:0]	O	The most significant bit (UPA_SPEED[2]), together with a mother-board jumber, sets the UPA-to-CPU frequency ratio.

JTAG/Debug Interface

Signal	Type	Name and Function
TDO	O	IEEE 1149 test data output. A three-state signal driven only when that TAP controller is in the shift-DR state.
TDI	I	IEEE 1149 test data input. This pin is internally pulled to logic one when not driven.
TCLK	I	IEEE 1149 test clock input. This pin if not hooked to a clock source must always be driven to a logic 1 or a logic 0.
TMS	I	IEEE 1149 test mode select input. This pin is internally pulled to logic one when not driven. Active high.
TRST_L	I	IEEE 1149 test reset input (active low). This pin is internally pulled to logic one when not driven. Active low.

Initialization Interface

Signal	Type	Name and Function
UPA_RESET_L	I	Driven by System Controller for POR (power-on) resets and on fatal system reset. Asserted asynchronously. Deasserted synchronous to UPA_CLK. Active low.
UPA_XIR_L	I	Driven to signal externally initiated reset (XIR). Actually acts like a non-maskable interrupt. Synchronous to UPA_CLK. Active low, asserted for one clock cycle.

Misc. Signals

Signal	Type	Name and Function
TEMP_SENSE_NEG TEMP_SENSE_POS	O	Connected to a thermistor next to the CPU package.
POWER_SET_POS POWER_SET_NEG	O	POWER_SET_NEG is tied to GND on the module. POWER_SET_POS is connected to GND via a 1690-ohm resistor. Sets voltage of programmable supply.
POWER_OV	O	Connected to GND via an 1180-ohm resistor. Sets overvoltage level for programmable supply.

CLOCK DISTRIBUTION

- The JTAG TCLK signal is distributed to the UDB-II, the SRAMs and the UltraSPARC-II
- The two UDB-II chips on the module share a single UPA_CLK made up of UPA_CLK[1]_POS and UPA_CLK[1]_NEG
- The differential signal pair, UPA_CLK[0]_POS and UPA_CLK[0]_NEG, are connected to the UltraSPARC-II to generate a reference signal for determining the phase relationship between the CPU clock and UPA clock

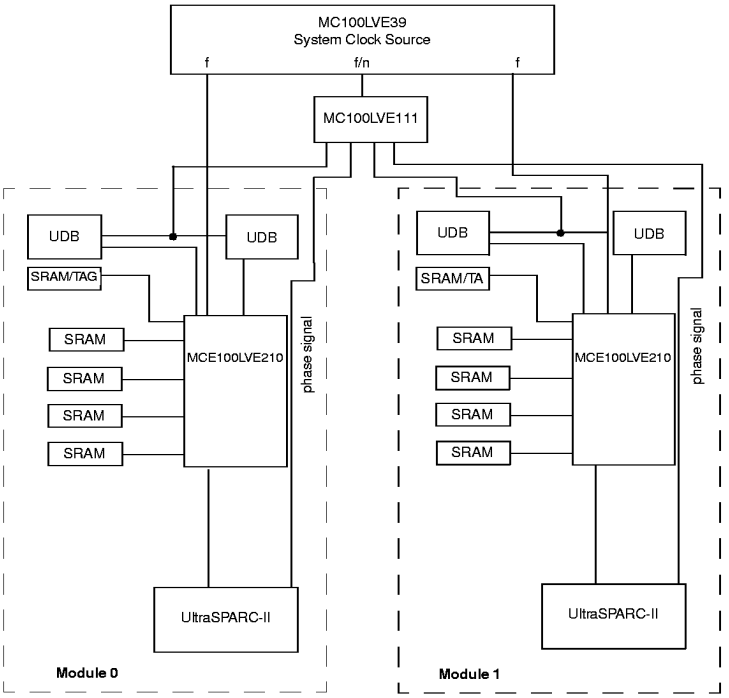


Figure 5. Module Clock Distribution

TABLE 1: Clock Skew for Clocks Provided to the Module

Clock Skew	Worst Case Skew
CPU clock to UDB-II E-Cache clock	500 ps
CPU clock to system ASIC clock	500 ps
UDB-II UPA clock to system ASIC clock	500 ps

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings[1]

Symbol	Parameter	Rating	Units
V_{DD}	Supply voltage range for I/O	0 to 3.8	V
V_{DD_CORE}	Supply voltage range for CPU core	0 to 3.0	V
V_I	Input voltage range[2]	-0.5 to V_{DD} + 0.5	V
V_O	Output voltage range	-0.5 to V_{DD} + 0.5	V
I_{IK}	Input clamp current (V_I < 0 - TBD or V_I > V_{DD} + TBD)	±20	mA
I_{OK}	Output clamp current (V_I < 0 - TBD or V_I > V_{DD} + TBD)	±50	mA
I_{OL}	Current into any output in the low state	50	mA
T_{STG}	Storage temperature	-20 to 125	°C

1. Operation of the device at values in excess of those listed above will result in degradation or destruction of the device. All voltages are defined with respect to ground. Functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. Unless otherwise noted, all voltages are with respect at V_{SS}.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Supply voltage for I/O	3.2	3.3	3.4	V
V_{DD_CORE}	Supply voltage for the CPU core	2.52	2.6	2.725	V
V_{SS}	Ground	–	0	–	V
V_{IH}	High-level input voltage	2.0	–	V_{DD} + 0.2	V
V_{IL}	Low-level input voltage	-0.3	–	0.8	V
I_{OH}	High-level output current	–	–	-4	mA
I_{OL}	Low-level output current	–	–	8	mA
T_J	Operating junction temperature	-	–	105	°C
T_A	Operating ambient temperature	-	-	-[1]	°C

1. Maximum ambient temperature is limited by air flow such that the maximum junction teperature does not exceed T_J . See Thermal Specifications on page 15.

DC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High-level output voltage	V_{DD} = Min, I_{OH} = Max	2.4	–	–	V
V_{IH}	High-level input voltage, PECL CLKs, UPA_CLK, & CPU_CLK		-	-	2.28	V
	High-level input voltage, except PECL CLKs, UPA_CLK, & CPU_CLK		-	-	2.0	V
V_{IL}	Low-level input voltage, PECL		1.49	-	-	V
	Low-level input voltage, except PECL		0.8	-	-	V
V_{OL}	Low-level output voltage	V_{DD} = Min, I_{OL} = Max	–	–	0.4	V
I_{DD}	Supply current for V_{DD}	V_{DD} = Max	–	5	7.54	A
I_{DD_CORE}	Supply current for V_{DD_CORE}	V_{DD_CORE} = MAX	–	9	11.94	A
I_{OZ}	High-impedance output current (Outputs without pull-ups)	V_{DD} = Max, V_O = 2.4 V	–	–	30	µA
		V_{DD} = Max, V_O = 0.4 V	–	–	-30	µA
	High-impedance output current (Outputs with pull-ups)	V_{DD} = Max, V_O = V_{SS} to V_{DD}	–	–	250	µA
I_I	Input current (inputs without pull-ups)	V_{DD} = Max, V_I = V_{SS} to V_{DD}	-20	–	20	µA
	Input current (inputs with pull-ups)	V_{DD} = Max, V_I = V_{SS} to V_{DD}	–	–	-250	µA
I_{OH}	High level output current		–	–	-4	mA
I_{OL}	Low level output current		–	–	8	mA

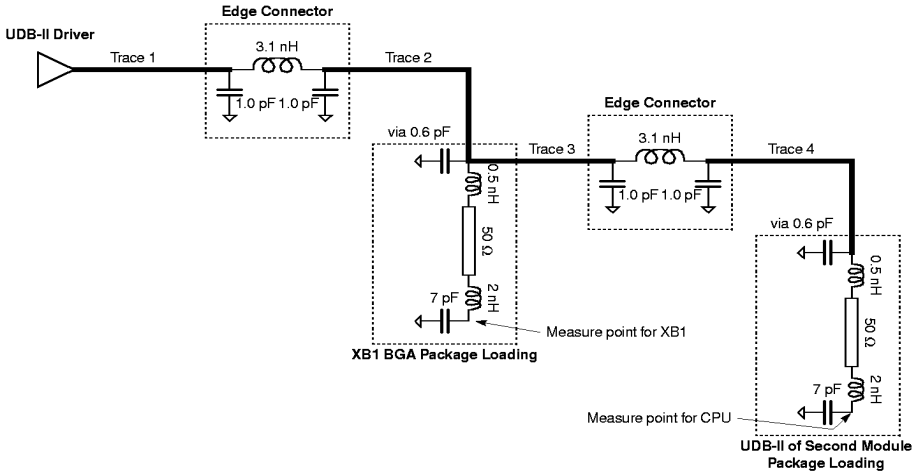
Power Consumption

The UltraSPARC-II module requires two V_{DD} supply voltages. V_{DD} and V_{DD_CORE} are currently required to be 3.3V and 2.6V, respectively. The V_{DD_CORE} supply should be programmable to allow for upgrades to higher speed modules. The estimated maximum power consumption of the STP5212 module is 58 watts @ 296 MHz.

TIMING SPECIFICATIONS

UPA Timing Specification

Preliminary timing specifications for the Module are specified at the edge connector pins in a typical system shown in *Figure 6*.



Worst Case: $Z_0 = 60\Omega$, $T_P = 180$ ps/inch, Trace 1 Length = 4.4″, Trace 2 Length = 0.6″, Trace 3 Length = 1.2″, Trace 4 Length = 4.4″

Best Case: $Z_0 = 50\Omega$, $T_P = 160$ ps/inch, Trace 1 Length = 2.2″, Trace 2 Length = 0.2″, Trace 3 Length = 0.2″, Trace 4 Length = 2.2″

Figure 6. Module System Loading for SYS_DATA, SYS_ECC

TABLE 2: Setup and Hold Time Specifications

Symbol	Description	Waveform	296 MHz		Unit
			Min	Max	
t_{SU}	UPA_DATA[127:0] setup time [1]	1	3.9	–	ns
t_{SU}	UPA_ADDR[35:0] setup time [2]	1	2.9	–	ns
t_{SU}	UPA_ECC[15:0] setup time [1]	1	3.9	–	ns
t_{SU}	UPA_S_REPLY[3:0] setup time [2]	1	4.4	–	ns
t_H	UPA_DATA[127:0] hold time[1]	1	0.7	–	ns
t_H	UPA_ADDR[35:0] hold time[2]	1	0.6	–	ns
t_H	UPA_ECC[15:0] hold time[1]	1	0.3	–	ns
t_H	UPA_S_REPLY[3:0] hold time[2]	1	0.6	–	ns

1. Signals referenced to UPA_CLK at the receiver IC input pin.
2. Signals referenced to CPU_CLK at the CPU input pin.

TABLE 3: Propagation Delay, Output Hold Time Specifications

Symbol	Description	Waveform	296 MHz		Unit
			Min	Max	
t_P	UPA_DATA[127:0] clk to out (see note 1 prev. table)	2	–	6.1	ns
t_P	UPA_ADDR[35:0] clk to out (see note 2 prev. table)	2	–	3.1	ns
t_P	UPA_ECC[15:0] clk to out (see note 1 prev. table)	2	–	6.1	ns
t_{OH}	UPA_DATA[127:0] clk out (see note 1 prev. table)	2	1.1	–	ns
t_{OH}	UPA_ADDR[35:0] clk out (see note 2 prev. table)	2	0.0	–	ns
t_{OH}	UPA_ECC[15:0] clk out (see note 1 prev. table)	2	1.4	–	ns

Timing Measurement Waveforms

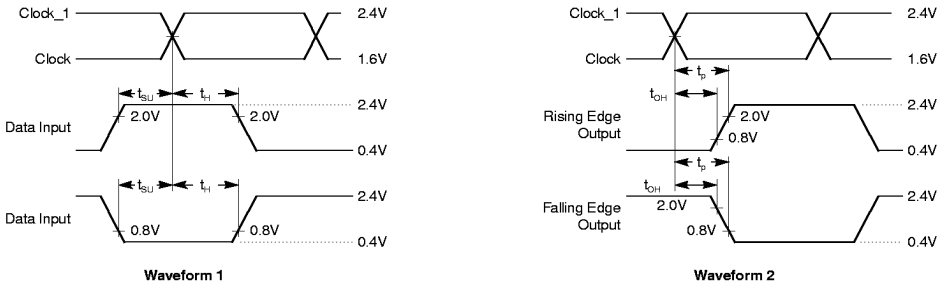


Figure 7. LVTTL Voltage Waveforms

MECHANICAL SPECIFICATIONS

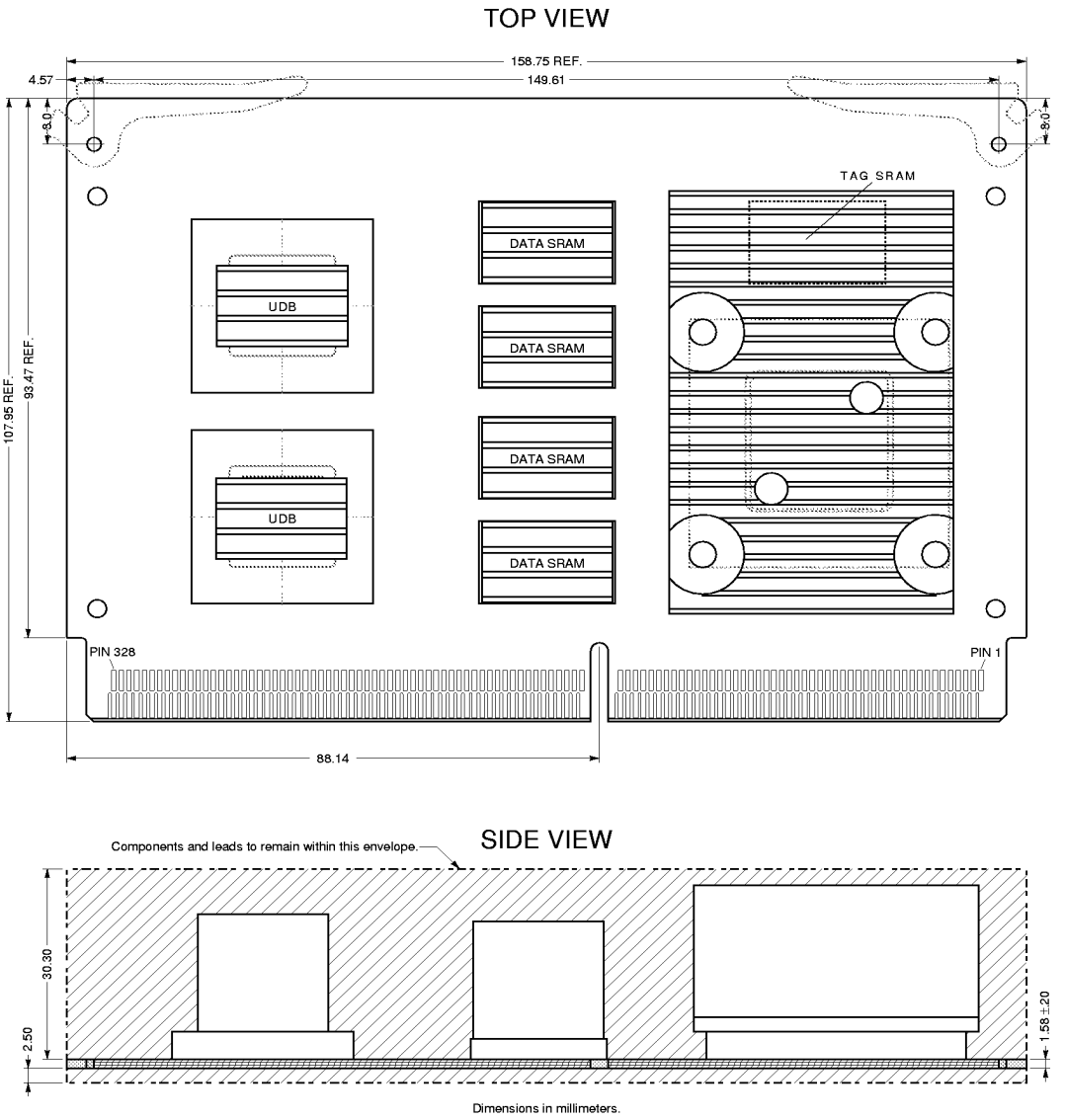


Figure 8. CPU Module Dimensions

THERMAL SPECIFICATIONS

The maximum junction temperature (T_j) specification is 105 ° C. This is equivalent to the maximum case temperature (T_C) of 89° C for the 296 MHz UltraSPARC-II CPU dissipating 31 watts (W) of power. T_C is defined at the center of the package heat spreader and can be obtained from the following relationship:

$$T_j = T_a + P_d \times (R_{jc} + R_{cs} + R_{sa})$$

where T_a is the ambient air temperature. P_d is the power dissipation.

The junction-to-case thermal resistance (R_{jc}) is approximately 0.6 °C/W for the 296 MHz UltraSPARC-II CPU.

The case-to sink thermal resistance (R_{cs}) is approximately 0.1 °C/W with the use of thermal grease between the heat sink and package.

The sink-to-air thermal resistances (R_{sa}) are listed in the following table:

Thermal Resistances

	Air Flow (ft/min)							
	150	200	296	400	500	650	800	1000
R_{sa}(°C/W)[1]	1.21	1.05	0.91	0.84	0.78	0.72	0.67	0.64

1. Ducted airflow for the heat sink 340-3537-03 (2.88" W x 1.85" L x 1" H).

T_j can also be calculated by measurement of the heat sink temperature (T_s) according to:

$$T_j = T_s + P_d \times (R_{jc} + R_{cs})$$

where T_s is measured in the heat sink base at the center of the CPU package.

TESTABILITY

The STP5211 UltraSPARC-II module implements the IEEE 1149.1 standard to aid in board level testing. Boundary Scan Description Language (BSDL) files are available for all the devices on the module, except the clock buffer.

AC Characteristics - JTAG Timing

Symbol	Parameter	Signals	Conditions	296 MHz			Units
				Min	Typ	Max	
t_W(TRST)	Test reset pulse width	TRST[1]		5	–	–	ns
t_{SU}(TDI)	Input setup time to TCK	TDI		–	3	–	ns
t_{SU}(TMS)	Input setup time to TCK	TMS		–	4	–	ns
t_H(TDI)	Input hold time to TCK	TDI		–	1.5	–	ns
t_H(TMS)	Input hold time to TCK	TMS		–	1.5	–	ns
t_{PD}(TDO)	Output delay from TCK[2]	TDO	I_{OL} = 8 mA	–	6	–	ns
t_{OH}(TDO)	Output hold time from TCK[2]	TDO	I_{OH} = -4 mA C_L = 35 pF V_{LOAD} = 1.5V	–	–	3	ns

1. TRST is an asynchronous reset.
2. TDO is referenced from falling edge of TCK.

JTAG (IEEE 1149.1) TIMING

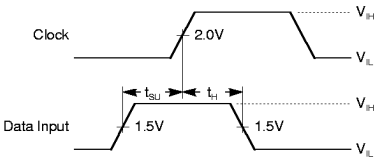


Figure 9. Voltage Waveforms - Setup and Hold Times

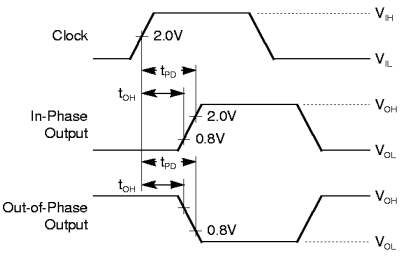


Figure 10. Voltage Waveforms - Propagation Delay Times

ORDERING INFORMATION

Part Number	Speed	Description
STP5212UPA-300	296 MHz CPU, 100 MHz UPA	296MHz CPU with a module system bus of 100MHz using UltraSPARC-II (STP1031), 2.0MB SRAMs, and UDB-IIs (STP1081).

Document Part Number: 805-0828-01