intel®

16.0 LOW POWER Intel486™ SX MICROPROCESSOR

Low Power Intel486™ SX CPU/ Intel487™ SX MCP

- Lower Power Dissipation
- — Dynamic Frequency Scalability
- — I_{CC}(max) Reduced to 150 mA at 2 MHz
- — Improved V_{CC} Rating (± 10%)
- Binary Compatible with Large Software Base
- — MS-DOS, OS/2, Windows
- — UNIX System V/386
- — iRMX, iRMK Kernels
- High Integration Enables On-Chip
- — 8 KByte Code and Data Cache
- — Floating Point Unit on the Intel487 SX Math CoProcessor
- — Paged, Virtual Memory Management
- Easy to Use
- — Built-In Self Test
- — Hardware Debugging Support
- — Intel Software Support
- — Extensive Third Party Software Support
- 168-Lead Pin Grid Array for Intel486 SX Microprocessor
- 196-Lead Plastic Quad Flat Package for Intel486 SX Microprocessor
- 169-Pin Grid Array Package for Intel487 SX Math CoProcessor
- High Performance Design
- — Intel486 One Clock Instruction Core
- — 16/20/25 MHz Operation for Intel486 SX
- — 64 MByte/Sec Burst Bus
- — CHMOS IV Process Technology
- — Dynamic Bus Sizing for 8-, 16- and 32-Bit Buses
- Complete 32-Bit Architecture
- — Address and Data Buses
- — Registers
- — 8-, 16- and 32-Bit Data Types
- Multiprocessor Support
- — Multiprocessor Instructions
- — Cache Consistency Protocols
- — Support for Second Level Cache

This section describes the Low Power Intel486 SX microprocessor. The Intel487 Math CoProcessor will support the low power Intel486 SX microprocessor as an optional upgrade available through the retail channel.

The Low Power Intel486 family microprocessors meet today's need for high performance portables. Their combination of special features like dynamic frequency scaling, lower minimum frequency, improved V_{CC} operation and high integration contribute significantly to lower power dissipation and meet the needs of portable computing.

The Low Power capability is achieved by operating the Intel486 microprocessor in the 2X mode. The frequency can be varied dynamically between maximum to minimum as needed. The frequency change does not affect contents of the registers and data integrity is maintained. Power dissipation is reduced significantly at 2 MHz where I_{CC} is only 150 mA compared to 600 mA at 20 MHz.

The Low Power Intel486 microprocessors are 100-percent compatible with all versions of the Intel386 microprocessor family, assuring compatibility with the more than $40 billion software base of MS-DOS, Windows, OS/2 and UNIX/System operating system applications. The Low Power Intel486 microprocessor integrates the same RISC-technology, one clock per instruction integer core, on-chip cache, and memory management unit as the standard Intel486 microprocessor.

The Intel487 Math CoProcessor provides optional math upgrade capability for the Intel486 SX microprocessor and supports low power operation; providing end-users increased floating point performance for more than 2100 software packages that were designed to use Intel Math CoProcessors. Note that the Intel OverDrive Processor does not work in systems based on the Low Power Intel486 CPU.

The following section on the Low Power Intel 486 SX microprocessor contains information specific to the Low Power device only. All data not defined are located in the appropriate sections of this data sheet unless specified otherwise.

16.1 Introduction

The Low Power Intel486 microprocessor brings Intel486 technology and performance to the portable computer market. The low power capability is achieved by a frequency scalability feature during normal operation. The operating frequency can be brought down dynamically resulting in lower power supply current (I_{CC}). This results in minimal power dissipation which ensures a longer battery life.

2

The Low Power Intel486 microprocessor integrates the same RISC-technology, one clock per instruction integer core, on-chip cache, and memory management unit as the standard Intel486 microprocessor.

The Low Power Intel486 microprocessor has the following special features:

- **Frequency Scalability**—This is achieved by operating the Intel486 microprocessor in the 2X clock mode. The frequency can be varied dynamically from maximum back to minimum or vice versa. The frequency change does not affect the register content of the CPU, thus data integrity is maintained.

- **Lower Minimum Frequency**—The Low Power Intel486 microprocessor can be operated at a minimum frequency of 2 MHz, at which I_{CC}(max) is only 150 mA, compared to an I_{CC}(max) of 600 mA at 20 MHz operation. The power dissipation is thus drastically reduced ensuring a longer battery life.

- **Improved V_{CC} Operation**—The Low Power Intel486 microprocessor has an improved V_{CC} rating of ±10%. Again this feature makes it extremely attractive to portable battery powered applications.

The above three features ensure power savings for portable computer systems resulting in prolonged battery life.

Besides these special features, the Low Power Intel486 microprocessor has an identical feature set to the standard Intel486 CPU. This includes:

- **Binary Compatibility**—The Low Power Intel486 CPU is binary compatible with the 8086, 8088, 80186, 80286, i386™ SX, i386™ DX, Intel486™ SX and Intel486™ DX CPUs.

- **Full 32-Bit Integer Processor**—The Low Power Intel486 CPU performs a complete set of arithmetic and logical operations on 8-, 16-, and 32-bit data types using a full-width ALU and eight general-purpose registers.

- **Separate 32-Bit Address and Data Paths**— Four gigabytes of physical memory can be addressed directly.

- **Single-Cycle Execution**—Many instructions execute in a single clock cycle.

- **On-Chip Floating Point Unit**—This is available on the Intel486 DX CPU. The 32-, 64-, and 80-bit formats specified in IEEE standard 754 are supported. The unit is binary compatible with the 8087, 80287, i387™, i387™ SX, and Intel Over-Drive Processor and the Intel486™ CPU.

- **On-Chip Memory Management Unit**—Address-management and memory-space protection mechanisms maintain the integrity of memory. This is necessary in multitasking and virtual-memory environments, like those implemented by the UNIX and OS/2 operating systems. Both memory segmentation and paging are supported.

- **On-Chip Cache with Cache Consistency Support**—The internal write-through cache can hold 8 KBytes of data or instructions. Cache hits are as fast as read accesses to a processor register. Bus activity is tracked to detect alterations in the memory which internal cache represents. The internal cache can be invalidated or flushed, so that an external cache controller can maintain cache consistency in multi-processor environments.

- **External Cache Control**—Write-back and flush controls over an external cache are provided so that the processor can maintain cache consistency in multi-processor environments.

- **Instruction Pipelining**—The fetching, decoding, execution and address translation of instructions are overlaped within the Low Power Intel486 microprocessor. This results in a continuous execution rate of one clock cycle per instruction, for most instructions.

- **Burst Cycles**—Burst transfers allow a new doubleword to be read from memory each clock cycle. With this capability the internal cache and instruction prefetch buffer can be filled very rapidly.

- **Write Buffers**—The processor contains write buffers to enhance the performance of consecutive writes to memory. The Low Power Intel486 CPU can continue operations internally after a write, without waiting for the write to be executed on the external bus.

- **Bus Backoff**—If another bus master needs control of the bus during a Low Power Intel486 microprocessor initiated bus cycle, the Low Power Intel486 microprocessor will float its bus signals, then restart its cycle when the bus becomes available again.

- **Instruction Restart**—Programs can continue execution following an exception generated by an unsuccessful attempt to access memory. This feature is important for supporting demand-paged virtual memory applications.

- **Dynamic Bus Sizing**—External controllers can dynamically alter the effective width of the data bus. Bus widths of 8, 16 or 32 bits can be used.

intel.

16.2 Pinout

The Low Power Intel486™ SX microprocessor pinout follows the same definition as the Intel486™ SX microprocessor given in Section 1.0, except for the pins listed in Table 16.1.

Table 16.1

i486 SX Microprocessor	Low Power i486 Microprocessor	Pin # PGA	Pin # PQFP
CLK	CLK2	C3	123
NC	CLKSEL	A3	127
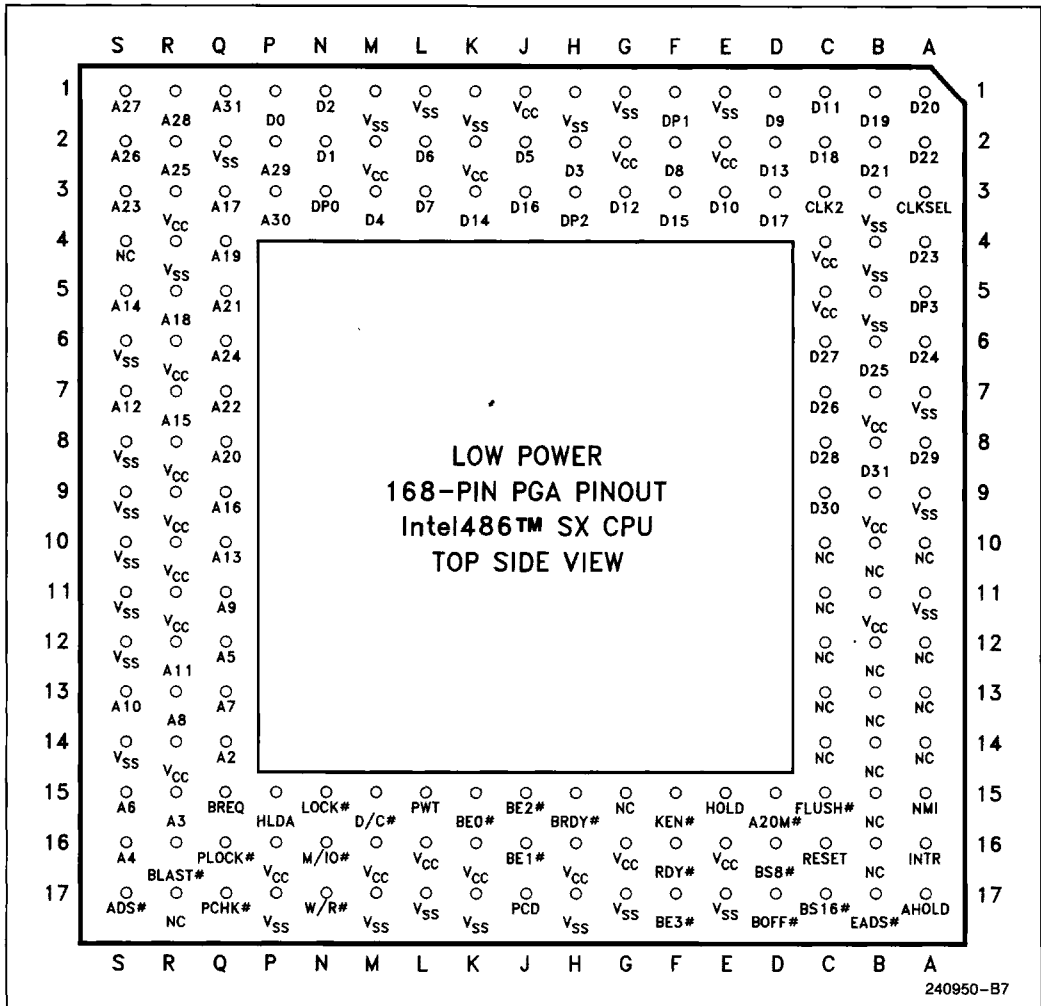
Figure 16-1. Low Power Intel486™ SX CPU Pinout (Top Side View)

Pinout grid (Top Side View), columns S R Q P N M L K J H G F E D C B A, rows 1–17:

	S	R	Q	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1	A27	A28	A31	D0	D2	Vss	Vss	Vss	Vcc	Vss	Vss	DP1	Vss	D9	D11	D19	D20
2	A26	A25	Vss	A29	D1	Vcc	D6	Vcc	D5	D3	Vcc	D8	Vcc	D13	D18	D21	D22
3	A23	Vcc	A17	A30	DP0	D4	D7	D14	D16	DP2	D12	D15	D10	D17	CLK2	Vss	CLKSEL
4	NC	Vss	A19												Vcc	Vss	D23
5	A14	A18	A21												Vcc	Vss	DP3
6	Vss	Vcc	A24												D27	Vss	D24
7	A12	A15	A22												D26	Vcc	Vss
8	Vss	Vcc	A20												D28	D31	D29
9	Vss	Vcc	A16												D30	Vcc	Vss
10	Vss	Vcc	A13												NC	NC	NC
11	Vss	Vcc	A9												NC	Vcc	Vss
12	Vss	A11	A5												NC	NC	NC
13	A10	A8	A7												NC	NC	NC
14	Vss	Vcc	A2												NC	NC	NC
15	A6	A3	BREQ	HLDA	LOCK#	D/C#	PWT	BE0#	BE2#	BRDY#	NC	KEN#	HOLD	A20M#	FLUSH#	NC	NMI
16	A4	BLAST#	PLOCK#	Vcc	M/IO#	Vcc	Vcc	BE0#	BE1#	Vcc	Vcc	RDY#	Vcc	BS8#	RESET	NC	INTR
17	ADS#	NC	PCHK#	Vss	W/R#	Vss	Vss	PCD	Vss	Vss	BE3#	Vss	BOFF#	BS16#	EADS#	AHOLD

Center text: LOW POWER 168-PIN PGA PINOUT Intel486™ SX CPU TOP SIDE VIEW

240950-B7

intel®

```
        A    B    C    D    E    F    G    H    J    K    L    M    N    P    Q    R    S
   1   D20  D19  D11  D9   VSS  DP1  VSS  VSS  VCC  VSS  VSS  VSS  D2   D0   A31  A28  A27   1
   2   D22  D21  D18  D13  VCC  D8   VCC  D3   D5   D6   VCC  D1   A29  VSS  A25  A26        2
   3  CLKSEL VSS CLK2 D17  D10  D15  D12  DP2  D16  D14  D7   D4   DPO  A30  A17  VCC  A23   3
   4   D23  VSS  VCC                                                    A19  VSS  NC        4
   5   DP3  VSS  VCC                                                    A21  A18  A14       5
   6   D24  D25  D27                                                    A24  VCC  VSS       6
   7   VSS  VCC  D26                                                    A22  A15  A12       7
   8   D29  D31  D28              LOW POWER                             A20  VCC  VSS       8
   9   VSS  VCC  D30           168-PIN PGA PINOUT                       A16  VCC  VSS       9
  10   NC   NC   NC            Intel486™ SX CPU                         A13  VCC  VSS      10
  11   VSS  VCC  NC             PIN SIDE VIEW                           A9   VCC  VSS      11
  12   NC   NC   NC                                                     A5   A11  VSS      12
  13   NC   NC   NC                                                     A7   A8   A10      13
  14   NC   NC   NC                                                     A2   VCC  VSS      14
  15  NMI   NC  FLUSH# A20M# HOLD KEN# NC  BRDY# BE2# BE0# PWT  D/C# LOCK# HLDA BREQ A3  A6 15
  16  INTR  NC  RESET BS8# VCC RDY# VCC BE1# VCC VCC VCC M/IO# VCC PLOCK# BLAST# A4       16
  17  AHOLD EADS# BS16# BOFF# VSS BE3# VSS VSS PCD VSS VSS VSS W/R# VSS PCHK# NC  ADS#    17
        A    B    C    D    E    F    G    H    J    K    L    M    N    P    Q    R    S
```

240950-B8

Figure 16-2. Low Power Intel486™ SX CPU Pinout (Pin Side View)

Figure 16-3. Low Power Intel486™ SX CPU 196-Lead PQFP Pinout

16.3 Pin Cross Reference (Intel486™ PGA Version)

Address		Data		Control		N/C	V_CC	V_SS
A_2	Q14	D_0	P1	A20M#	D15	A10	B7	A7
A_3	R15	D_1	N2	ADS#	S17	A12	B9	A9
A_4	S16	D_2	N1	AHOLD	A17	A13	B11	A11
A_5	Q12	D_3	H2	BE0#	K15	A14	C4	B3
A_6	S15	D_4	M3	BE1#	J16	B10	C5	B4
A_7	Q13	D_5	J2	BE2#	J15	B12	E2	B5
A_8	R13	D_6	L2	BE3#	F17	B13	E16	E1
A_9	Q11	D_7	L3	BLAST#	R16	B14	G2	E17
A_{10}	S13	D_8	F2	BOFF#	D17	B16	G16	G1
A_{11}	R12	D_9	D1	BRDY#	H15	C10	H16	G17
A_{12}	S7	D_{10}	E3	BREQ	Q15	C11	J1	H1
A_{13}	Q10	D_{11}	C1	BS8#	D16	C12	K2	H17
A_{14}	S5	D_{12}	G3	BS16#	C17	C13	K16	K1
A_{15}	R7	D_{13}	D2	CLK2	C3	G15	L16	K17
A_{16}	Q9	D_{14}	K3	CLKSEL	A3	R17	M2	L1
A_{17}	Q3	D_{15}	F3	D/C#	M15	S4	M16	L17
A_{18}	R5	D_{16}	J3	DP0	N3		P16	M1
A_{19}	Q4	D_{17}	D3	DP1	F1		R3	M17
A_{20}	Q8	D_{18}	C2	DP2	H3		R6	P17
A_{21}	Q5	D_{19}	B1	DP3	A5		R8	Q2
A_{22}	Q7	D_{20}	A1	EADS#	B17		R9	R4
A_{23}	S3	D_{21}	B2	FERR#	C14		R10	S6
A_{24}	Q6	D_{22}	A2	FLUSH#	C15		R11	S8
A_{25}	R2	D_{23}	A4	HLDA	P15		R14	S9
A_{26}	S2	D_{24}	A6	HOLD	E15			S10
A_{27}	S1	D_{25}	B6	IGNNE#	A15			S11
A_{28}	R1	D_{26}	C7	INTR	A16			S12
A_{29}	P2	D_{27}	C6	KEN#	F15			S14
A_{30}	P3	D_{28}	C8	LOCK#	N15			
A_{31}	Q1	D_{29}	A8	M/IO#	N16			
		D_{30}	C9	NMI	B15			
		D_{31}	B8	PCD	J17			
				PCHK#	Q17			
				PWT	L15			
				PLOCK#	Q16			
				RDY#	F16			
				RESET	C16			
				W/R#	N17			

16.4 Pin Cross Reference by Signal Type (Intel486™ SX CPU) (PQFP Version)

Address		Data		Control		N/C	V_{CC}	V_{SS}
A_2	146	D_0	17	A20M#	104	15	6	1
A_3	150	D_1	18	ADS#	145	34	19	11
A_4	152	D_2	20	AHOLD	129	52	24	21
A_5	152	D_3	23	BE0#	117	56	28	22
A_6	158	D_4	25	BE1#	116	60	36	33
A_7	159	D_5	26	BE2#	115	64	49	40
A_8	161	D_6	27	BE3#	113	68	54	50
A_9	163	D_7	29	BLAST#	144	72	62	58
A_{10}	165	D_8	31	BOFF#	137	73	70	66
A_{11}	172	D_9	32	BRDY#	138	75	84	86
A_{12}	174	D_{10}	35	BREQ	118	76	93	95
A_{13}	176	D_{11}	37	BS8#	135	77	98	96
A_{14}	178	D_{12}	38	BS16#	136	78	107	99
A_{15}	180	D_{13}	39	CLK2	123	79	112	109
A_{16}	181	D_{14}	41	CLKSEL	127	81	119	114
A_{17}	183	D_{15}	42	D/C#	110	82	125	121
A_{18}	189	D_{16}	44	DP0	16	83	131	126
A_{19}	191	D_{17}	45	DP1	30	85	147	141
A_{20}	193	D_{18}	46	DP2	43	87	164	148
A_{21}	2	D_{19}	47	DP3	57	88	170	167
A_{22}	3	D_{20}	48	EADS#	105	89	175	168
A_{23}	4	D_{21}	51	FLUSH#	102	90	179	177
A_{24}	5	D_{22}	53	HLDA	122	91	184	182
A_{25}	7	D_{23}	55	HOLD	130	92	196	194
A_{26}	8	D_{24}	59	INTR	101	94		
A_{27}	9	D_{25}	61	KEN#	132	97		
A_{28}	10	D_{26}	63	LOCK#	142	124		
A_{29}	12	D_{27}	65	M/IO#	111	134		
A_{30}	13	D_{28}	67	NMI	100	140		
A_{31}	14	D_{29}	69	PCD	106	149		
		D_{30}	71	PCHK#	139	151		
		D_{31}	74	PWT	108	153		
				PLOCK#	143	155		
				RDY#	133	157		
				RESET	103	160		
				TCK	128	162		
				TDI	185	166		
				TDO	80	166		
				TMS	187	169		
				UP#	156	171		
				W/R#	120	173		
						186		
						188		
						190		
						192		
						195		

16.5 Pin Description

All pin descriptions for the Low Power Intel486 SX microprocessor follow the same definition as the Intel486 SX microprocessor with the exception of those listed in Table 16.2.

Table 16.2

Symbol	Type	Name and Function
CLK2	I	**CLK2** provides the fundamental timing for the Low Power Intel486 SX microprocessor. This is twice the internal frequency of the CPU.
CLKSEL	I	**CLOCK SELECT** pin selects the 2X mode required for the Low Power Intel486 SX CPU. A well defined pulse on this pin establishes the phase relationship of the 2X clock. With the exception of a pulse during cold reset, this pin should be driven low at all times and must be free of spikes or glitches.

OUTPUT PINS

Table 16.3 lists all the output pins, indicating their active level, and when they are floated.

Table 16.3. Output Pins

Name	Active Level	When Floated
BREQ	HIGH	
HLDA	HIGH	
BE0# – BE3#	LOW	Bus Hold
PWT, PCD	HIGH	Bus Hold
W/R#, D/C#, M/IO#	HIGH/LOW	Bus Hold
LOCK#	LOW	Bus Hold
PLOCK#	LOW	Bus Hold
ADS#	LOW	Bus Hold
BLAST#	LOW	Bus Hold
PCHK#	LOW	
FERR# *	LOW	
A2-A3	HIGH	Bus, Address Hold

*Present on Intel486 DX CPU Only

INPUT PINS

Table 16.4 lists all input pins, indicating their active level, and whether they are synchronous or asynchronous inputs.

Table 16.4. Input Pins

Name	Active Level	Synchronous/ Asynchronous
CLK2		
CLKSEL		
RESET	HIGH	Asynchronous
HOLD	HIGH	Synchronous
AHOLD	HIGH	Synchronous
EADS#	LOW	Synchronous
BOFF#	LOW	Synchronous
FLUSH#	LOW	Asynchronous
A20M#	LOW	Asynchronous
BS16#, BS8#	LOW	Synchronous
KEN#	LOW	Synchronous
RDY#	LOW	Synchronous
BRDY#	LOW	Synchronous
INTR	HIGH	Asynchronous
NMI	HIGH	Asynchronous
IGNNE# *(1)	LOW	Asynchronous
UP#(2)	LOW	Asynchronous

NOTES:
1. The IGNNE# pin is present on the Intel486 DX CPU and Intel487 SX MCP only.
2. The UP# pin is present on the Intel486 SX CPU PQFP package only.

intel®

INPUT/OUTPUT PINS

Table 16.5 lists all the input/output pins, indicating their active level and when they are floated.

Table 16.5. Input/Output Pins

Name	Active Level	When Floated
D0–D31	HIGH	Bus Hold
DP0–DP3	HIGH	Bus Hold
A4–A31	HIGH	Bus, Address Hold

Table 16.6. Test Pins

Name	Input or Output	Sampled/ Driven On
TCK	Input	N/A
TDI	Input	Rising Edge of TCK
TDO	Output	Falling Edge of TCK
TMS	Input	Rising Edge of TCK

Table 16.7. Component and Revision ID (PGA)

i486 SX Microprocessor Stepping Name	Component ID	Revision ID
A0	04	20
B0	04	22

NOTE:
Table 16.7 shows the Component ID number and Revision ID number for the A-0 stepping of the Intel486 SX Micropocesor and Intel OverDrive Processor. When an Intel OverDrive Processor is installed in the system, the Component ID and Revision ID is provided by the Intel OverDrive Processor and not the Intel486 SX Microprocessor. The Component ID and Revision ID read by the BIOS/software may change when a Performance Upgrade Component, such as the Intel OverDrive Processor, is installed in an Intel486 SX Microprocessor based system.

16.6 Signal Description

With the exception of CLK2 and CLKSEL, all signals follow the same definition as the Intel486 microprocessor. The A.C. timing parameters for all of these signals are given in Tables 16.11–16.13.

CLOCK (CLK2)

CLK2 provides the fundamental timing for the Low Power Intel486 microprocessor. It is divided by two internally to generate the internal processor clock used for instruction execution. The internal clock is comprised of two phases, "phase one" and "phase two". Each CLK2 period is a phase of the internal clock. Figure 15.4 illustrates the relationship. If desired, the phase of the internal processor clock can be synchronized to a known phase by ensuring the pulse on the CLKSEL pin meets the applicable timings during cold boot (power-up reset).

All set-up, hold, float-delay and valid delay timings are referenced to the phase one of the clock.

The internal processor clock (CLK) is similar to the clock signal of the standard Intel486 microprocessor. All I/O signals get sampled on the rising edge of this signal, i.e. the rising edge of phase one. Thus it is important to synchronize the external circuitry with the phase one of CLK2.

2

CLKSEL

Clock Select pin selects the 2X mode required for the Low Power Intel486 CPU. This pin should be driven low after power-up and during the entire operation of the CPU. However, a well defined pulse is required on CLKSEL pin during cold boot (power-up reset) to establish the phase relationship of the 2X clock. The reset pulse width during cold reset should be at least 1 ms. As shown in Figure 16.5, the pulse on CLKSEL should be asserted by the end of reset (approximately 0.9 ms after driving reset active) and at least 30 CLK2 periods before the falling edge of reset.

Figure 16.6 shows the detailed timing definition of this pulse. The pulse on CLKSEL pin is only required during power-up reset. During all other times including warm resets the CLKSEL pin should be driven low and must be free of spikes or glitches. After the power-up reset, the system must track the phase of CLK2 at all times including during warm resets so that the input/output signals can be sampled at the appropriate clock edge. The phase relationship is described in the next section.
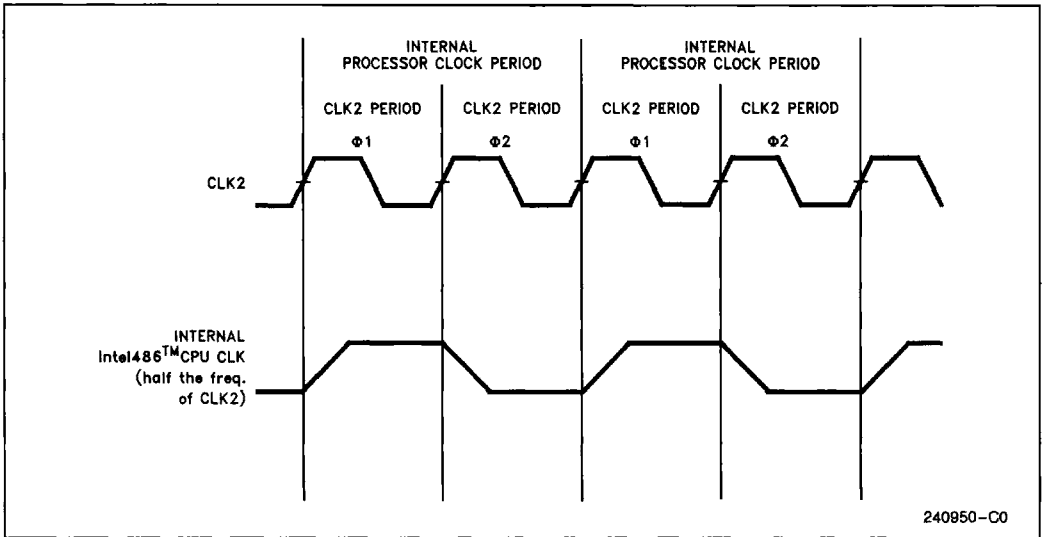
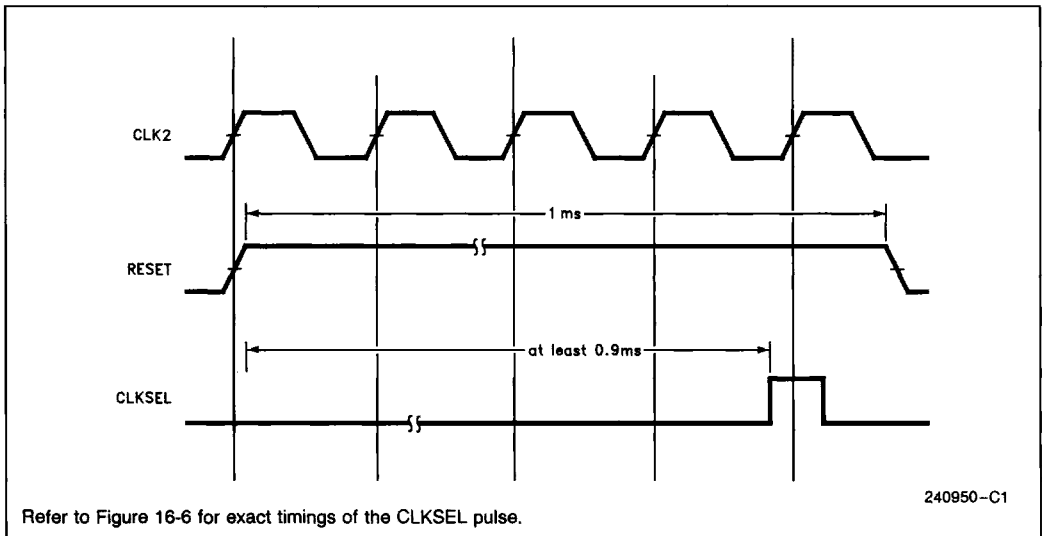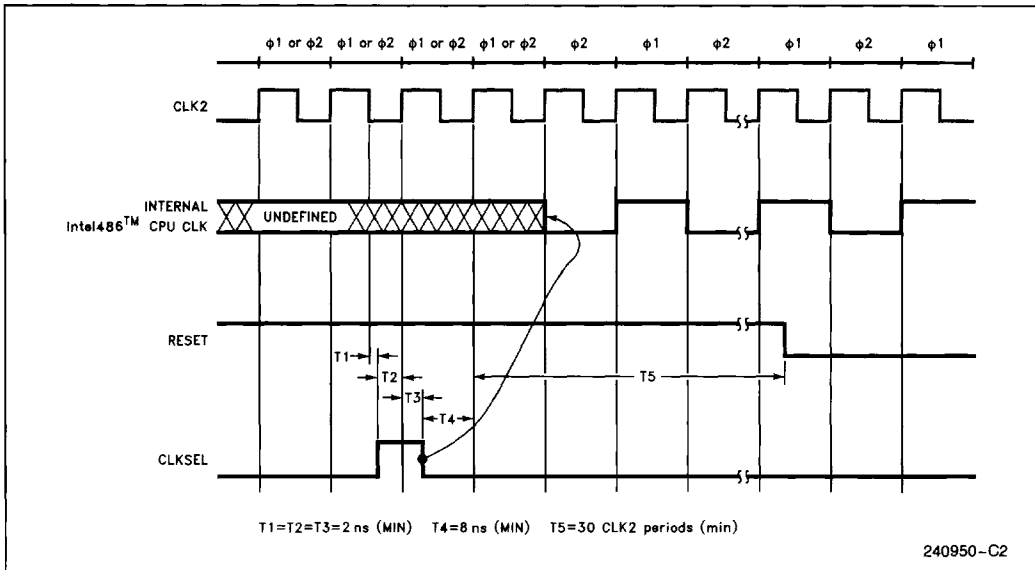**Figure 16.4. CLK2 Signal and Internal Processor Clock**

Refer to Figure 16-6 for exact timings of the CLKSEL pulse.

Figure 16.5. CLKSEL Pulse with Reference to the Reset Pulse Width

T1=T2=T3=2 ns (MIN)   T4=8 ns (MIN)   T5=30 CLK2 periods (min)

240950-C2

Figure 16.6. CLKSEL Timing Definition during Power-Up Reset

16.7 Architecture Overview

The Low Power Intel486 SX microprocessor is architecturally similar to the Intel486 SX CPU. Thus all bus cycles follow the same definition. The difference lies in the fact that the Low Power Intel486 SX CPU works with an external 2X clock input (CLK2). As shown in Figure 16.4, each of the internal processor clock (CLK) cycles is two CLK2 cycles wide. Thus a 25 MHz Low Power Intel486 microprocessor needs a 50 MHz clock input.

CLK2 provides the fundamental timing for the Low Power Intel486 SX CPU. It is divided by two internally to generate the internal processor clock (CLK) used for instruction execution. The internal clock is comprised of two phases, "phase one" and "phase two". Each CLK2 period is a phase of the internal clock. All Low Power Intel486 SX microprocessor inputs are sampled at the rising edge of phase 1. Each bus cycle is comprised of at least two bus states, T1 and T2. Each bus state in turn consists of two CLK2 cycles phase 1 and phase 2 of the bus state. The bus state diagram in Section 7.2.13 is valid for the Low Power Intel486 SX microprocessor.

NOTE:
The timing diagrams given for the Intel486 SX can be used for the Low Power Intel486 SX microprocessor. Read "CLK" signal as the internal clock of the CPU, with "CLK2" (the input clock of the Low Power Intel486 CPU) being twice the frequency of the internal processor clock as shown in Figure 16.4.

The following describes how the input signals are sampled and output signals are referenced with respect to the input clock (CLK2):

INPUT SIGNALS

The Low Power Intel486 SX CPU samples all its **synchronous** input signals (i.e., RDY#, BRDY#, BS8#, BS16#, KEN#, EADS#, BOFF#, HOLD and AHOLD) at the rising edge of phase 1, as long as proper setup and hold times relative to that clock edge are met.

The Low Power Intel486 SX CPU samples all its **asynchronous** input signals (i.e., RESET, INTR, NMI, A20M# FLUSH#, IGNNE#) at every other rising edge of the system clock (Phase 1), as long as proper setup and hold times relative to that clock edge are met.

OUTPUT SIGNALS

The A.C. timing specifications for output signals (i.e., valid and float delay timings) are specified with respect to the rising edge of the Phase 1 of the system clock. This holds true for all output signals including ADS# and PCHK#.

2

16.8 Variable CPU Frequency

The Low Power Intel486 SX microprocessor allows the CPU frequency to change dynamically. As shown in Figures 16.7 and 16.8, the relationship between frequency and power consumption is approximately linear. Thus lowering the CPU frequency, reduces the power supply current (I_{CC}) consumed by the CPU.

The following must be satisified to change the CPU frequency:

1. Frequency can be changed at least 8 clocks after satisfying t4 (see Figure 16.6). The system can be started at a lower frequency and after satisfying the CLKSEL pulse specifications, it can be operated at the required speed.

2. The change in frequency should satisfy the minimum specification of "CLK2 high time" and "CLK2 low time". That is, at no time should the clock period go below the specified clock high and clock low times (see A.C. specifications for exact values).
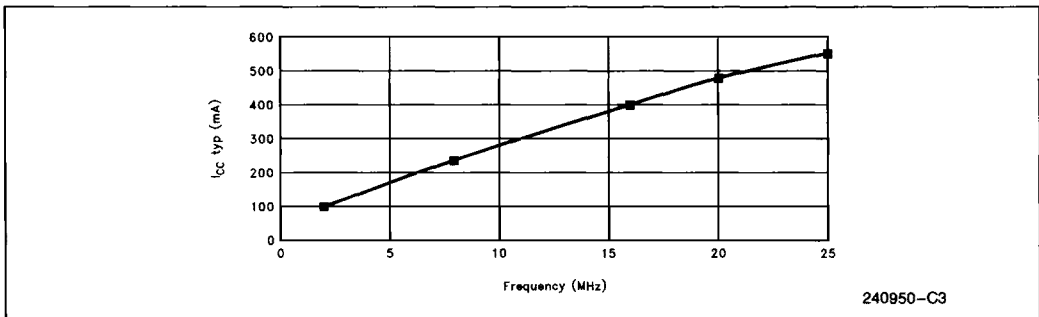
Figure 16.7. Frequency vs I_{CC}(typ) (PGA Version)
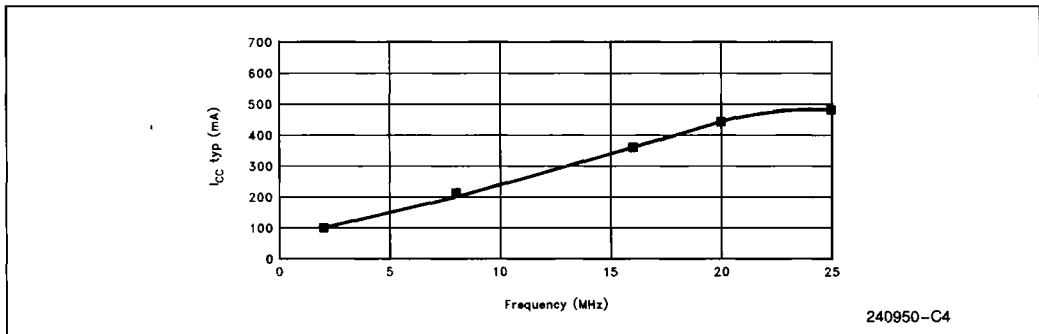
Figure 16.8. Frequency vs I_{CC}(typ) (PQFP Version)

16.9 D.C./A.C. Specifications

Table 16.6 provides the absolute maximum ratings. It is a stress rating only and functional operation at the maximums is not guaranteed. Functional operating conditions are given in Section 16.9.1 D.C. Specifications and 16.9.3 A.C. Specifications.

Table 16.6. Absolute Maximum Ratings

Case Temperature under Bias	$-65°C$ to $+110°C$
Storage Temperature	$-65°C$ to $+150°C$
Voltage on Any Pin with Respect to Ground	$-0.5V$ to ($V_{CC} + 0.5V$)
Supply Voltage with Respect to V_{SS}	$-0.5V$ to $+6.5V$

16.9.1 D.C. SPECIFICATIONS

Table 16.7 provides the D.C. operating conditions for the Low Power Intel486 SX microprocessor (PGA Version) and the Intel487 SX Math CoProcessor installed in a low power system.

Functional Operating Range: $V_{CC} = 5V \pm 10\%$; $T_{case} = 0°C$ to $+85°C$.

Table 16.7. Low Power Intel486 SX Microprocessor D.C. Parametric Values (PGA Version)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	-0.3	$+0.8$	V	
V_{IH}	Input High Voltage	2.0	$V_{CC} + 0.3$	V	
V_{OL}	Output Low Voltage		0.45	V	(Note 1)
V_{OH}	Output High Voltage	2.4		V	(Note 2)
I_{CC}	Power Supply Current CLK2 = 32 MHz = 40 MHz = 50 MHz		525 600 700	mA	(Note 3)
I_{CCF}	Power Supply Current with Intel486 SX CPU Tri-stated (floating) CLK2 = 32 MHz = 40 MHz = 50 MHz		400 500 600	mA	
I_{LI}	Input Leakage Current		± 15	μA	(Note 4)
I_{IH}	Input Leakage Current		200	μA	(Note 5)
I_{IL}	Input Leakage Current		-400	μA	(Note 6)
I_{LO}	Output Leakage Current		± 15	μA	
C_{IN}	Input Capacitance		20	pF	$F_C = 1$ MHz[7]
C_O	I/O or Output Capacitance		20	pF	$F_C = 1$ MHz[7]
C_{CLK}	CLK Capacitance		20	pF	$F_C = 1$ MHz[7]

NOTES:
1. This parameter is measured at:
   Address, Data BEn 4.0 mA
   Definition, Control 5.0 mA
2. This parameter is measured at:
   Address, Data BEn -1.0 mA
   Definition, Control -0.9 mA
3. Typical supply current
   I_{CC} = 400 @CLK2 = 32 MHz (Normal Operation)
   = 475 mA @CLK2 = 40 MHz
   = 500 mA @CLK2 = 50 MHz
   I_{CCF} = 325 mA @CLK2 = 32 MHz Intel486 CPU Tri-stated (Floating)
   = 400 mA @CLK2 = 40 MHz
   = 470 mA @CLK2 = 50 MHz
4. This parameter is for inputs without pullups or pulldowns and $0 \leq V_{IN} \leq V_{CC}$.
5. This parameter is for inputs with pulldowns and $V_{IH} = 2.4V$.
6. This parameter is for inputs with pullups and $V_{IL} = 0.45V$.
7. Not 100% tested.

Table 16.8 provides the D.C. Operating Conditions for the Low Power Intel486 SX microprocessor (PQFP version) and the Intel487 SX Math CoProcessor installed in a low power system.

Functional Operating Range: V_{CC} = 5V − 10%, +5%; T_{case} = 0°C to +85°C

Table 16.8. Low Power Intel486™ SX Microprocessor D.C. Parametric Values (PQFP version)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IL}	Input Low Voltage	−0.3	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.3	V	
V_{OL}	Output Low Voltage		0.45	V	(Note 1)
V_{OH}	Output High Voltage	2.4		V	(Note 2)
I_{CC}	Power Supply Current CLK2 = 32 MHz CLK2 = 40 MHz CLK2 = 50 MHz		450 500 560	mA	(Note 3)
I_{CCF}	Power Supply Current with Intel486 SX CPU in Power Down Mode		50	mA	(Note 7)
I_{LI}	Input Leakage Current		±15	μA	(Note 4)
I_{IH}	Input Leakage Current		200	μA	(Note 5)
I_{IL}	Input Leakage Current		−400	μA	(Note 6)
I_{LO}	Output Leakage Current		±15	μA	
C_{IN}	Input Capacitance		10	pF	F_C = 1 MHz[7]
C_O	I/O or Output Capacitance		10	pF	F_C = 1 MHz[7]
C_{CLK}	CLK Capacitance		6	pF	F_C = 1 MHz[7]

NOTES:
1. This parameter is measured at:
   Address, Data, BEn   4.0 mA
   Definition, Control   5.0 mA
2. This parameter is measured at:
   Address, Data BEn   −1.0 mA
   Definition, Control   −0.9 mA
3. Typical supply current:
   I_{CC} 380 mA @ CLK2 = 32 MHz (Normal Operation)
        440 mA @ CLK2 = 40 MHz
        480 mA @ CLK2 = 50 MHz
4. This parameter is for inputs without pullups or pulldowns and $0 \le V_{IN} \le V_{CC}$.
5. This parameter is for inputs with pulldowns and V_{IH} = 2.4V.
6. This parameter is for inputs with pullups and V_{IL} = 0.45V.
7. Not 100% tested.

16.9.2 POWER SUPPLY CURRENT vs FREQUENCY

Following is the power consumption of the Low Power Intel486 microprocessor or Intel487 SX Math CoProcessor installed in a low power system for different frequencies.

Table 16.9. Power Supply Current (I_{CC}) Values over Frequencies of Operation (PGA Version)

CLK2 Frequency (MHz)	Operating Frequency (MHz)	$I_{CC(max)}$ (mA)	$I_{CC(typ)}$ (mA)
4	2	150	100
16	8	325	235
32	16	525	400
40	20	600	475
50	25	700	550

Table 16.10. Power Supply Current (I_{CC}) Values over Frequencies of Operation (PQFP Version)

CLK2 Frequency (MHz)	Operating Frequency (MHz)	I_{CC} (max) (mA)	I_{CC} (typ) (mA)
4	2	150	100
16	8	250	210
32	16	450	380
40	20	500	440
50	25	560	480

16.9.3 A.C. SPECIFICATIONS

The following tables provide the A.C. specifications for the Low Power Intel486 SX microprocessors. They consist of output delays, input setup requirements and input hold requirements. All A.C. specifications are relative to the rising edge of the phase 1 of the input system clock (CLK2), unless otherwise specified.

Table 16.11. Low Power Intel486™ SX—16 MHz Microprocessor/Intel487 SX Math CoProcessor A.C. Characteristics

V_{CC} = 5V $\pm$10%; T_{case} = 0°C to +85°C; C_L = 50 pF[2] unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	2	16	MHz		Half of CLK2 Frequency
t_1	CLK2 Period	31	250	ns	16.9	
t_2	CLK2 High Time	10		ns	16.9	At 2V
t_3	CLK2 Low Time	10		ns	16.9	At 0.8V
t_4	CLK2 Fall Time		4	ns	16.9	2V to 0.8V
t_5	CLK2 Rise Time		4	ns	16.9	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, **FERR#** *, BREQ, HLDA Valid Delay	3	26	ns	16.10	
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		42	ns	16.10	After Clock Edge[1]

**Table 16.11. Low Power Intel486™ SX—16 MHz
Microprocessor/Intel487™ SX Math CoProcessor A.C. Characteristics** (Continued)
$V_{CC} = 5V \pm 10\%$; $T_{case} = 0°C$ to $+85°C$; $C_L = 50$ pF[2] unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_8	PCHK# Valid Delay	3	35	ns	16.10	
t_{8a}	BLAST#, PLOCK# Valid Delay	3	35	ns	16.10	
t_9	BLAST#, PLOCK# Float Delay		42	ns	16.10	After Clock Edge[1]
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	3	30	ns	16.10	
t_{11}	D0–D31, DP0–3 Write Data Float Delay		42	ns	16.10	After Clock Edge[1]
t_{12}	EADS# Setup Time	12		ns	16.11	
t_{13}	EADS# Hold Time	4		ns	16.11	
t_{14}	KEN#, BS16#, BS8# Setup Time	12		ns	16.11	
t_{15}	KEN#, BS16#, BS8# Hold Time	4		ns	16.11	
t_{16}	RDY#, BRDY# Setup Time	12		ns	16.11	
t_{17}	RDY#, BRDY# Hold Time	4		ns	16.11	
t_{18}	HOLD, AHOLD, BOFF# Setup Time	12		ns	16.11	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	4		ns	16.11	
t_{20}	RESET, FLUSH#, A20M#, NMI, INTR, **IGNNE#** * Setup Time	14		ns	16.11	
t_{21}	RESET, FLUSH#, A20M#, NMI, INTR, **IGNNE#** * Hold Time	4		ns	16.11	
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	10		ns	16.11	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	4		ns	16.11	
	CLKSEL	See Figures 16.5 and 16.6 for details on this signal. Figure 16.6 shows minimum timings required for the proper operation of the CPU. The pulse on CLKSEL can be of any length as long as the minimums are satisfied and the transitions from low to high occurs at the clock edge shown.				

*Present only in the Intel487 SX Math CoProcessor

NOTES:
1. Not 100% tested, guaranteed by design characterization.
2. All timing specifications assume $C_L = 50$ pF.

Table 16.12. Low Power Intel486™ SX—20 MHz
Microprocessor/Intel487™ SX Math CoProcessor A.C. Characteristics

$V_{CC} = 5V \pm 10\%$; $T_{case} = 0°C$ to $+85°C$; $C_L = 50$ pF[2] unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	2	20	MHz		Half of CLK2 Frequency
t_1	CLK2 Period	25	250	ns	16.9	
t_2	CLK2 High Time	8.5		ns	16.9	At 2V
t_3	CLK2 Low Time	8.5		ns	16.9	At 0.8V
t_4	CLK2 Fall Time		3	ns	16.9	2V to 0.8V
t_5	CLK2 Rise Time		3	ns	16.9	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, **FERR#***, BREQ, HLDA Valid Delay	3	23	ns	16.10	
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		37	ns	16.10	After Clock Edge[1]
t_8	PCHK# Valid Delay	3	28	ns	16.10	
t_{8a}	BLAST#, PLOCK# Valid Delay	3	28	ns	16.10	
t_9	BLAST#, PLOCK# Float Delay		37	ns	16.10	After Clock Edge[1]
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	3	26	ns	16.10	
t_{11}	D0–D31, DP0–3 Write Data Float Delay		37	ns	16.10	After Clock Edge[1]
t_{12}	EADS# Setup Time	10		ns	16.11	
t_{13}	EADS# Hold Time	4		ns	16.11	
t_{14}	KEN#, BS16#, BS8# Setup Time	10		ns	16.11	
t_{15}	KEN#, BS16#, BS8# Hold Time	4		ns	16.11	
t_{16}	RDY#, BRDY# Setup Time	10		ns	16.11	
t_{17}	RDY#, BRDY# Hold Time	4		ns	16.11	
t_{18}	HOLD, AHOLD, BOFF# Setup Time	12		ns	16.11	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	4		ns	16.11	
t_{20}	RESET, FLUSH#, A20M#, NMI, INTR, **IGNNE#*** Setup Time	12		ns	16.11	
t_{21}	RESET, FLUSH#, A20M#, NMI, INTR, **IGNNE#*** Hold Time	4		ns	16.11	
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	6		ns	16.11	
t_{23}	D0–D31, DP0–3, A4–A31 Read Hold Time	4		ns	16.11	

*Present only in the Intel487 SX Math CoProcessor

NOTES:
1. Not 100% tested, guaranteed by design characterization.
2. All timing specifications assume $C_L = 50$ pF.

intel®

$V_{CC} = 5V \pm 10\%$; $T_{case} = 0°C$ to $+85°C$; $C_L = 50$ pF[2] unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Figure	Notes
	Frequency	2	25	MHz		Half of CLK2 Frequency
t_1	CLK2 Period	20	250	ns	16.9	
t_2	CLK2 High Time	7		ns	16.9	At 2V
t_3	CLK2 Low Time	7		ns	16.9	At 0.8V
t_4	CLK2 Fall Time		2	ns	16.9	2V to 0.8V
t_5	CLK2 Rise Time		2	ns	16.9	0.8V to 2V
t_6	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK#, **FERR#***, BREQ, HLDA Valid Delay	3	19	ns	16.10	
t_7	A2–A31, PWT, PCD, BE0–3#, M/IO#, D/C#, W/R#, ADS#, LOCK# Float Delay		28	ns	16.10	After Clock Edge[1]
t_8	PCHK# Valid Delay	3	24	ns	16.10	
t_{8a}	BLAST#, PLOCK# Valid Delay	3	24	ns	16.10	
t_9	BLAST#, PLOCK# Float Delay		28	ns	16.10	After Clock Edge[1]
t_{10}	D0–D31, DP0–3 Write Data Valid Delay	3	20	ns	16.10	
t_{11}	D0–D31, DP0–3 Write Data Float Delay		28	ns	16.10	After Clock Edge[1]
t_{12}	EADS# Setup Time	9		ns	16.11	
t_{13}	EADS# Hold Time	4		ns	16.11	
t_{14}	KEN#, BS16#, BS8# Setup Time	9		ns	16.11	
t_{15}	KEN#, BS16#, BS8# Hold Time	4		ns	16.11	
t_{16}	RDY#, BRDY# Setup Time	9		ns	16.11	
t_{17}	RDY#, BRDY# Hold Time	4		ns	16.11	
t_{18}	HOLD, AHOLD, BOFF# Setup Time	11		ns	16.11	
t_{19}	HOLD, AHOLD, BOFF# Hold Time	4		ns	16.11	
t_{20}	RESET, FLUSH#, A20M#, NMI, INTR, **IGNNE#*** Setup Time	11		ns	16.11	
t_{21}	RESET, FLUSH#, A20M#, NMI, INTR, **IGNNE#*** Hold Time	4		ns	16.11	
t_{22}	D0–D31, DP0–3, A4–A31 Read Setup Time	6		ns	16.11	

*Present only in the Intel487™ SX Math CoProcessor

NOTES:
1. Not 100% tested, guaranteed by design characterization.
2. All timing specifications assume $C_L = 50$ pF.

**Table 16.13. Low Power Intel486™ SX—25 MHz
Microprocessor/Intel487™ SX Math CoProcessor A.C. Characteristics** (Continued)
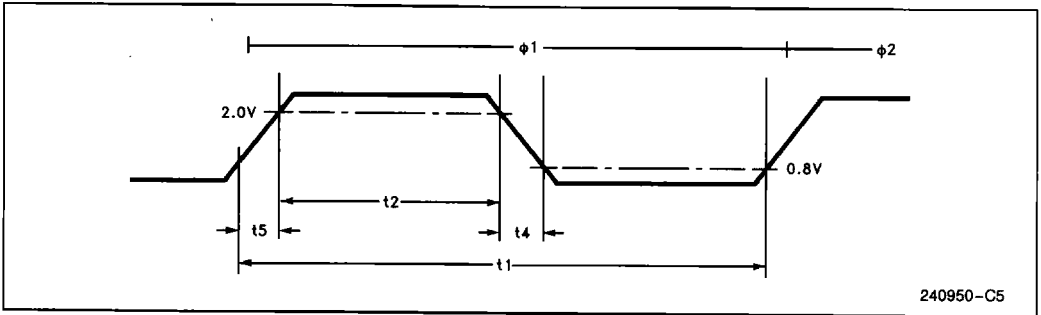$V_{CC} = 5V \pm 10\%$; $T_{case} = 0°C$ to $+85°C$; $C_L = 50$ pF[2] unless otherwise specified

Symbol	Parameter	Min	Max	Unit	Figure	Notes
t_{23}	D0−D31, DP0−3, A4−A31 Read Hold Time	4		ns	2.3	
	CLKSEL	See Figures 16.5 and 16.6 for details on this signal. Figure 16.6 shows minimum timings required for the proper operation of the CPU. The pulse on CLKSEL can be of any length as long as the minimums are satisfied and the transitions from low to high occurs at the clock edge shown.				

*Present only in the Intel487™ SX Math CoProcessor

NOTES:
1. Not 100% tested, guaranteed by design characterization.
2. All timing specifications assume $C_L = 50$ pF.

240950−C5

Figure 16.9. CLK2 Waveform

tX = t12, t14, t16, t18, t20, t22
ty = t13, t15, t17, t19, t21, t23

240950−C6
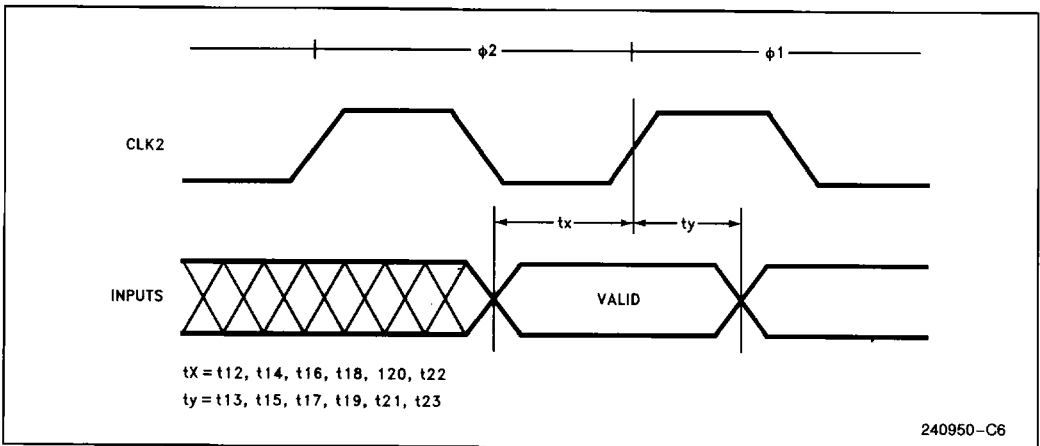
Figure 16.10. Setup and Hold Timings

intel®
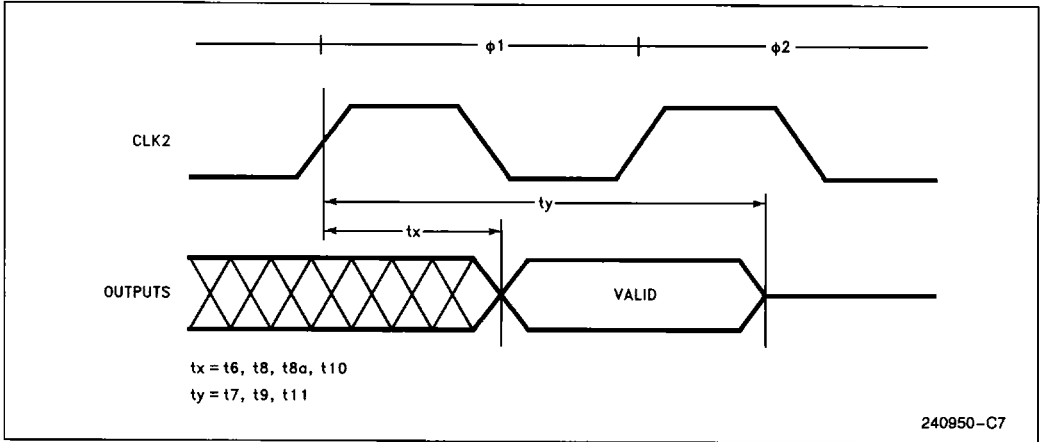

tx = t6, t8, t8a, t10
ty = t7, t9, t11

240950-C7

Figure 16.11. Valid and Float Delay Timings

16.10 Math Upgrade for Low Power Intel486™ SX Microprocessor

The Intel487 SX Math CoProcessor (MCP) is the math upgrade for the Low Power Intel486 SX microprocessor. The Intel487 SX MCP is designed and tested to operate with an external 1X clock input (standard mode) when it is installed in an Intel486 SX CPU system or with an external 2X clock input (low power mode) when it is installed in a Low Power Intel486 SX CPU based system. The Intel487 SX MCP is a super-set of the Intel486 SX CPU, containing a floating point unit, in addition to all other on-chip units present in the Intel486 SX microprocessor.

The Floating Point Unit (FPU) performs floating point operations on the 32-, 64-, and 80-bit arithmetic formats specified in IEEE Standard 754. Like the integer processing unit, the floating point unit architecture is binary-compatible with the 8087 and 80287 Math CoProcessors. The architecture is 100% compatible with the Intel287 and Intel387 Math CoProcessors.

The on-chip floating point unit of the Intel487 SX Math CoProcessor is similar to the FPU of the

Intel486 DX CPU containing eight data registers, a tag word, a control register, a status register, an instruction pointer and a data pointer. (For details on FP registers and instructions, see Section 2.1.3).

Note that the Intel487 SX Math Coprocessor is the only upgrade available for the Low Power Intel486 SX microprocessor based designs. It is fully compatible with the Low Power mode of the Intel486 SX CPU. However, the Intel OverDrive Processor does not work in systems based on the Low Power Intel486 CPU. All address, data and control signals, including the external CPU clock input (CLK2) and the CLKSEL signal of the Low Power Intel486 SX CPU, must be tied to the corresponding signals of the Intel487 SX MCP (i.e. the Intel486 SX CPU's CLK2 signal must be connected to the Intel487 SX MCP's CLK2 signal, and the Intel486 SX CPU's CLKSEL signal must be connected to the CLKSEL signal on the Intel487 SX MCP). Additionally, the performance upgrade circuit given in Section 6.6 should be followed to provide the math upgrade capability in Low Power Intel486 SX CPU systems.

The D.C./A.C. specifications given in Section 16.9 apply to the Low Power Intel486 SX CPU and the Intel487 SX MCP when it is installed in a Low Power Intel486 SX CPU system.

16.10.1 PINOUT
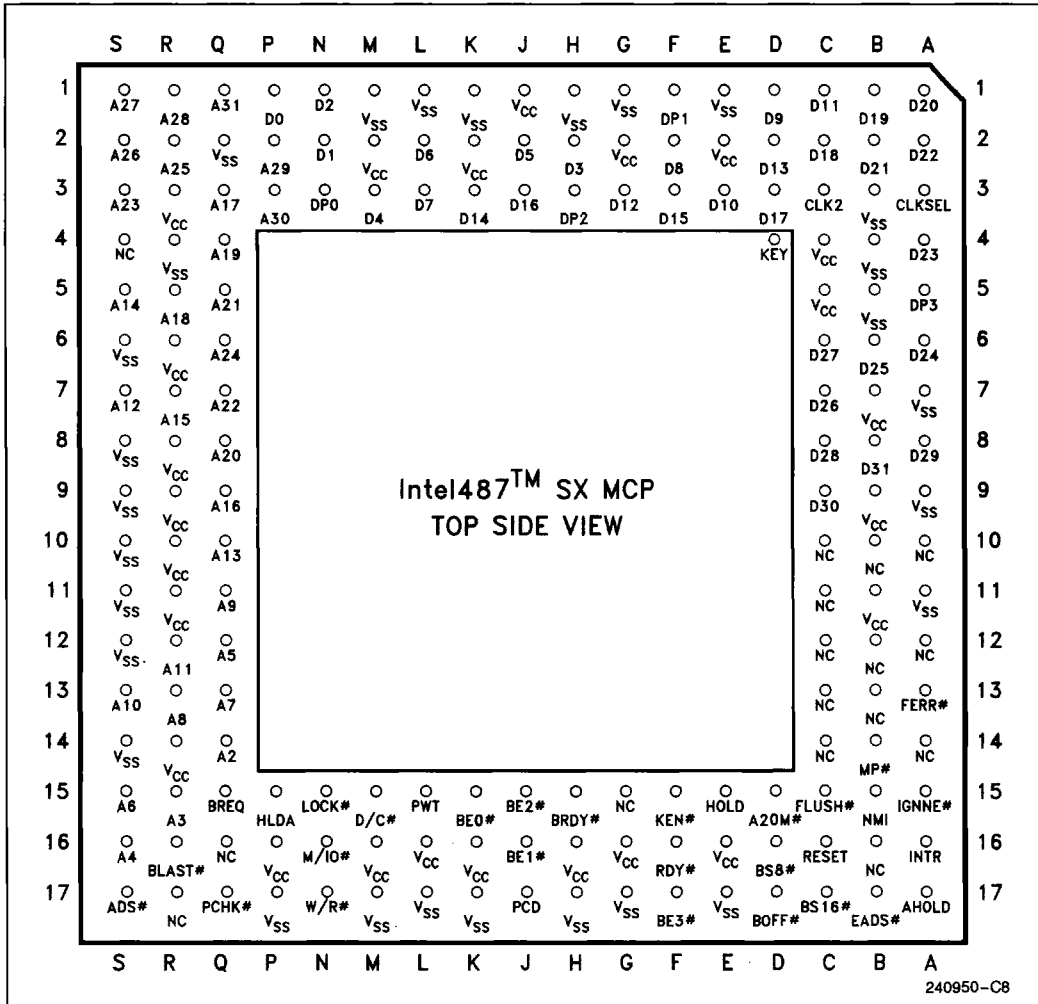
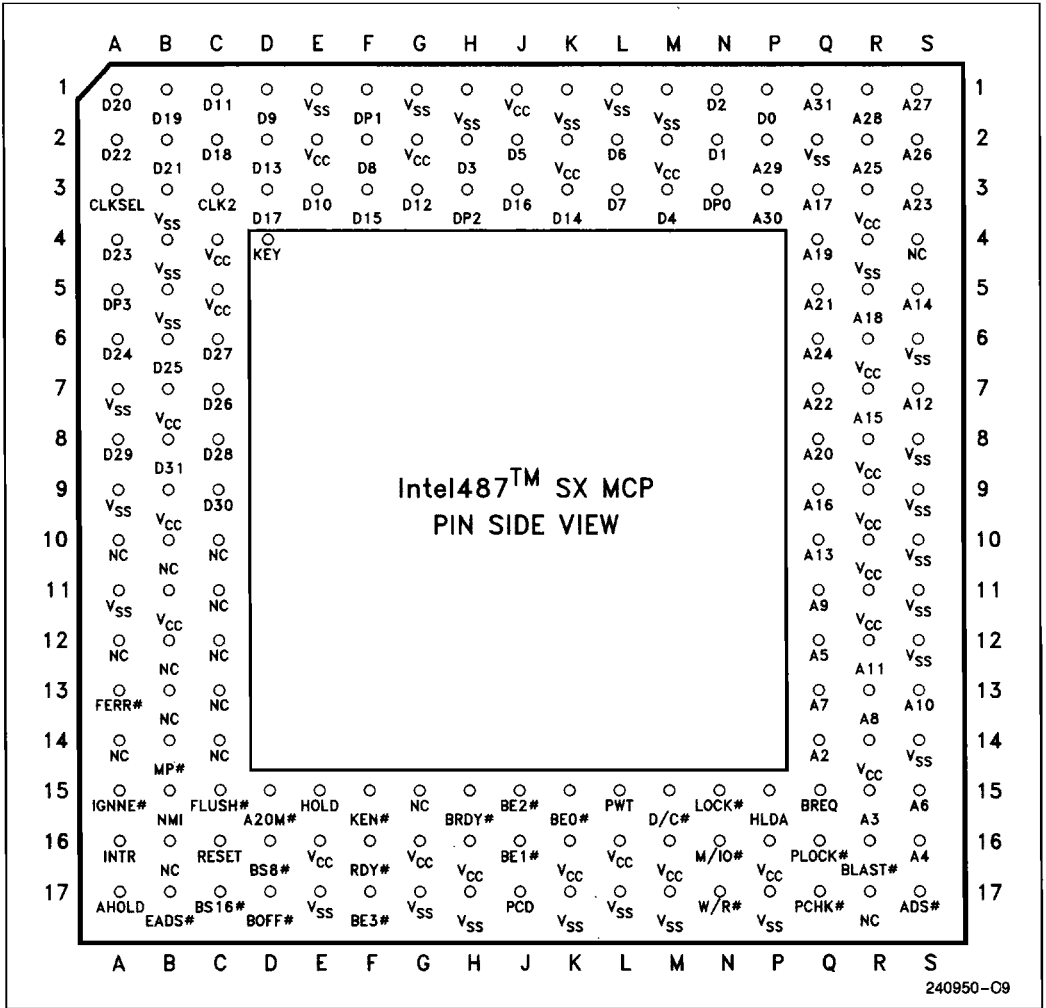Figure 16.12. Intel487™ SX MCP Pinout for Low Power Designs (Top Side View)

intel®

Figure 16.13. Intel487™ SX MCP Pinout for Low Power Designs (Pin Side View)

240950-09

16.10.2 PIN REFERENCE OF Intel487™ SX Math CoProcessor

Table 16.14. Pin Cross Reference by Pin Name

Address		Data		Control		N/C	Vcc	Vss
A_2	Q14	D_0	P1	A20M#	D15	A10	B7	A7
A_3	R15	D_1	N2	ADS#	S17	A12	B9	A9
A_4	S16	D_2	N1	AHOLD	A17	A14	B11	A11
A_5	Q12	D_3	H2	BE0#	K15	B10	C4	B3
A_6	S15	D_4	M3	BE1#	J16	B12	C5	B4
A_7	Q13	D_5	J2	BE2#	J15	B13	E2	B5
A_8	R13	D_6	L2	BE3#	F17	B16	E16	E1
A_9	Q11	D_7	L3	BLAST#	R16	C10	G2	E17
A_{10}	S13	D_8	F2	BOFF#	D17	C11	G16	G1
A_{11}	R12	D_9	D1	BRDY#	H15	C12	H16	G17
A_{12}	S7	D_{10}	E3	BREQ	Q15	C13	J1	H1
A_{13}	Q10	D_{11}	C1	BS8#	D16	C14	K2	H17
A_{14}	S5	D_{12}	G3	BS16#	C17	G15	K16	K1
A_{15}	R7	D_{13}	D2	CLK2	C3	R17	L16	K17
A_{16}	Q9	D_{14}	K3	CLKSEL	A3	S4	M2	L1
A_{17}	Q3	D_{15}	F3	D/C#	M15	D4	M16	L17
A_{18}	R5	D_{16}	J3	DP0	N3		P16	M1
A_{19}	Q4	D_{17}	D3	DP1	F1		R3	M17
A_{20}	Q8	D_{18}	C2	DP2	H3		R6	P17
A_{21}	Q5	D_{19}	B1	DP3	A5		R8	Q2
A_{22}	Q7	D_{20}	A1	EADS#	B17		R9	R4
A_{23}	S3	D_{21}	B2	FERR#	A13		R10	S6
A_{24}	Q6	D_{22}	A2	FLUSH#	C15		R11	S8
A_{25}	R2	D_{23}	A4	HLDA	P15		R14	S9
A_{26}	S2	D_{24}	A6	HOLD	E15			S10
A_{27}	S1	D_{25}	B6	IGNNE#	A15			S11
A_{28}	R1	D_{26}	C7	INTR	A16			S12
A_{29}	P2	D_{27}	C6	KEN#	F15			S14
A_{30}	P3	D_{28}	C8	LOCK#	N15			
A_{31}	Q1	D_{29}	A8	M/IO#	N16			
		D_{30}	C9	MP#	B14			
		D_{31}	B8	NMI	B15			
				PCD	J17			
				PCHK#	Q17			
				PWT	L15			
				PLOCK#	Q16			
				RDY#	F16			
				RESET	C16			
				W/R#	N17			

16.10.3 Intel487™ SX Math CoProcessor PIN DESCRIPTION

The Intel487 SX Math CoProcessor consists of all the Intel486 SX microprocessor signals with the following additional pins.

NUMERIC ERROR REPORTING		
FERR#	O	The **Floating point error** pin is driven active when a floating point error occurs. FERR# is similar to the ERROR# pin on the i387 Math CoProcessor. FERR# is included for compatibility with systems using DOS type floating point error reporting. FERR# is active LOW, and is not floated CONT1g bus hold.
IGNNE#	I	When the **ignore numeric error** pin is asserted, the Low Power Intel487 SX Math CoProcessor will ignore a numeric error and continue executing non-control floating point instructions. When IGNNE# is deasserted the Low Power Intel487 SX Math CoProcessor will freeze on a non-control floating point instruction, if a previous floating point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 is set. IGNNE# is active LOW and is provided with a small internal pullup resistor. IGNNE# is asynchronous but setup and hold times t_{20} and t_{21} must be met to insure recognition on any specific clock.
Intel487™ SX Math CoProcessor INTERFACE		
MP#	O	The **math present** pin is used to signal the Intel486 SX microprocessor to float its outputs and get-off the bus. This pin can be used to check the presence of the Math CoProcessor in the two socket math upgrade circuit. It is active low and is never floated. MP# is driven low at power-up and remains active for the entire duration of the Intel487™ SX Math CoProcessor operation.
KEY PIN		
KEY		The **KEY** pin is an electrically non-functional pin which is used to insure the correct Intel487 SX Math CoProcessor orientation in a 169-pin socket. KEY pin is located at "D4" and is the 169th pin of the Intel487 SX MCP.

17.0 SUGGESTED SOURCES FOR Intel486™ SX MICROPROCESSOR/Intel OverDrive™ PROCESSOR ACCESSORIES

Following are some suggested sources of accessories for the Intel486 SX microprocessor/Intel OverDrive Processor. They are not an endorsement of any kind, nor a warranty of the performance of any of the listed products and/or companies.

Sockets

1. McKenzie Technology
   44370 Old Palmspring Blvd.
   Fremont, CA   94538
   Tel: (415) 651-2700

2. E-CAM Technology, Inc.
   14455 North Hayden Rd.
   Suite 208
   Scottsdale, AZ   85260
   Tel: (602) 443-1949

3. Augat Inc. (for sockets with decaps)
   Interconnection Products Group
   33 Perry Ave.
   P.O. Box 779
   Attleboro, MA   02703
   Tel: (508) 222-2202

OverDrive Processor Socket for the Intel OverDrive Processor

1. Amp Incorporated
   P.O. Box 3608
   Harrisburg, PA 17105-3608
   Tel: (800) 522-6752

2. Thomas & Betts
   200 Executive Center Dr.
   P.O. Box 24901
   Greenville, SC 29616-2401
   Tel: (201) 685-1600

3. Yamaichi Electronics Inc.
   1 420 Koll Circle Suite B
   San Jose, CA 95112
   Tel: (408) 452-0797

Heat Sinks/Fins

1. Thermalloy Inc.
   2021 West Valley View Lane
   Dallas, TX   75381-0839
   Tel: (214) 243-4321

2. E G & G Division
   60 Audubon Road
   Wakefield, MA   01880
   Tel: (617) 245-5900

TTL Crystals/Oscillators

1. NEL Frequency Controls, Inc.
   357 Beloit Street
   Burlington, WI   53105
   Tel: (414) 763-3591

2. M-Tron
   P.O. Box 630
   Yankton, SD   57078
   Tel: (605) 665-9321

Debugging Tower

1. Emulation Technology
   2344 Walsh Ave., Building F
   Santa Clara, CA   95051
   Tel: (408) 982-0664

2

18.0 REVISION HISTORY

Revision -004 of the Intel486 SX Microprocessor Data Book contains many updates and improvements to the original version. A revision summary of major changes is listed below:

The sections significantly revised since version -001 are:

Cover Page	Added Intel486 SX CPU PQFP package information.
Figure 1.1a	Corrected the Intel486 SX CPU pinout. Pin D6 at location F2 has been changed to pin D8.
Figure 1.1b	Corrected the Intel487 SX MCP pinout. Pin D6 at location F2 has been changed to pin D8.
Figure 1.2a	Corrected the Intel486 SX CPU pinout. Pin D6 at location F2 has been changed to pin D8.
Figure 1.2b	Corrected the Intel487 SX MCP pinout. Pin D6 at location F2 has been changed to pin D8.
Figure 1.3	Added Intel486 SX CPU PQFP pinout.
Table 1.1c & Table 1.1d	Added Intel486 SX CPU PQFP package Pin Cross Reference table.
Quick Pin Reference	The PWT and PCD functional description has been clarified. New signals for only the Intel486 SX CPU PQFP package have been added.
Table 1.2	The MP# pin has been added to the input pin list for the Intel487 SX MCP.
Table 1.3	The UP# pin has been added to the input pin list for the Intel486 SX CPU PQFP package.
Table 1.5	Added a new pin table for the Intel486 SX CPU PQFP package test pins.
Component & Revision ID	Added note about Component ID and Revision ID numbers for the Intel486 SX CPU and Intel487 SX MCP.
Section 2.0	A description of the features of the Intel486 SX CPU in the PQFP package has been added.
Section 6.2.9	Added description of HOLD recognition during BOFF#.
Section 6.2.12	Added PCD and PWT description when paging disabled.
Section 6.2.15	Corrected explanation of A20M# sampling during reset.

Section 6.2.16	Added section on Performance Upgrade support signal description for the Intel486 SX CPU PQFP package.
Section 6.2.17	Added section on Boundary Scan Test Signals for the Intel486 SX CPU PQFP package.
Figure 6.4	Added additional details on signal sampling during RESET.
Figure 6.5.1	Added details about FERR# signal.
Figure 6.6	Corrected Intel487 SX MCP signal name on the Performance Upgrade circuit. The HOLD signal from the Intel487 SX MCP should be connected to the HOLD signal from the Intel486 SX CPU PGA package; the DATA signal from the Intel487 SX MCP should NOT be connected to the HOLD signal from the Intel486 SX CPU PGA package.
Figure 6.7	Added a Performance Upgrade circuit for the Intel486 SX CPU in the PQFP package.
Figure 7.30	Added HOLD to state transition between Tb and T1b.
Section 8.1	Corrected description of how BIST is initiated.
Section 8.2.2	Added information about moves to TR4 and TR5.
Section 8.4	Corrected description of how the Tri-State Output Test Mode is initiated.
Section 8.5	Section 8.5 describes the Boundary Scan feature of the PQFP version of the Intel486 SX CPU.
Table 13.2	16 MHz and 25 MHz D.C. specifications were added for the Intel486 SX CPU and for the PGA package.
Table 13.3	Table 12.3 is a new table which shows the 16 MHz, 20 MHz, and 25 MHz D.C. specifications for the Intel486 SX CPU for the PQFP package. The maximum and typical I_{CC} specification for the 20 MHz Intel487 SX MCP has been reduced.
Table 13.4	16 MHz and 25 MHz D.C. specifications were added for the Intel487 SX MCP.
Table 13.5	Added table with 16 MHz A.C. specifications for the Intel486 SX CPU and Intel487 SX MCP.

Table 13.6	Added improved 20 MHz A.C. specifications for T6 through T11 for the Intel486 SX CPU and Intel487 SX MCP. Minimum frequency was changed from 16 MHz to 8 MHz.
Table 13.7	Added table with 25 MHz A.C. specifications for the Intel486 SX CPU and Intel487 SX MCP.
Section 13.4.2	Added Derating curves for Intel486 SX CPU in PQFP.
Figure 14.3a & Figure 14.3b & Figure 14.3c & Table 14.2	Figures 13.3a, 13.3b, 13.3c and Table 13.2 were added to show the specifications for the 196 pin PQFP package.
Table 14.4	Table 13.4 was added to provide the θ_{JA} and θ_{JC} values for the 196 pin PQFP package.
Table 14.5 & Table 14.6	Corrected maximum T_A tables for the Intel486 SX CPU for the PGA package and the Intel487 SX MCP.
Table 14.7	Table 13.7 was added to show the maximum T_A values for the Intel486 SX CPU for the 196 pin PQFP package.
Section 15.0	Corrected address for AMP Incorporated.
Appendix B	A FINIT instruction was added to the "restore__EFLAGS" section of the Intel Recommended CPU Identification Code.

Significant revisions since -002 are listed below:

Intel OverDrive Processor information/specifications have been added throughout the document, including 33 MHz specifications for the OverDrive Processor. Section 8.0 contains OverDrive Processor specific information.

A new section was added containing a summary of differences between the Intel486 SX Microprocessor in PGA and PQFP packages.

Intel OverDrive Processor information/specifications have been added throughout the document. Section 13.0 contains OverDrive Processor specific information.

33 MHz Intel486 SX Microprocessor specifications have been added throughout the document.

Low Power Intel486 DX CPU information/specifications have been added. Section 16.0 contains Low Power specific information.

Cover Page	Listed boundary scan compatibility feature for PQFP package.

Pinout	Noted the pinout and pin description for the Intel487 SX MCP are identical to the Intel OverDrive Processor except for the MP# pin is redefined as the UP# pin on the Intel OverDrive Processor.
Pin Description	More clearly defined A20M# pin.
Table 1.1d	Corrected Bus Request instruction from BREQ# to BREQ.
Table 1.6	Added B0 stepping information for Intel486 SX microprocessor along with OverDrive Processor stepping information.
Table 6.3	Added stepping info for Intel487 SX MCP and OverDrive Processor.
Section 8.1	Added number of clocks required for BIST at 25 MHz.
Section 8.5.5	Removed FERR# as a control pin for MISCCTL.
Chapter 12	New chapter on the differences with the Intel486 SX Microprocessor in PGA vs PQFP.
Chapter 13	New chapter on OverDrive Processor.
Section 14.3	Added D.C. specs for Intel 33 MHz 486 SX microprocessor.
Table 13.5	Changed Hold times for Intel 16 MHz 486 SX microprocessor 4 ns to 3 ns.
Section 13.4	Added A.C. specs for Intel486™ SX 33 MHz for PGA and PQFP packages.
Section 13.4	Added Boundary Scan Test signals and timing diagrams.
Chapter 16	New section for Low Power Intel486 SX microprocessor.

The sections significantly revised since version -003 are:

Section 6.5	Added clarification for the built in self test (BIST) during reset.
Section 7.2.9	Added explanation of bus hold and hold acknowledge protocol.
Figure 7.26b	Added figure to illustrate HOLD request acknowledge during BOFF#.
Table 14.2	Changed PGA I_{CC} Max specifications for 16 MHz and 33 MHz.
Table 14.3	Changed PQFP I_{CC} Max specifications for all frequencies.
Table 14.8	Changed Max specification of t_9 BLAST#, PLOCK# Float Delay.

2

Table 14.9   Changed Min and Max specifica-
                    tions for Boundary Scan Test In-
                    puts.

Table 15.4   Changed maximum ambient tem-
                    perature specifications for 16 MHz
                    and 33 MHz CPUs in PGA pack-
                    age.

Table 15.7 and   Changed maximum ambient tem-
Table 15.8   perature specifications for all fre-
                    quencies of CPUs in PQFP pack-
                    age.
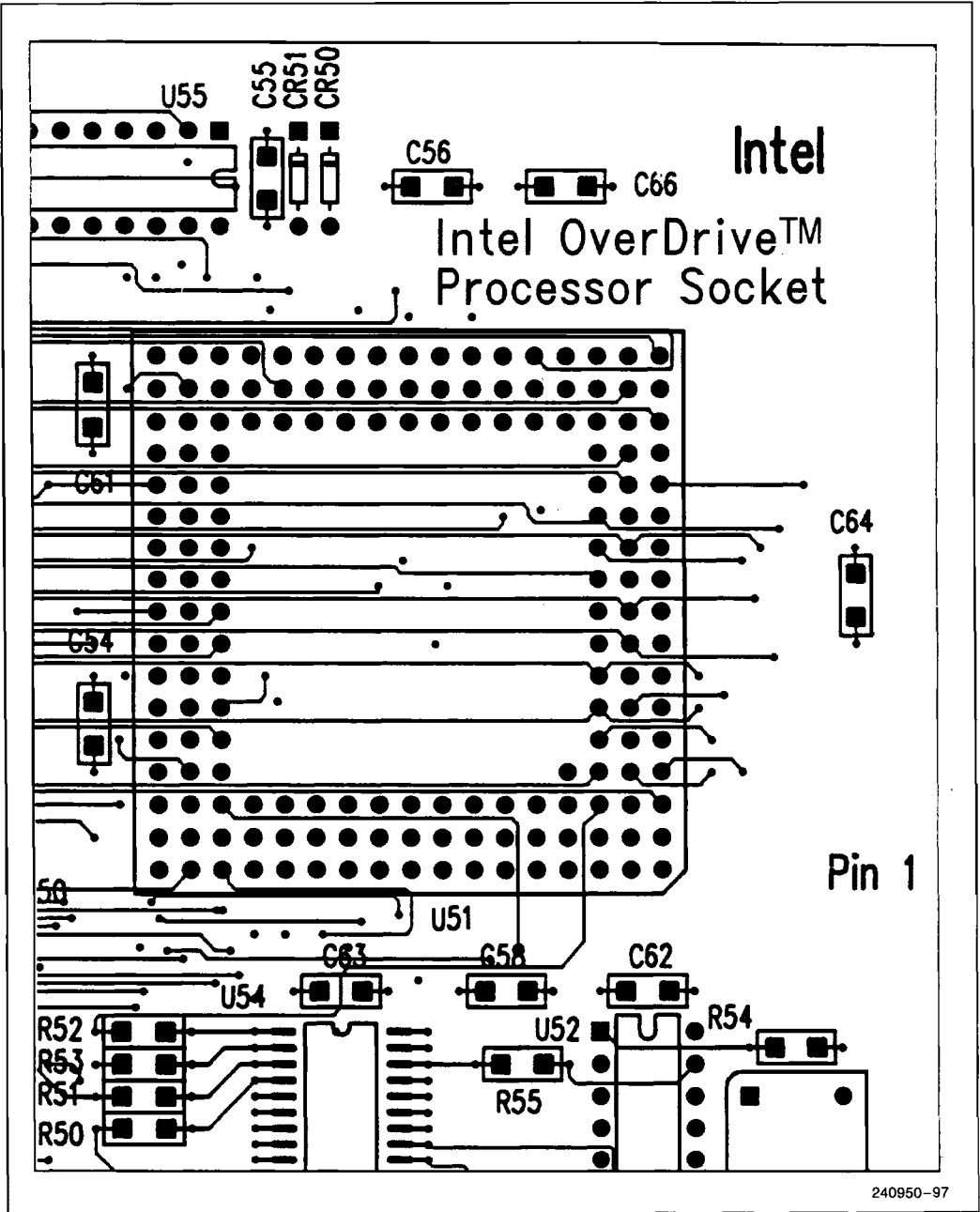
intel®

APPENDIX A
OverDrive™ PROCESSOR
INSTALLATION MADE EASY

OEM PC manufacturers can make OverDrive Processor installation easier for the end user and reseller. Simple and foolproof OverDrive Processor installation results in fewer broken PC boards and less end user and reseller frustration. The following is a brief list of ways to make OverDrive Processor installation simple and foolproof for the end user and reseller:

1. Intel has packaged the Intel487 SX Math CoProcessor in a 169 pin PGA package. The 169th pin insures that the Intel487 SX Math CoProcessor fits into a 169 pin socket in only the correct orientation. Supplying a 169 pin socket as the OverDrive Processor eliminates the possibility of damaging the PC board due to end users and resellers powering up the system with the OverDrive Processor in an incorrect orientation[1].

2. Because of the high pin count of the Intel487 SX Math CoProcessor package, the insertion force required for a standard PGA socket is excessive. Even most Low Insertion Force sockets require approximately 30 lbs. (13.5 kg) of insertion force. A Zero Insertion Force socket insures that the OverDrive Processor installation insertion force does not damage the PC board. Be sure to allow enough clearance for the socket handle when a Zero Insertion Force socket is used.

3. Make the OverDrive Processor socket easily accessible to the end user. (i.e., Do not place the OverDrive Processor socket under a disk drive.)

4. Label the Intel487 SX Math CoProcessor socket and the location of pin 1 by silk screening this information on the PC board. See Figure A.

5. Describe the Intel487 SX Math CoProcessor installation procedure in the PC's User's Manual.

NOTE:
1. Many socket manufacturers use a standard grid array for PGA sockets. The socket cover contains more than the required number of pin holes, but contacts are only loaded where required for electrical connection. For the 169th pin to assist the end user and reseller in installing the chip with the correct orientation, it is essential that the socket have only 169 pin holes in the cover. The only sure way to ascertain that a socket has only 169 pin holes is to order samples and do a visual check.

intel®

Figure A. Example of PC Board with "Intel OverDrive™ Processor Socket"
and "Pin 1" Silk Screened onto PC Board

240950-97

APPENDIX B
INTEL RECOMMENDED CPU IDENTIFICATION CODE

The CPU identification assembly code will determine for the user which Intel microprocessor and if a Intel Math CoProcessor is installed in the system. If a 486 microprocessor has been installed, the program will determine if the CPU is with/without a floating point unit. This code should be executed so the system can be configured for a particular application, which may depend on the microprocessor and Math CoProcessor installed in the system.

```
            TITLE  CPUID
            DOSSEG
            .model  small

            .stack  100h

            .data
fp_status           dw       ?
id_mess             db       "This system has a$"
fp_8087             db       "and an 8087 Math CoProcessor$"
fp_80287            db       "and an 287 Math CoProcessor$"
fp_80387            db       "and an 387 Math CoProcessor$"
c8086               db       "n8086/8088 microprocessor$"
c286                db       "n80286 microprocessor$"
c386                db       "386 microprocessor$"
c486                db       "486 DX microprocesser/487 SX Math
                             "CoProcessor$"
c486nfp             db       "486 SX Microprocessor$"
period              db       ".$",13,10
present_86           dw       0
present_286          dw       0
present_386          dw       0
present_486          dw       0
;
;           The purpose of this code is to allow the user the ability to identify
;           the processor and coprocesor that is currently in the system. The
;           algorithm of the program is to first determine the processor id.
;           When that is accomplished, the program continues to then identify
;           whether a coprocessor exists in the system. If a coprocessor or
;           integrated coprocessor exists, the program will identify the
;           coprocessor id. If one does not exist, the program then terminates.
;

            .code
start:
            mov      ax,@data
            mov      ds,ax                  ; set segment register

            mov      dx,offset id_mess      ;print header message
            mov      ah,9h
            int      21h
```

```
;
;           8086 check
;           Bits 12-15 are always set on the 8086 processor.
;
                pushf                       ; save EFLAGS
                pop     bx                  ; store EFLAGS in BX
          .     mov     ax,0fffh            ; clear bits 12-15
                and     ax,bx               ;        in EFLAGS
                push    ax                  ; store new EFLAGS value on stack
                popf                        ; replace current EFLAGS value
                pushf                       ; set new EFLAGS
                pop     ax                  ; store new EFLAGS in AX
                and     ax,0f000h           ; if bits 12-15 are set, then CPU
                cmp     ax,0f000h           ;        is an 8086/8088
                mov     dx,offset c8086     ; store 8086/8088 message
                mov     present_86,1        ; turn on 8086/8088 flag
                je      check_fpu           ; if CPU is 8086/8088, check for
                                            ; 8087


;
;           80286 CPU Check
;           Bits 12-15 are always clear on the 80286 processor.
;
                or      bx,0f000h           ; try to set bits 12-15
                push    bx
                popf
                pushf
                pop     ax
                and     ax,0f000h           ; if bits 12-15 are cleared, then
                mov     dx,offset c286      ;        CPU is an 80286
                mov     present_86,0        ; turn off 8086/8088 flag
                mov     present_286,1       ; turn on 80286 flag
                jz      check_fpu           ; if CPU is 80286, check for 80287


;
;           386 CPU check
;           The AC bit, bit #18, is a new bit introduced in the EFLAGS register
;           on the 486 DX CPU to generate alignment faults. This bit can be set
;           on the 486 DX CPU, but not on the 386 CPU.
;
                mov     bx,sp               ; save current stack pointer to
                                            ; align it
                and     sp,not 3            ; align stack to avoid AC fault
                db      66h
                pushf                       ; push original EFLAGS
                db      66h
                pop     ax                  ; get original EFLAGS
                db      66h
                mov     cx,ax               ; save original EFLAGS
                db      66h                 ; xor EAX,40000h
                xor     ax,0                ; flip AC bit in EFLAGS
                dw      4                   ; upper 16-bits of xor constant
                db      66h
                push    ax                  ; save for EFLAGS
                db      66h
                popf                        ; copy to EFLAGS
```

```
            db      66h
            pushf                       ; push EFLAGS
            db      66h
            pop     ax                  ; get new EFLAGS value
            db      66h
            xor     ax,cx               ; if AC bit cannot be changed,
                                        ; CPU is
            mov     dx,offset c386      ; store 386 message
            mov     present_286,0       ; turn off 80286 flag
            mov     present_386,1       ; turn on 386 flag
            je      check_fpu           ; if CPU is 386, now check for
                                        ;   80287/80387


;
;           486 DX CPU and 486 DX CPU w/o FPU checking
;
            mov     dx,offset c486nfp   ; store 486NFP message
            mov     present_386,0       ; turn off 386 flag
            mov     present_486,1       ; turn on 486 flag


;
;           Co-processor checking begins here for the 8086/80286/386 CPUs.
;           The algorithm is to determine whether or not the floating-point
;           status and control words can be written to, the correct coprocessor
;           is then determined depending on the processer id. Coprocessor checks
;           are first performed for an 8086, 80286 and a 486 DX CPU. If the
;           coprocessor id is still undetermined, the system must contain a 386
;           CPU. The 386 CPU may work with either an 80287 or an 80387. The
;           infinity of the coprocessor must be checked to determine the correct
;           coprocessor id.
;

check_fpu:                              ; check for 8087/80287/80387
            fninit                      ; reset FP status word
            mov     fp_status,5a5ah     ; initialize temp word to non-zero
                                        ; value
            fnstsw  fp_status           ; save FP status word
            mov     ax,fp_status        ; check FP status word
            cmp     al,0                ; see if correct status with
                                        ; written
            jne     print_one           ; jump if not Valid, no NPX
                                        ; installed

            fnstcw  fp_status           ; save FP control word
            mov     ax,fp_status        ; check FP control word
            and     ax,103fh            ; see if selected parts looks OK
            cmp     ax,3fh              ; check that ones and zeroes
                                        ; correctly read
            jne     print_one           ; jump if not Valid, no NPX
                                        ; installed

            cmp     present_486,1       ; check if 486 flag is on
            je      is_486              ; if so, jump to print 486 message
            jmp     not_486             ; else continue with 386 checking

is_486:
            mov     dx,offset c486      ; store 486 message
            jmp     print_one
```

2

```
not_486:
                cmp     present_386,1         ; check if 386 flag is on
                jne     print_87_287          ; if 386 flag not on, check NPX for
                                              ;   8086/8088/80286
                mov     ah,9h                 ; print out 386 CPU ID first
                int     21h
;
;        80287/80387 check for the 386 CPU
;
                fld1                          ; must use default control from
                                              ; FNINIT
                fldz                          ; form infinity
                fdiv                          ; 8087/80287 says +inf = inf
                fld     st                    ; form negative infinity
                fchs                          ; 80387 says +inf < > -inf
                fcompp                        ; see if they are the same and
                                              ; remove them
                fstsw   fp_status             ; look at status from FCOMPP
                mov     ax,fp_status
                mov     dx,offset fp_80287    ; store 80287 message
                sahf                          ; see if infinities matched
                jz      restore_EFLAGS        ; jump if 8087/80287 is present
                mov     dx,offset fp_80387    ; store 80387 message

restore_EFLAGS:
                finit                         ; clear any pending fp exception
                mov     ah,9h                 ; print NPX message
                int     21h
                db      66h
                push    cx                    ; push ECX
                db      66h
                popf                          ; restore original EFLAGS register
                mov     sp,bx                 ; restore original stack pointer
                jmp     exit

print_one:
                mov     ah,9h                 ; print out CPU ID with no NPX
                int     21h
                jmp     exit

print_87_287:
                mov     ah,9h                 ; print out 8086/8088/80286 first
                int     21h
                cmp     present_86,1          ; if 8086/8088 flag is on
                mov     dx,offset fp_8087     ; store 8087 message
                je      print_fpu
                mov     dx,offset fp_80287    ; else CPU = 80286, store 80287
                                              ; message

print_fpu:
                mov     ah,9h                 ; print out NPX
                int     21h
                jmp     exit

exit:
                mov     dx,offset period      ; print out a period of end message
                mov     ah,9h
                int     21h

                mov     ax,4c00h              ; terminate program
                int     21h

                end     start
```