

131,072-WORD BY 8-BIT STATIC RAM

DESCRIPTION

The TC551001BPI/BFI/BFTI/BTRI/BSOI/BSRI is a 1,048,576-bit static random access memory (SRAM) organized as 131,072 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single $5\text{ V} \pm 10\%$ power supply. Advanced circuit technology provides both high speed and low power at an operating current of 5 mA/MHz (typ) and a minimum cycle time of 85 ns . It is automatically placed in low-power mode at $2\text{ }\mu\text{A}$ standby current (typ) when chip enable (CE1) is asserted high or (CE2) is asserted low. There are three control inputs. CE1 and CE2 are used to select the device and for data retention control, and output enable (OE) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of -40° to 85°C , the TC551001BPI/BFI/BFTI/BTRI/BSOI/BSRI can be used in environments exhibiting extreme temperature conditions. The TC551001BPI/BFI/BFTI/BTRI/BSOI/BSRI is available in a standard plastic 32-pin dual-in-line package (DIP), plastic 32-pin small-outline package (SOP) and normal and reverse pinout plastic 32-pin thin-small-outline package (TSOP).

FEATURES

- Low-power dissipation
 - Operating: 27.5 mW/MHz (typical)
- Standby current of $200\text{ }\mu\text{A}$ (maximum)
- Single power supply voltage of $5\text{ V} \pm 10\%$
- Power down features using CE1 and CE2.
- Data retention supply voltage of 2 to 5.5 V
- Direct TTL compatibility for all inputs and outputs
- Wide operating temperature range of -40° to 85°C

• Access Times (maximum):

	TC551001BPI/BFI/BFTI/BTRI/BSOI/BSRI	
	-85	-10
Access Time	85 ns	100 ns
CE1 Access Time	85 ns	100 ns
CE2 Access Time	85 ns	100 ns
OE Access Time	45 ns	50 ns

• Packages:

DIP32-P-600-2.54 (BPI)	(Weight: 4.45 g typ)
SOP32-P-525-1.27 (BFI)	(Weight: 1.04 g typ)
TSOP I 32-P-0820-0.50 (BFTI)	(Weight: 0.34 g typ)
TSOP I 32-P-0820-0.50A (BTRI)	(Weight: 0.34 g typ)
TSOP I 32-P-0.50 (BSOI)	(Weight: 0.24 g typ)
TSOP I 32-P-0.50A (BSRI)	(Weight: 0.24 g typ)

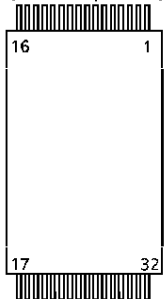
PIN ASSIGNMENT (TOP VIEW)

○ 32 PIN DIP & SOP

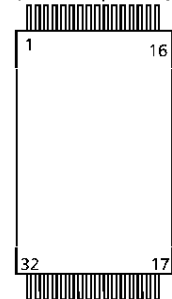
NC	1	32	V _{DD}
A ₁₆	2	31	A ₁₅
A ₁₄	3	30	CE2
A ₁₂	4	29	R/W
A ₇	5	28	A ₁₃
A ₆	6	27	A ₈
A ₅	7	26	A ₉
A ₄	8	25	A ₁₁
A ₃	9	24	OE
A ₂	10	23	A ₁₀
A ₁	11	22	CE1
A ₀	12	21	I/O ₈
I/O ₁	13	20	I/O ₇
I/O ₂	14	19	I/O ₆
I/O ₃	15	18	I/O ₅
GND	16	17	I/O ₄

○ 32 PIN TSOP

(Normal pinout)



(Reverse pinout)



PIN NAMES

A ₀ to A ₁₆	Address Inputs
R/W	Read/Write Control
OE	Output Enable
CE1, CE2	Chip Enable
I/O ₁ to I/O ₈	Data Input/Output
V _{DD}	Power (+ 5V)
GND	Ground
NC	No Connection

Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A ₁₁	A ₉	A ₈	A ₁₃	R/W	CE2	A ₁₅	V _{DD}	NC	A ₁₆	A ₁₄	A ₁₂	A ₇	A ₆	A ₅	A ₄
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A ₃	A ₂	A ₁	A ₀	I/O ₁	I/O ₂	I/O ₃	GND	I/O ₄	I/O ₅	I/O ₆	I/O ₇	I/O ₈	CE1	A ₁₀	OE

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The diagram illustrates the internal architecture of a 1024 x 128 x 8 (1048576) memory array. Key components include:

- Row Address Buffer:** Receives address bits A7 through A16.
- Row Address Register:** Receives a clock signal (CE) and outputs to the Row Address Decoder.
- Row Address Decoder:** Decodes the row address and outputs to the Memory Cell Array.
- Memory Cell Array:** The core storage element, labeled 1024 x 128 x 8 (1048576).
- Sense Amp:** Receives data from the Memory Cell Array and outputs to the Column Address Decoder.
- Column Address Decoder:** Decodes the column address and outputs to the Column Address Register.
- Column Address Register:** Receives a clock signal (CE) and outputs to the Column Address Buffer.
- Column Address Buffer:** Outputs address bits A0 through A6 to the Memory Cell Array.
- Data Control:** Receives data from I/O1 through I/O8 and outputs to the Memory Cell Array.
- Clock Generator:** Receives a clock signal (CE) and outputs to the Row Address Register and Column Address Register.
- Control Signals:** OE (Output Enable), R/W (Read/Write), CE1 (Chip Enable 1), and CE2 (Chip Enable 2) are shown at the bottom.
- Power and Ground:** VDD and GND connections are indicated at the top right.

MODE	$\overline{\text{CE1}}$	CE2	$\overline{\text{OE}}$	R/W	I/O1 to I/O8	POWER
Read	L	H	L	H	D _{OUT}	I _{DDO}
Write	L	H	*	L	D _{IN}	I _{DDO}
Outputs Disabled	L	H	H	H	High-Z	I _{DDO}
Standby	H	X	X	X	High-Z	I _{DD5}
	X	L	X	X	High-Z	I _{DD5}

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	– 0.3 to 7.0	V
V _{IN}	Input Voltage	– 0.3* to 7.0	V
V _{I/O}	Input and Output Voltage	– 0.5 to V _{DD} + 0.5	V
P _D	Power Dissipation	1.0/0.6**	W
T _{solder}	Soldering Temperature (10 s)	260	°C
T _{strg.}	Storage Temperature	– 55 to 150	°C
T _{opr.}	Operating Temperature	– 40 to 85	°C

** SOP

DC RECOMMENDED OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	–	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3^*	–	0.6	
V_{DH}	Data Retention Supply Voltage	2.0	–	5.5	

* -3.0 V when measured at a pulse width of 50 nsDC CHARACTERISTICS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 5\text{ V} \pm 10\%$)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT	
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DD}		–	–	± 1.0	μA	
I _{OH}	Output High Current	V _{OH} = 2.4 V		– 1.0	–	–	mA	
I _{OL}	Output Low Current	V _{OL} = 0.4 V		4.0	–	–	mA	
I _{LO}	Output Leakage Current	CE1 = V _{IH} or CE2 = V _{IL} or R/W = V _{IL} or OE = V _{IH} , V _{OUT} = 0 V to V _{DD}		–	–	± 1.0	μA	
I _{DDO1}	Operating Current	CE1 = V _{IL} and CE2 = V _{IH} and R/W = V _{IH} , I _{OUT} = 0 mA Other Inputs = V _{IH} /V _{IL}	Tcycle	min	–	–	70	mA
				1 μs	–	–	20	
I _{DDO2}		CE1 = 0.2 V and CE2 = V _{DD} – 0.2 V R/W = V _{DD} – 0.2 V, I _{OUT} = 0 mA Other Inputs = V _{DD} – 0.2 V/0.2 V	Tcycle	min			60	mA
					1 μs	–	–	
I _{DDs1}	Standby Current	CE1 = V _{IH} or CE2 = V _{IL}		–	–	3	mA	
I _{DDs2} (Note)		CE1 = V _{DD} – 0.2 V or CE2 = 0.2 V V _{DD} = 2.0 to 5.5 V, Ta = – 40° to 85°C		–	2	200	μA	

Note: In standby mode with $\overline{CE1} \geq V_{DD} - 0.2\text{ V}$, these limits are assured for the condition $CE2 \geq V_{DD} - 0.2\text{ V}$ or $CE2 \leq 0.2\text{ V}$.CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C_{IN}	Input Capacitance	$V_{IN} = \text{GND}$	10	pF
C_{OUT}	Output Capacitance	$V_{OUT} = \text{GND}$	10	

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS ($T_a = -40^\circ$ to 85°C , $V_{DD} = 5\text{ V} \pm 10\%$)

READ CYCLE

SYMBOL	PARAMETER	TC551001BPI/BFI/BFTI/BTRI/BSTI/BSRI				UNIT
		-85		-10		
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	85	–	100	–	ns
t _{ACC}	Address Access Time	–	85	–	100	
t _{CO1}	Chip Enable ($\overline{CE1}$) Access Time	–	85	–	100	
t _{CO2}	Chip Enable (CE2) Access Time	–	85	–	100	
t _{OE}	Output Enable Access Time	–	45	–	50	
t _{COE}	Chip Enable Low to Output Active	5	–	5	–	
t _{OEE}	Output Enable Low to Output Active	0	–	0	–	
t _{OD}	Chip Enable High to Output High-Z	–	35	–	40	
t _{ODO}	Output Enable High to Output High-Z	–	35	–	40	
t _{OH}	Output Data Hold Time	10	–	10	–	

WRITE CYCLE

SYMBOL	PARAMETER	TC551001BPI/BFI/BFTI/BTRI/BSTI/BSRI				UNIT
		-85		-10		
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	85	–	100	–	ns
t _{WP}	Write Pulse Width	60	–	60	–	
t _{CW}	Chip Enable to End of Write	75	–	80	–	
t _{AS}	Address Setup Time	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	
t _{ODW}	R/W Low t _{Low} to Output High-Z	–	35	–	40	
t _{OEW}	R/W High to Output Active	0	–	0	–	
t _{DS}	Data Setup Time	35	–	40	–	
t _{DH}	Data Hold Time	0	–	0	–	

AC TEST CONDITIONS

Output load: 100 pF + one TTL gate

Input pulse level: 0.4 V, 2.6 V

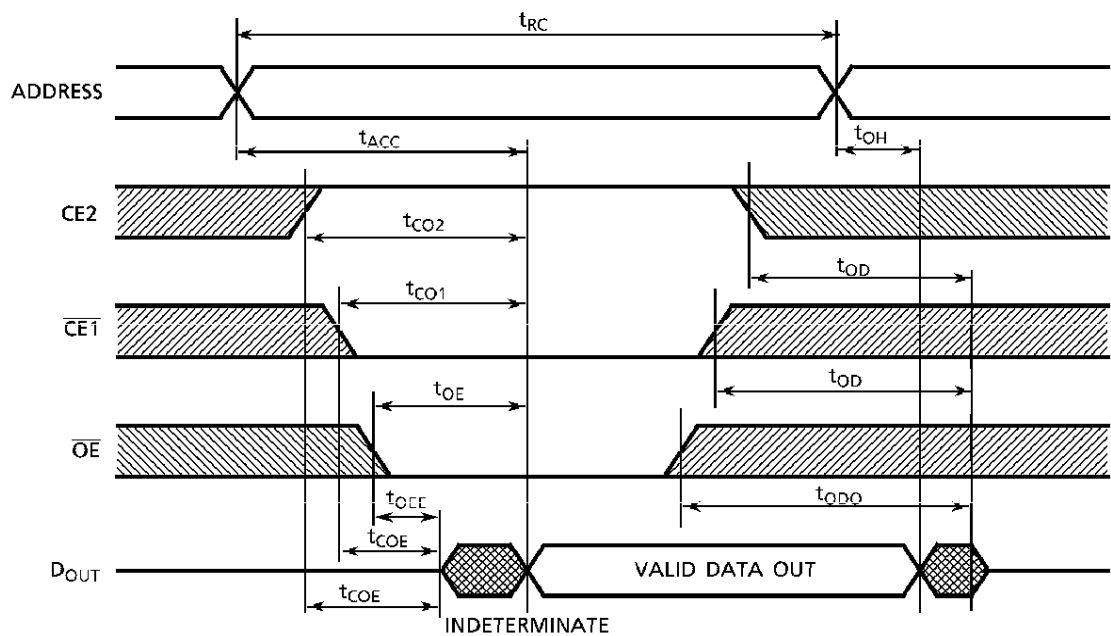
Timing measurements: 1.5 V

Reference level: 1.5 V

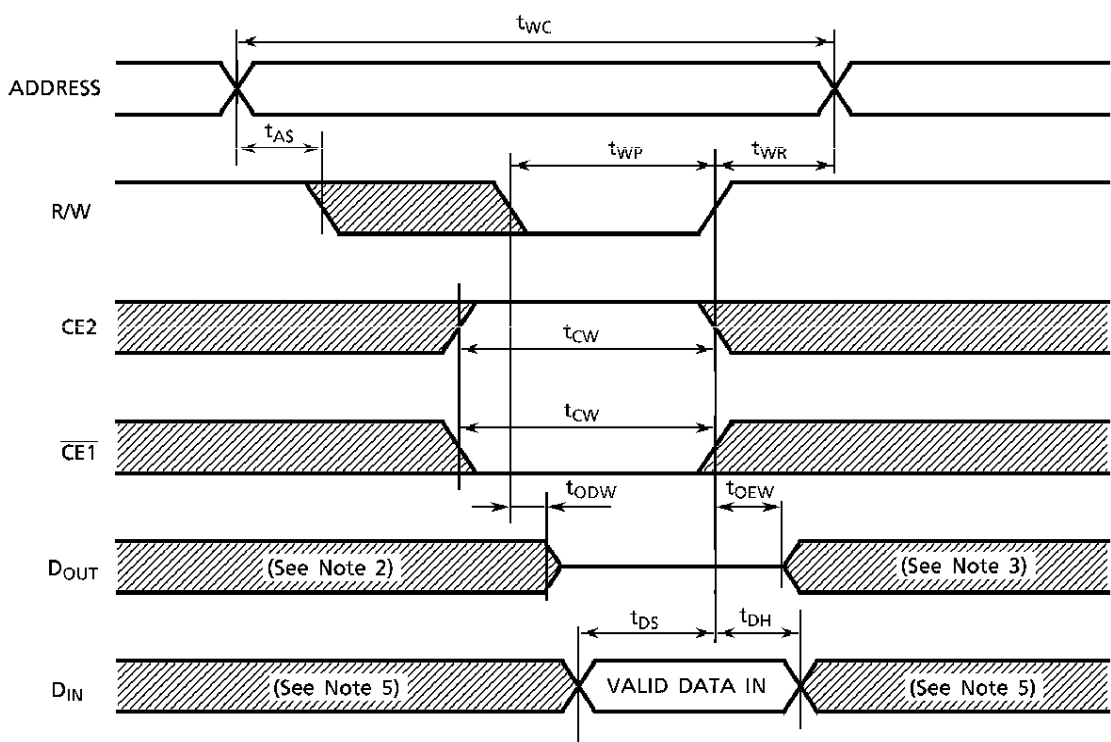
t_R , t_F : 5 ns

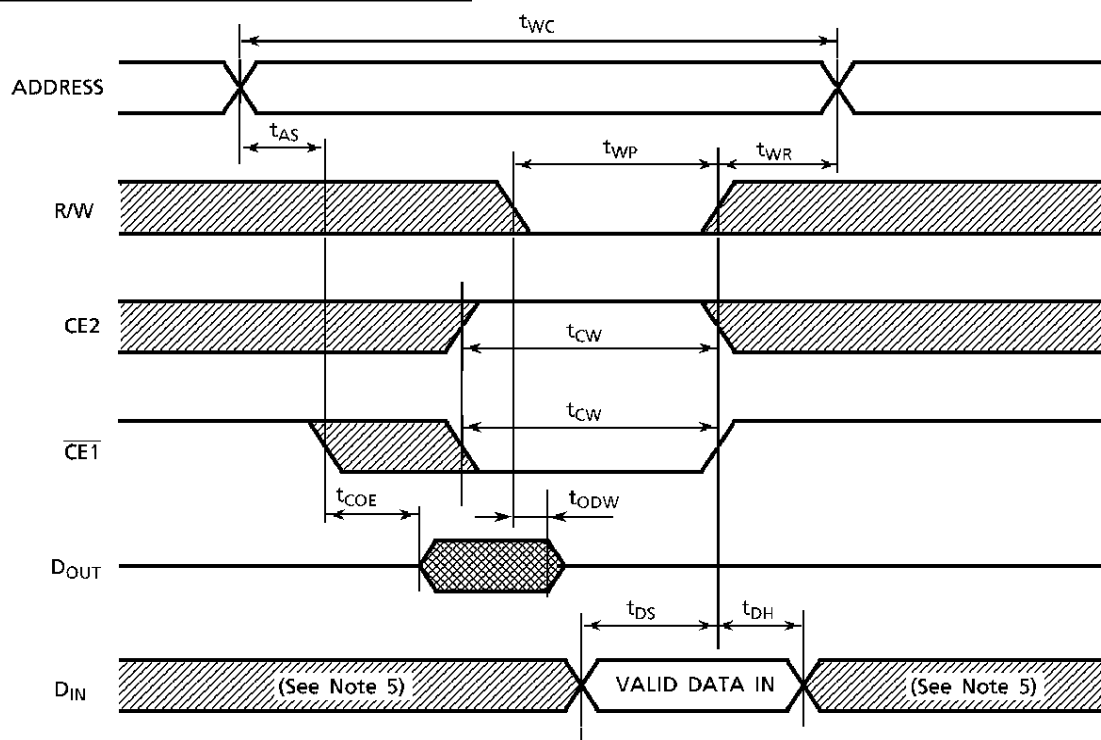
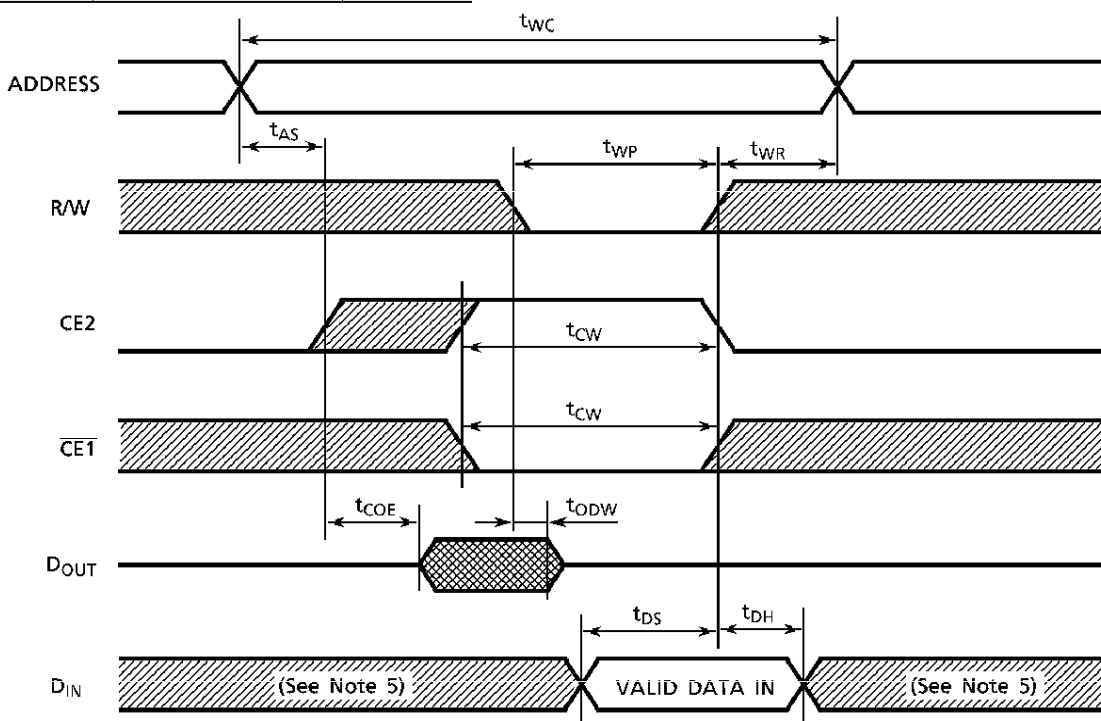
TIMING DIAGRAMS

READ CYCLE (See Note 1)



WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



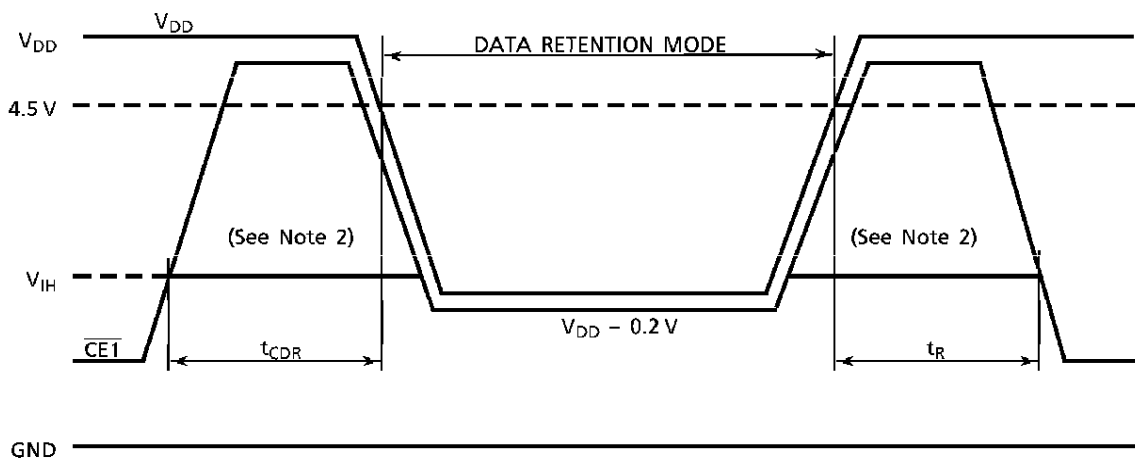
WRITE CYCLE 2 ($\overline{\text{CE1}}$ CONTROLLED) (See Note 4)WRITE CYCLE 3 (CE2 CONTROLLED) (See Note 4)

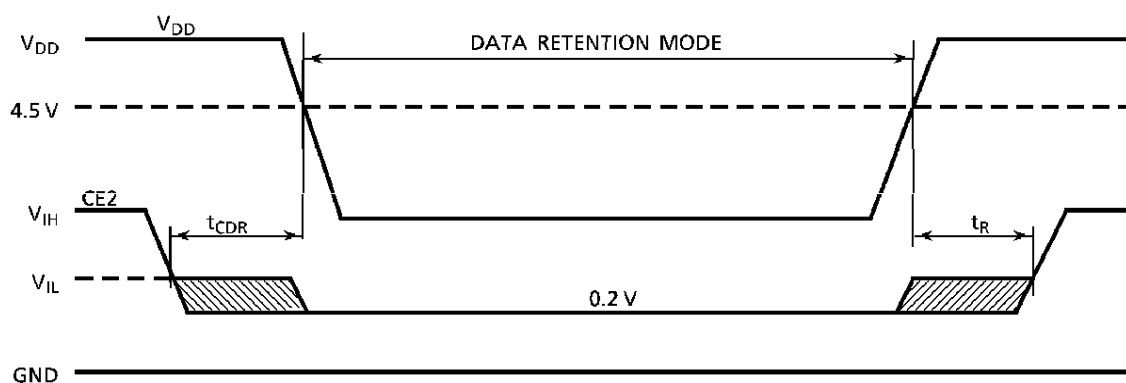
- Note:
- (1) R/W remains HIGH for the read cycle.
 - (2) If $\overline{\text{CE1}}$ goes LOW (or CE2 goes HIGH) coincident with or after R/W goes LOW, the outputs will remain at high impedance.
 - (3) If $\overline{\text{CE1}}$ goes HIGH (or CE2 goes LOW) coincident with or before R/W goes HIGH, the outputs will remain at high impedance.
 - (4) If $\overline{\text{OE}}$ is HIGH during the write cycle, the outputs will remain at high impedance.
 - (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = - 40° to 85°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V _{DH}	Data Retention Supply Voltage		2.0	—	5.5	V
I _{DD\$2}	Standby Current	V _{DH} = 3.0 V	—	—	100	μA
		V _{DH} = 5.5 V	—	—	200	
t _{CDR}	Chip Deselect to Data Retention Mode Time		0	—	—	nS
t _R	Recovery Time		5	—	—	mS

$\overline{\text{CE1}}$ CONTROLLED DATA RETENTION MODE (See Note 1)



CE2 CONTROLLED DATA RETENTION MODE (See Note 3)

Note: (1) In $\overline{CE1}$ controlled data retention mode, minimum standby current mode is entered when

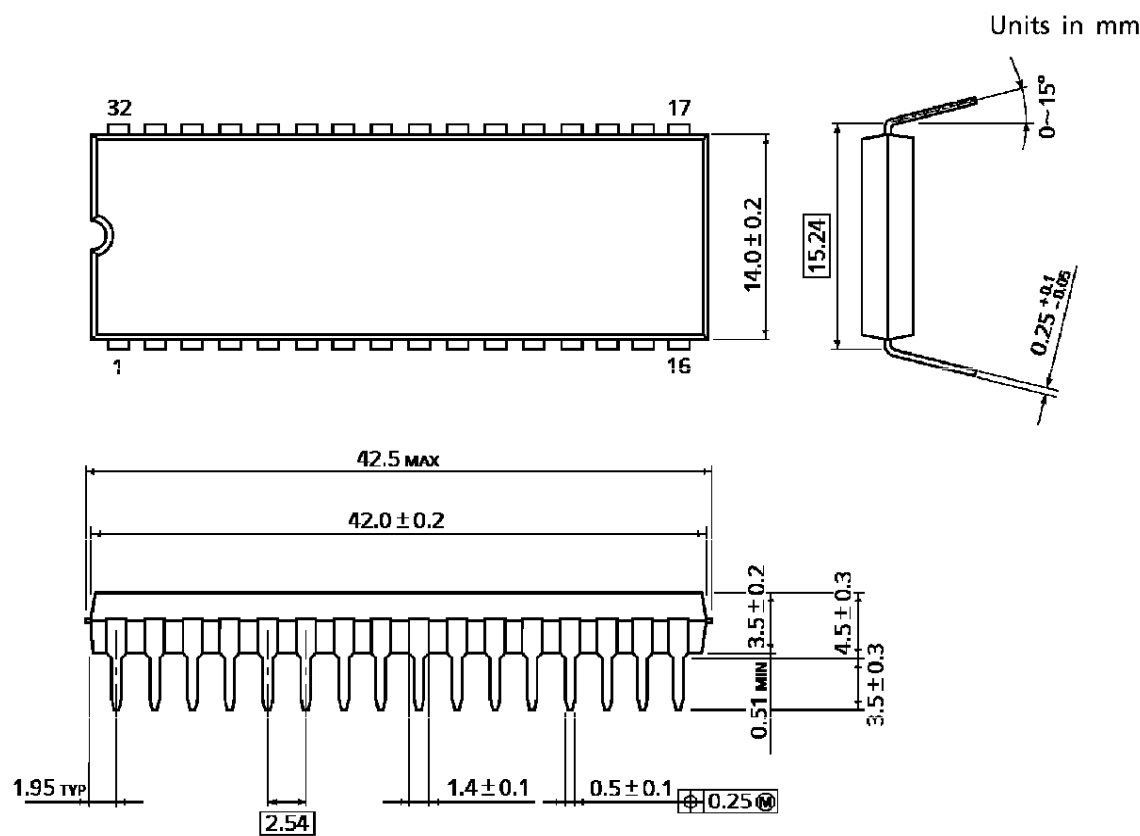
$$CE2 \leq 0.2 \text{ V or } CE2 \geq V_{DD} - 0.2 \text{ V.}$$

(2) When $\overline{CE1}$ is operating at the V_{IH} level (2.4 V), the operation current is given by I_{DDs1} during the transition of V_{DD} from 4.5 to 2.6 V.

(3) In $CE2$ controlled data retention mode, minimum standby current mode is entered when

$$CE2 \leq 0.2 \text{ V.}$$

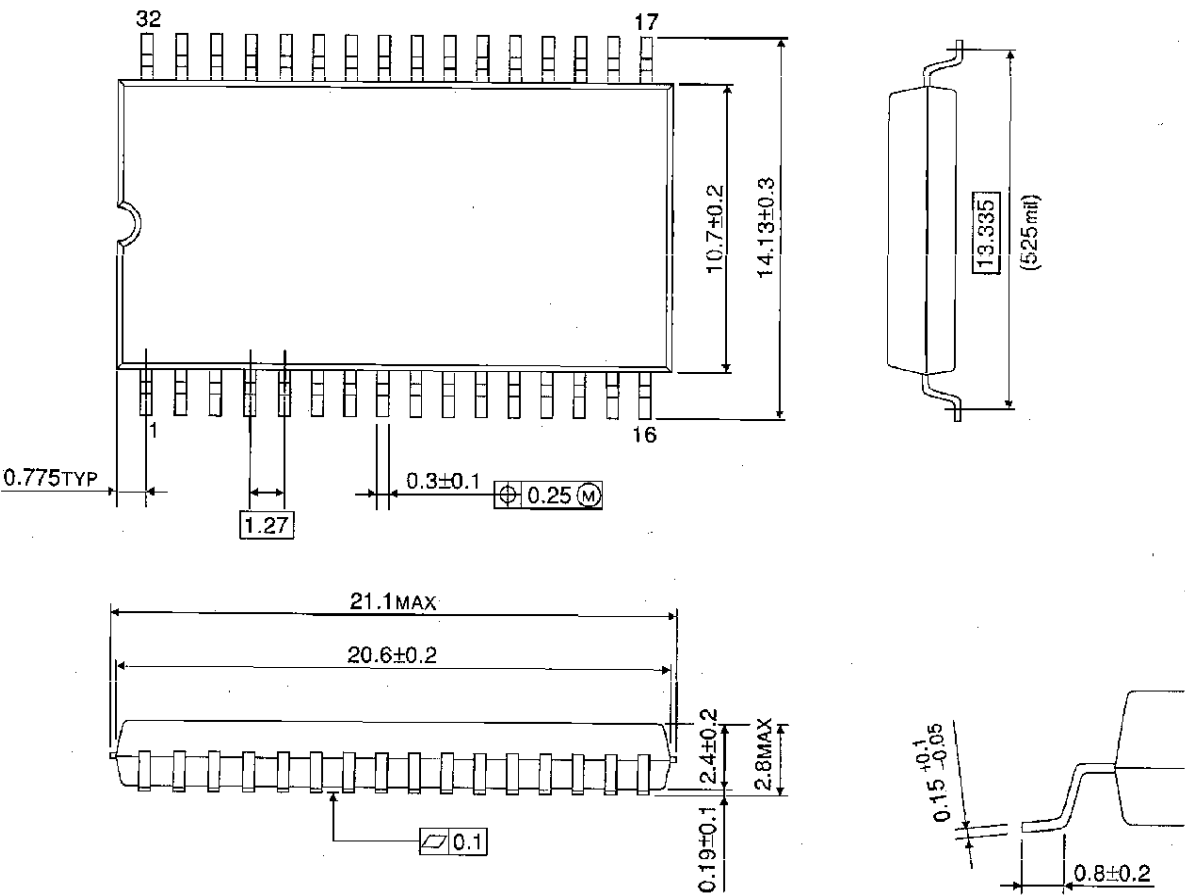
PACKAGE DIMENSIONS (DIP32-P-600-2.54)



Weight: 4.45 g (typ)

PACKAGE DIMENSIONS (SOP32-P-525-1.27)

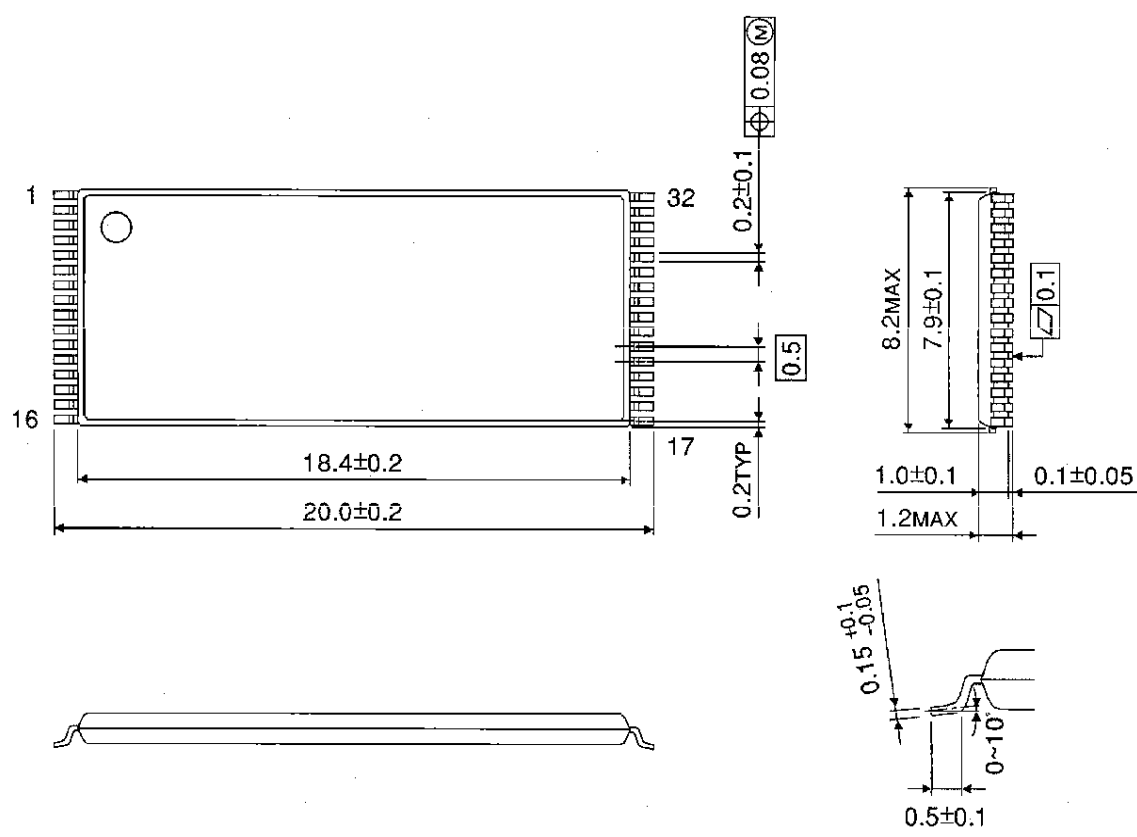
Units in mm



Weight: 1.04 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0820-0.50)

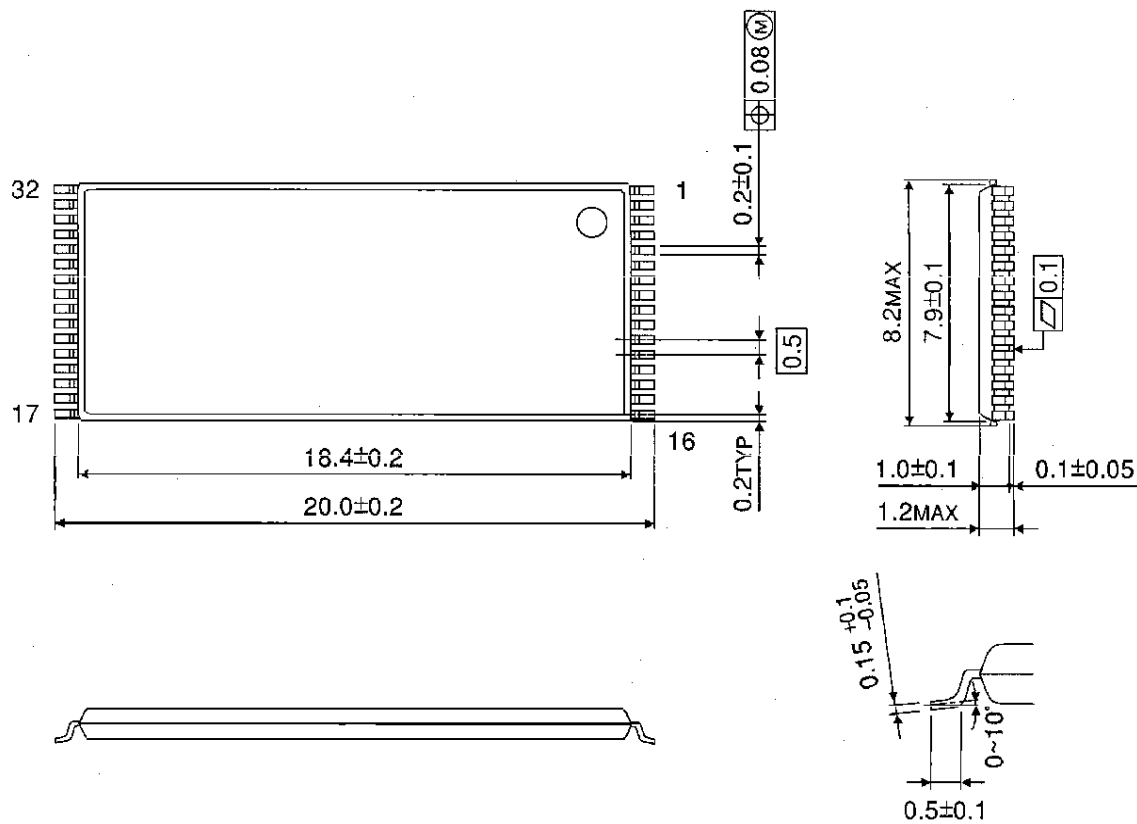
Units in mm



Weight: 0.34 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0820-0.50A)

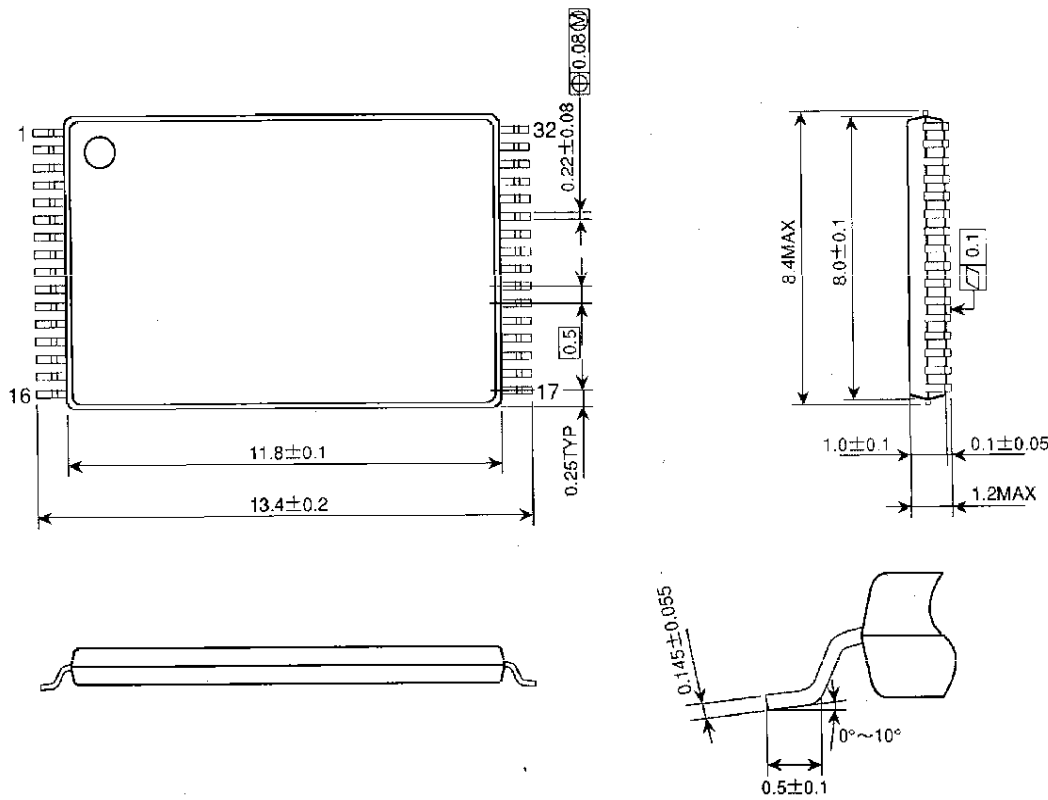
Units in mm



Weight: 0.34 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0.50)

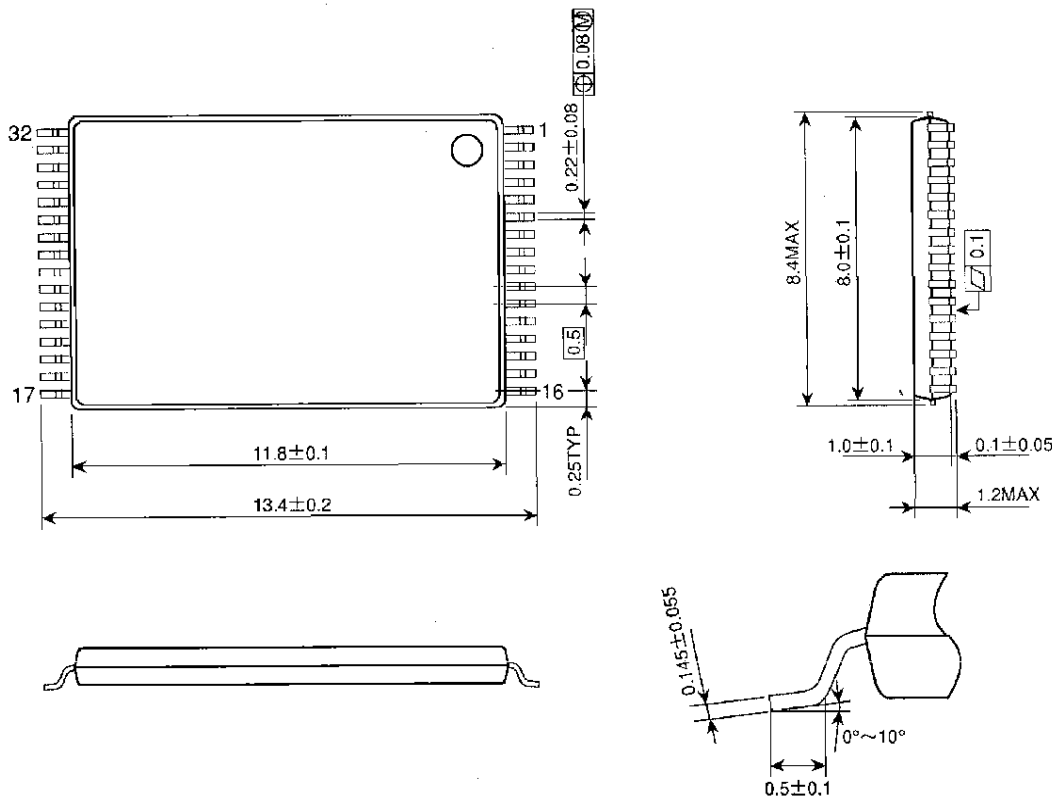
Units in mm



Weight: 0.24 g (typ)

PACKAGE DIMENSIONS (TSOP I 32-P-0.50A)

Units in mm



Weight: 0.24 g (typ)