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The MPC8245 combines a MPC603e core microprocessor with a PCI bridge. The PCI support on the MPC8245 will allow system designers to rapidly design systems using peripherals already designed for PCI and the other standard interfaces. The MPC8245 also integrates a high-performance memory controller which supports various types of ROM and SDRAM. The MPC8245 is the second of a family of products that provides system-level support for industry standard interfaces with a MPC603e processor core.

This document describes pertinent electrical and physical characteristics of the MPC8245. For functional characteristics of the processor, refer to the *MPC8245 Integrated Processor User's Manual* (MPC8245UM/D).

This document contains the following topics:

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http://www.motorola.com/semiconductors

1.1 Overview

The MPC8245 integrated processor is comprised of a peripheral logic block and a 32-bit superscalar MPC603e core, as shown in Figure 1.
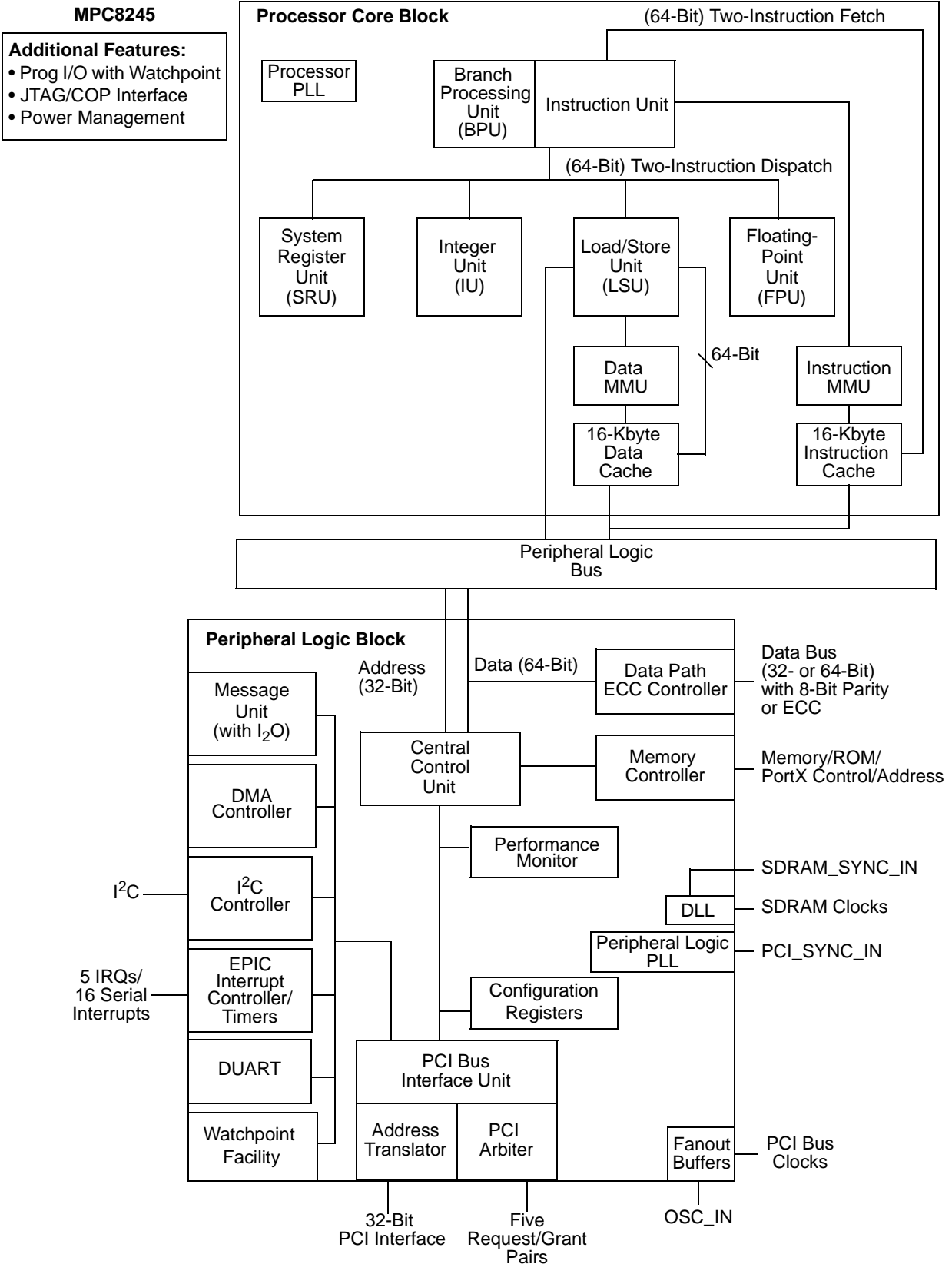
Figure 1. MPC8245 Block Diagram

The peripheral logic integrates a PCI bridge, dual universal asynchronous receiver/transmitter (DUART), memory controller, DMA controller, EPIC interrupt controller, a message unit (and I_2O interface), and an I^2C controller. The processor core is a full-featured, high-performance processor with floating-point support, memory management, 16-Kbyte instruction cache, 16-Kbyte data cache, and power management features. The integration reduces the overall packaging requirements and the number of discrete devices required for an embedded system.

The MPC8245 contains an internal peripheral logic bus that interfaces the processor core to the peripheral logic. The core can operate at a variety of frequencies, allowing the designer to trade-off performance for power consumption. The processor core is clocked from a separate PLL, which is referenced to the peripheral logic PLL. This allows the microprocessor and the peripheral logic block to operate at different frequencies, while maintaining a synchronous bus interface. The interface uses a 64- or 32-bit data bus (depending on memory data bus width) and a 32-bit address bus along with control signals that enable the interface between the processor and peripheral logic to be optimized for performance. PCI accesses to the MPC8245 memory space are passed to the processor bus for snooping when snoop mode is enabled.

The processor core and peripheral logic are general-purpose in order to serve a variety of embedded applications. The MPC8245 can be used as either a PCI host or PCI agent controller.

1.2   Features

Major features of the MPC8245 are as follows:

- Processor core
  - High-performance, superscalar processor core
  - Integer unit (IU), floating-point unit (FPU) (software enabled or disabled), load/store unit (LSU), system register unit (SRU), and a branch processing unit (BPU)
  - 16-Kbyte instruction cache
  - 16-Kbyte data cache
  - Lockable L1 caches—entire cache or on a per-way basis up to three of four ways
  - Dynamic power management—supports 60x nap, doze, and sleep modes
- Peripheral logic
  - Peripheral logic bus
    - Supports various operating frequencies and bus divider ratios
    - 32-bit address bus, 64-bit data bus
    - Supports full memory coherency
    - Decoupled address and data buses for pipelining of peripheral logic bus accesses
    - Store gathering on peripheral logic bus-to-PCI writes
  - Memory interface
    - Supports up to 2 Gbytes of SDRAM memory
    - High-bandwidth data bus (32- or 64-bit) to SDRAM
    - Programmable timing supporting SDRAM
    - Supports 1 to 8 banks of 16-, 64-, 128-, 256-, or 512-Mbit memory devices
    - Write buffering for PCI and processor accesses
    - Supports normal parity, read-modify-write (RMW), or ECC

- – Data-path buffering between memory interface and processor
- – Low-voltage TTL logic (LVTTL) interfaces
- – 272 Mbytes of base and extended ROM/Flash/PortX space
- – Base ROM space supports 8-bit data path or same size as the SDRAM data path (32- or 64-bit)
- – Extended ROM space supports 8-, 16-, 32-bit gathering data path, 32- or 64-bit (wide) data path
- – PortX: 8-, 16-, 32-, or 64-bit general-purpose I/O port using ROM controller interface with programmable address strobe timing, data ready input signal ($\overline{\text{DRDY}}$), and 4 chip selects
— 32-bit PCI interface
- – Operates up to 66 MHz
- – PCI 2.2-compliant
- – PCI 5.0-V tolerance
- – Support for dual address cycle (DAC) for 64-bit PCI addressing (master only)
- – Support for PCI locked accesses to memory
- – Support for accesses to PCI memory, I/O, and configuration spaces
- – Selectable big- or little-endian operation
- – Store gathering of processor-to-PCI write and PCI-to-memory write accesses
- – Memory prefetching of PCI read accesses
- – Selectable hardware-enforced coherency
- – PCI bus arbitration unit (five request/grant pairs)
- – PCI agent mode capability
- – Address translation with two inbound and outbound units (ATU)
- – Some internal configuration registers accessible from PCI
— Two-channel integrated DMA controller (writes to ROM/PortX not supported)
- – Supports direct mode or chaining mode (automatic linking of DMA transfers)
- – Supports scatter gathering—read or write discontinuous memory
- – 64-byte transfer queue per channel
- – Interrupt on completed segment, chain, and error
- – Local-to-local memory
- – PCI-to-PCI memory
- – Local-to-PCI memory
- – PCI memory-to-local memory
— Message unit
- – Two doorbell registers
- – Two inbound and two outbound messaging registers
- – I$_2$O message interface
— I^{2}C controller with full master/slave support that accepts broadcast messages

— Embedded programmable interrupt controller (EPIC)

– Five hardware interrupts (IRQs) or 16 serial interrupts

– Four programmable timers with cascade

— Two (dual) universal asynchronous receiver/transmitters (UARTs)

— Integrated PCI bus and SDRAM clock generation

— Programmable PCI bus and memory interface output drivers

• System level performance monitor facility

• Debug features

— Memory attribute and PCI attribute signals

— Debug address signals

— $\overline{\text{MIV}}$ signal: marks valid address and data bus cycles on the memory bus

— Programmable input and output signals with watchpoint capability

— Error injection/capture on data path

— IEEE 1149.1 (JTAG)/test interface

1.3   General Parameters

The following list provides a summary of the general parameters of the MPC8245:

Technology	0.25 µm CMOS, five-layer metal
Die size	49.2 mm^2
Transistor count	4.5 million
Logic design	Fully static
Packages	Surface-mount 352 tape ball grid array (TBGA)
Core power supply:	1.8 V ± 100 mV DC (only for 266 and 300 MHz parts) 2.0 V ± 100 mV DC (for 266, 300, 333, and 350 MHz parts) (nominal; see Table 2 for details and recommended operating conditions)
I/O power supply	3.0 to 3.6 V DC

1.4   Electrical and Thermal Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8245.

1.4.1   DC Electrical Characteristics

This section covers ratings, conditions, and other characteristics.

1.4.1.1 Absolute Maximum Ratings

The tables in this section describe the MPC8245 DC electrical characteristics. Table 1 provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings

Characteristic [1]	Symbol	Range	Unit
Supply Voltage—CPU Core and Peripheral Logic	Vdd	–0.3 to 2.1	V
Supply Voltage—Memory Bus Drivers	GVdd	–0.3 to 3.6	V
Supply Voltage—PCI and Standard I/O Buffers	OVdd	–0.3 to 3.6	V
Supply Voltage—PLLs	AVdd/AVdd2	–0.3 to 2.1	V
Supply Voltage—PCI Reference	LVdd	–0.3 to 5.4	V
Input Voltage [2]	V_{IN}	–0.3 to 3.6	V
Operational Die-Junction Temperature Range	T_J	0 to 105	°C
Storage Temperature Range	T_{STG}	–55 to 150	°C

Notes:
1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. PCI inputs with LVdd = 5 V ± 5% V DC may be correspondingly stressed at voltages exceeding LVdd + 0.5 V DC.

1.4.1.2 Recommended Operating Conditions

Table 2 provides the recommended operating conditions for the MPC8245.

Table 2. Recommended Operating Conditions

Characteristic		Symbol	Recommended Value	Unit	Notes
Supply Voltage		Vdd	1.8 ± 100 mV	V	4, 6
			2.0 ± 100 mV	V	6
I/O Buffer Supply for PCI and Standard		OVdd	3.3 ± 0.3	V	6
Supply Voltages for Memory Bus Drivers		GVdd	3.3 ± 5%	V	8
CPU PLL Supply Voltage		AVdd	1.8 ± 100 mV	V	4, 6
			2.0 ± 100 mV	V	6
PLL Supply Voltage—Peripheral Logic		AVdd2	1.8 ± 100 mV	V	4, 6
			2.0 ± 100 mV	V	6
PCI Reference		LVdd	5.0 ± 5%	V	2, 9, 10
			3.3 ± 0.3	V	3, 9, 10
Input Voltage	PCI Inputs	V_{IN}	0 to 3.6 or 5.75	V	2, 3
	All Other Inputs		0 to 3.6	V	5

Table 2. Recommended Operating Conditions (continued)

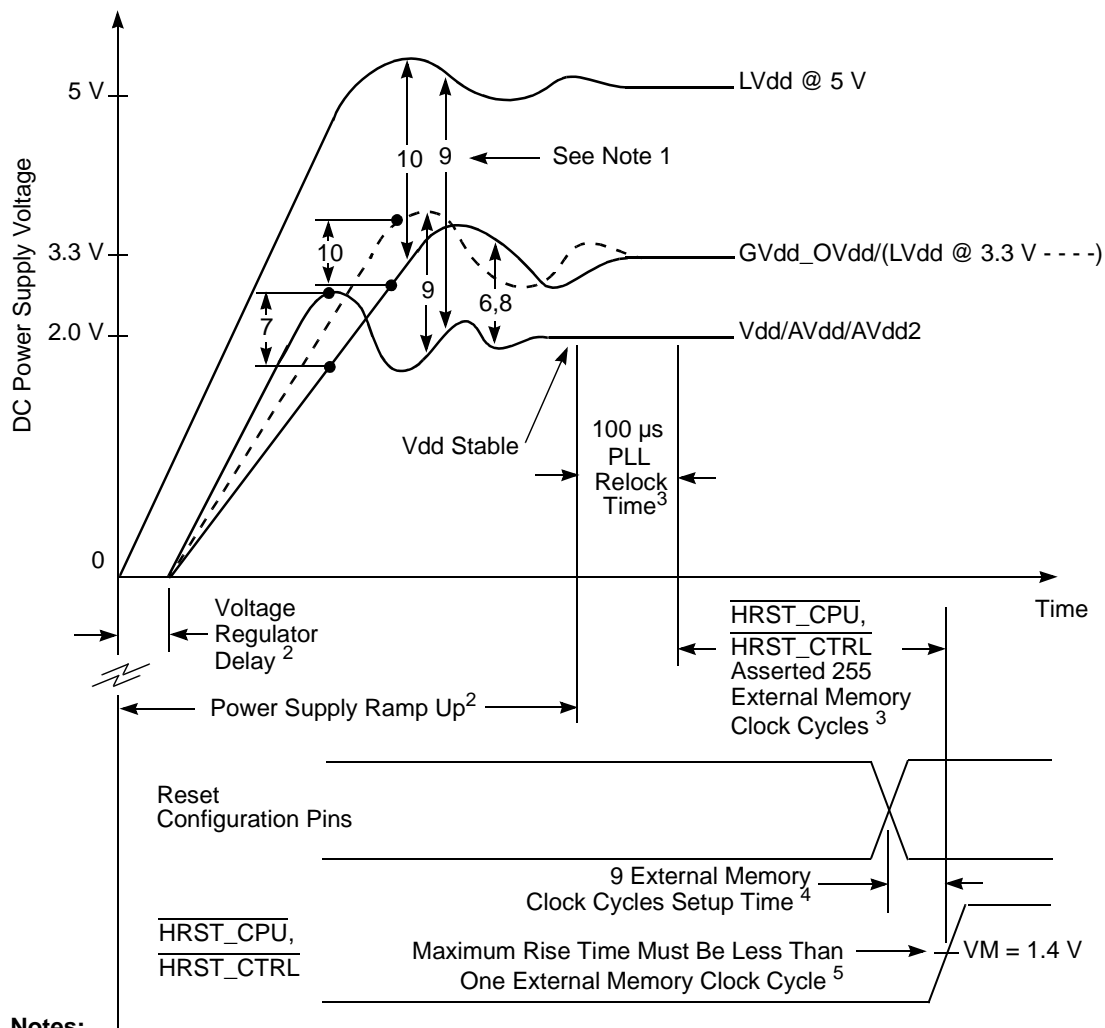| Characteristic	Symbol	Recommended Value	Unit	Notes
Die-Junction Temperature	T_J	0 to 105	°C	

Notes:
1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. PCI pins are designed to withstand LVdd + 0.5 V dc when LVdd is connected to a 5.0 V dc power supply.
3. PCI pins are designed to withstand LVdd + 0.5 V dc when LVdd is connected to a 3.3 V dc power supply.
4. CPU speed limited to 266 MHz and 300 MHz operation at this voltage. See Table 9.

Cautions:
5. Input voltage (V_{IN}) must not be greater than the supply voltage (Vdd/AVdd/AVdd2) by more than 2.5 V at all times including during power-on reset. Input voltage (V_{IN}) must not be greater than GVdd/OVdd by more than 0.6 V at all times including during power-on reset.
6. OVdd must not exceed Vdd/AVdd/AVdd2 by more than 1.8 V at any time including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
7. Vdd/AVdd/AVdd2 must not exceed OVdd by more than 0.6 V at any time including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
8. GVdd must not exceed Vdd/AVdd/AVdd2 by more than 1.8 V at any time including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
9. LVdd must not exceed Vdd/AVdd/AVdd2 by more than 5.4 V at any time including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
10. LVdd must not exceed OVdd by more than 3.0 V at any time including during power-on reset. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.

Figure 2 shows supply voltage sequencing and separation cautions.

Notes:

1. Numbers associated with waveform separations correspond to caution numbers listed in Table 2.
2. Refer to Section 1.7.2, "Power Supply Sizing" for additional information on this topic.
3. Refer to Table 8 for additional information on PLL relock and reset signal assertion timing requirements.
4. Refer to Table 9 for additional information on reset configuration pin setup timing requirements.
5. HRST_CPU/HRST_CTRL must transition from a logic 0 to a logic 1 in less than one SDRAM_SYNC_IN clock cycle for the device to be in the nonreset state.

Figure 2. Supply Voltage Sequencing and Separation Cautions

Figure 3 shows the undershoot and overshoot voltage of the memory interface of the MPC8245.
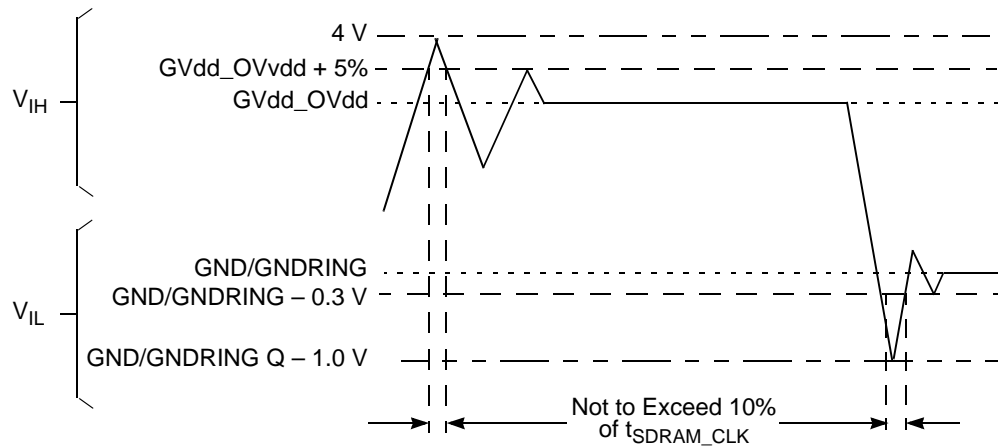
Figure 3. Overshoot/Undershoot Voltage

1.4.1.3 DC Electrical Characteristics

Table 3 provides the DC electrical characteristics for the MPC8245 at recommended operating conditions.

Table 3. DC Electrical Specifications

At recommended operating conditions (see Table 2)

Characteristic	Condition [3]	Symbol	Min	Max	Unit
Input High Voltage [1]	PCI only	V_{IH}	$0.65 \times OVdd$	LVdd	V
Input Low Voltage	PCI only	V_{IL}	—	$0.3 \times OVdd$	V
Input High Voltage	All other pins (GVdd = 3.3 V)	V_{IH}	2.0	3.3	V
Input Low Voltage	All inputs except PCI_SYNC_IN	V_{IL}	GND	0.8	V
PCI_SYNC_IN Input High Voltage		CV_{IH}	2.4	—	V
PCI_SYNC_IN Input Low Voltage		CV_{IL}	GND	0.4	V
Input Leakage Current [4] for Pins Using DRV_PCI Driver	$0.5\ V \leq V_{IN} \leq 2.7\ V$ @ LVdd = 4.75	I_L	—	±70	µA
Input Leakage Current [4] All Others	LVdd = 3.6 V GVdd ≤ 3.465	I_L	—	±10	µA
Output High Voltage	I_{OH} = Driver Dependent [2] (GVdd = 3.3 V)	V_{OH}	2.4	—	V
Output Low Voltage	I_{OL} = Driver Dependent [2] (GVdd = 3.3 V)	V_{OL}	—	0.4	V

Table 3. DC Electrical Specifications (continued)

At recommended operating conditions (see Table 2)

Characteristic	Condition [3]	Symbol	Min	Max	Unit
Capacitance	V_{IN} = 0 V, f = 1 MHz	C_{IN}	—	7.0	pF

Notes:
1. See Table 16 for pins with internal pull-up resistors.
2. See Table 4 for the typical drive capability of a specific signal pin based on the type of output driver associated with that pin as listed in Table 16.
3. These specifications are for the default driver strengths indicated in Table 4.
4. Leakage current is measured on input and output pins in the high-impedance state. The leakage current is measured for nominal OVdd/LVdd and Vdd or both OVdd/LVdd and Vdd must vary in the same direction.

1.4.1.4   Output Driver Characteristics

Table 4 provides information on the characteristics of the output drivers referenced in Table 16. The values are preliminary estimates from an IBIS model and are not tested.

Table 4. Drive Capability of MPC8245 Output Pins [5]

Driver Type	Programmable Output Impedance (Ω)	Supply Voltage	I_{OH}	I_{OL}	Unit	Notes
DRV_STD_MEM	20	OVdd = 3.3 V	36.6	18.0	mA	2, 4, 6
	40 (default)		18.6	9.2	mA	2, 4, 6
DRV_PCI	20		12.0	12.4	mA	1, 3
	40 (default)		6.1	6.3	mA	1, 3
DRV_MEM_CTRL DRV_PCI_CLK DRV_MEM_CLK	6 (default)	GVdd = 3.3 V	89.0	42.3	mA	2, 4
	20		36.6	18.0	mA	2, 4
	40		18.6	9.2	mA	2, 4

Notes:
1. For DRV_PCI, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.33 V label by interpolating between the 0.3 V and 0.4 V table entries' current values which corresponds to the PCI V_{OH} = 2.97 = 0.9 $\times$ OVdd (OVdd = 3.3 V) where table entry voltage = OVdd − PCI V_{OH}.
2. For all others with GVdd or OVdd = 3.3 V, I_{OH} read from the IBIS listing in the pull-up mode, I(Min) column, at the 0.9 V table entry which corresponds to the V_{OH} = 2.4 V where table entry voltage = GVdd/OVdd − V_{OH}.
3. For DRV_PCI, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at 0.33 V = PCI V_{OL} = 0 $\times$ OVdd (OVdd = 3.3 V) by interpolating between the 0.3 V and 0.4 V table entries.
4. For all others with GVdd or OVdd = 3.3 V, I_{OL} read from the IBIS listing in the pull-down mode, I(Min) column, at the 0.4 V table entry.
5. See driver bit details for output driver control register (0x72) in the *MPC8245 Integrated Processor User's Manual*.
6. See Chip Errata No. 19 in the *MPC8245/MPC8241 RISC Microprocessor Chip Errata*.

1.4.1.5 Power Characteristics

Table 5 provides preliminary estimated power consumption data for the MPC8245.

Table 5. Preliminary Power Consumption

Mode	PCI Bus Clock/Memory Bus Clock CPU Clock Frequency (MHz)							Unit	Notes
	66/66/266	66/133/266	66/66/300	66/100/300	33/83/333	66/133/333	66/100/350		
Typical	1.5 (1.2)	1.7 (1.3)	1.6 (1.3)	1.7 (1.4)	1.8	2.0	1.9	W	1, 5
Max—FP	1.9 (1.5)	2.1 (1.7)	2.0 (1.6)	2.1 (1.7)	2.2	2.4	2.4	W	1, 2
Max—INT	1.6 (1.3)	1.8 (1.5)	1.7 (1.4)	1.9 (1.5)	1.9	2.1	2.1	W	1, 3
Doze	1.0 (0.8)	1.3 (1.0)	1.1 (0.9)	1.3 (1.0)	1.3	1.5	1.4	W	1, 4, 6
Nap	0.3 (0.3)	0.5 (0.5)	0.4 (0.3)	0.5 (0.4)	0.4	0.6	0.5	W	1, 4, 6
Sleep	0.4 (0.3)	0.2 (0.2)	0.4 (0.3)	0.4 (0.3)	0.2	0.2	0.4	W	1, 4, 6
I/O Power Supplies [10]									
Mode		Minimum		Maximum			Unit	Notes	
Typ—OVdd		200		500			mW	7, 8	
Typ—GVdd		300		600			mW	7, 9	

Notes:
1. The values include Vdd, AVdd, and AVdd2 but do not include I/O supply power, see Section 1.7.2, "Power Supply Sizing," for information on OVdd and GVdd supply power. Values shown in parenthesis ( ) indicate power consumption at Vdd/AVdd/AVdd2 = 1.8 V.
2. Maximum—FP power is measured at Vdd = 2.1 V with dynamic power management enabled while running an entirely cache-resident, looping, floating-point multiplication instruction.
3. Maximum—INT power is measured at Vdd = 2.1 V with dynamic power management enabled while running entirely cache-resident, looping, integer instructions.
4. Power saving mode maximums are measured at Vdd = 2.1 V while the device is in doze, nap, or sleep mode.
5. Typical power is measured at Vdd = AVdd = 2.0 V, OVdd = 3.3 V where a nominal FP value, a nominal INT value, and a value where there is a continuous flush of cache lines with alternating ones and zeros on 64-bit boundaries to local memory are averaged.
6. Power saving mode data measured with only two PCI_CLKs and two SDRAM_CLKs enabled.
7. The typical minimum I/O power values were results of the MPC8245 performing cache resident integer operations at the slowest frequency combination of 33:66:200 (PCI:Mem:CPU) MHz.
8. The typical maximum OVdd value resulted from the MPC8245 operating at the fastest frequency combination of 66:100:350 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros to PCI memory.
9. The typical maximum GVdd value resulted from the MPC8245 operating at the fastest frequency combination of 66:100:350 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros on 64-bit boundaries to local memory.
10. Power consumption of PLL supply pins (AVdd and AVdd2) < 15 mW. Guaranteed by design and is not tested.

1.4.2   Thermal Characteristics

Table 6 provides the package thermal characteristics for the MPC8245. For further information, see Section 1.7.9, "Thermal Management Information."

Table 6. Thermal Characterization Data

Characteristic	Symbol	Value	Unit
Die Junction-to-Case Thermal Resistance	θ_{JC}	1.8	°C/W
Die Junction-to-Board Thermal Resistance	θ_{JB}	4.8	°C/W

Note: Refer to Section 1.7, "System Design Information," for more details about thermal management.

1.4.3   AC Electrical Characteristics

This section provides the AC electrical characteristics for the MPC8245. After fabrication, functional parts are sorted by maximum processor core frequency as shown in Table 7 and tested for conformance to the AC specifications for that frequency. The processor core frequency is determined by the bus (PCI_SYNC_IN) clock frequency and the settings of the PLL_CFG[0:4] signals. Parts are sold by maximum processor core frequency. See Section 1.9, "Ordering Information."

Table 7 provides the operating frequency information for the MPC8245 at recommended operating conditions (see Table 2) with LVdd = 3.3 V ± 0.3 V.

Table 7. Operating Frequency [1]

Characteristic [2, 3]	266 MHz	300 MHz	333 MHz	350 MHz	Unit
	Vdd/AVdd/AVdd2 = 1.8/2.0 ± 100 mV		Vdd/AVdd/AVdd2 = 2.0 ± 100 mV		
Processor Frequency (CPU)	100–266	100–300	100–333	100–350	MHz
Memory Bus Frequency	33–133	33–100 [4]	33–133	33–100 [4]	MHz
PCI Input Frequency	25–66				MHz

Notes:
1. See part number specification document MPC8245RZUPNS/D for additional part offering information.
2. **Caution:** The PCI_SYNC_IN frequency and PLL_CFG[0:4] settings must be chosen such that the resulting peripheral logic/memory bus frequency and CPU (core) frequencies do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0:4] signal description in Section 1.6, "PLL Configuration," for valid PLL_CFG[0:4] settings and PCI_SYNC_IN frequencies.
3. See Table 17 and Table 18 for more details on VCO limitations for memory and CPU VCO frequencies of various PLL configurations.
4. There are no available PLL_CFG[0:4] settings which support 133 MHz memory interface operation at 300 MHz CPU and 350 MHz operation, since the multipliers do not allow a 300:133 and 350:133 ratio relation. However, running these parts are slower speeds may produce ratios that will run above 100 MHz. See Table 17 for the PLL settings.

1.4.3.1 Clock AC Specifications

Table 8 provides the clock AC timing specifications at recommended operating conditions, as defined in Section 1.4.3.2, "Input AC Timing Specifications" These specifications are for the default driver strengths indicated in Table 4.

Table 8. Clock AC Timing Specifications

At recommended operating conditions (see Table 2) with LVdd = 3.3 V ± 0.3 V

Num	Characteristics and Conditions	Min	Max	Unit	Notes
1a	Frequency of Operation (PCI_SYNC_IN)	25	66	MHz	
2, 3	PCI_SYNC_IN Rise and Fall Times	—	2.0	ns	1
4	PCI_SYNC_IN Duty Cycle Measured at 1.4 V	40	60	%	
5a	PCI_SYNC_IN Pulse Width High Measured at 1.4 V	6	9	ns	2
5b	PCI_SYNC_IN Pulse Width Low Measured at 1.4 V	6	9	ns	2
7	PCI_SYNC_IN Jitter	—	150	ps	
8a	PCI_CLK[0:4] Skew (Pin-to-Pin)	—	250	ps	
8b	SDRAM_CLK[0:3] Skew (Pin-to-Pin)	—	190	ps	3
10	Internal PLL Relock Time	—	100	µs	2, 4, 5
15	DLL Lock Range with DLL_EXTEND = 0 Disabled (Default)	$0 \leq (NT_{clk} - t_{loop} - t_{fix0}) \leq 7$		ns	6
16	DLL Lock Range with DLL_EXTEND = 1 Enabled	$0 \leq (NT_{clk} - T_{clk}/2 - t_{loop} - t_{fix0}) \leq 7$		ns	6
17	Frequency of Operation (OSC_IN)	25	66	MHz	
19	OSC_IN Rise and Fall Times	—	5	ns	7
20	OSC_IN Duty Cycle Measured at 1.4 V	40	60	%	
21	OSC_IN Frequency Stability	—	100	ppm	

Notes:
1. Rise and fall times for the PCI_SYNC_IN input are measured from 0.4 to 2.4 V.
2. Specification value at maximum frequency of operation.
3. Pin-to-pin skew includes quantifying the additional amount of clock skew (or jitter) from the DLL besides any intentional skew added to the clocking signals from the variable length DLL synchronization feedback loop, that is, the amount of variance between the internal *sys_logic_clk* and the SDRAM_SYNC_IN signal after the DLL is locked. While pin-to-pin skew between SDRAM_CLKs can be measured, the relationship between the internal *sys_logic_clk* and the external SDRAM_SYNC_IN cannot be measured and is guaranteed by design.
4. Relock time is guaranteed by design and characterization. Relock time is not tested.
5. Relock timing is guaranteed by design. PLL-relock time is the maximum amount of time required for PLL lock after a stable Vdd and PCI_SYNC_IN are reached during the reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that HRST_CPU/HRST_CTRL must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the reset sequence.
6. DLL_EXTEND is bit 7 of the PMC2 register <72>. N is a non-zero integer (1 or 2). T_{clk} is the period of one SDRAM_SYNC_OUT clock cycle in ns. T_{loop} is the propagation delay of the DLL synchronization feedback loop (PC board runner) from SDRAM_SYNC_OUT to SDRAM_SYNC_IN in ns; 6.25 inches of loop length (unloaded PC board runner) corresponds to approximately 1 ns of delay. T_{fix0} is a fixed delay inherent in the design when the DLL is at tap point 0 and the DLL is contributing no delay; T_{fix0} equals approximately 3 ns. See Figure 5 through Figure 8 for DLL locking ranges.
7. Rise and fall times for the OSC_IN input is guaranteed by design and characterization. OSC_IN input rise and fall times are not tested.

Electrical and Thermal Characteristics

Figure 4 shows the PCI_SYNC_IN input clock timing diagram and Figure 5 through Figure 8 show the DLL locking range loop delay vs. frequency of operation.

VM = Midpoint Voltage (1.4 V)
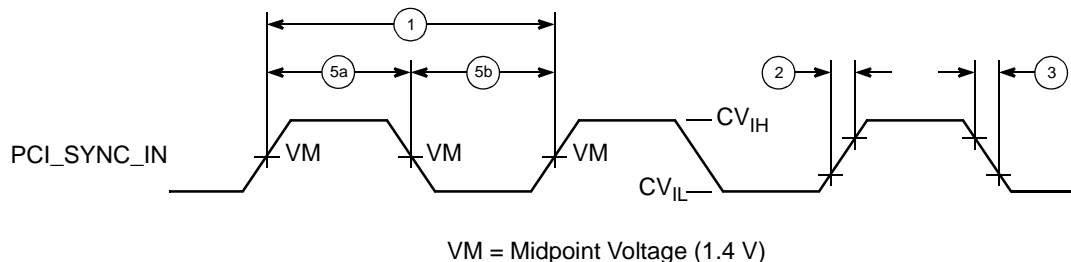
Figure 4. PCI_SYNC_IN Input Clock Timing Diagram

The graphs in Figure 5 through Figure 8 define the areas of DLL locking for various modes. The grey areas represent where the DLL will lock.

Note the following bit descriptions and definitions:

- For standard DLL mode (non-extended): Clear bit 7 (DLL_EXTEND) at offset 0x72 (default).
- For extended DLL mode: Set bit 7 (DLL_EXTEND) at offset 0x72.
- Normal tap delay (default): Clear bit 2 (DLL_MAX_DELAY) at offset 0x76.
- Max tap delay: Set bit 2 (DLL_MAX_DELAY) at offset 0x76.

Note also that the DLL_MAX_DELAY bit can lengthen the amount of time through the delay line. This is accomplished by increasing the time between each of the 128 tap points in the delay line. Although this increased time makes it easier to guarantee that the reference clock will be within the DLL lock range, it also means there may be slightly more jitter in the output clock of the DLL, should the phase comparator shift the clock between adjacent tap points.
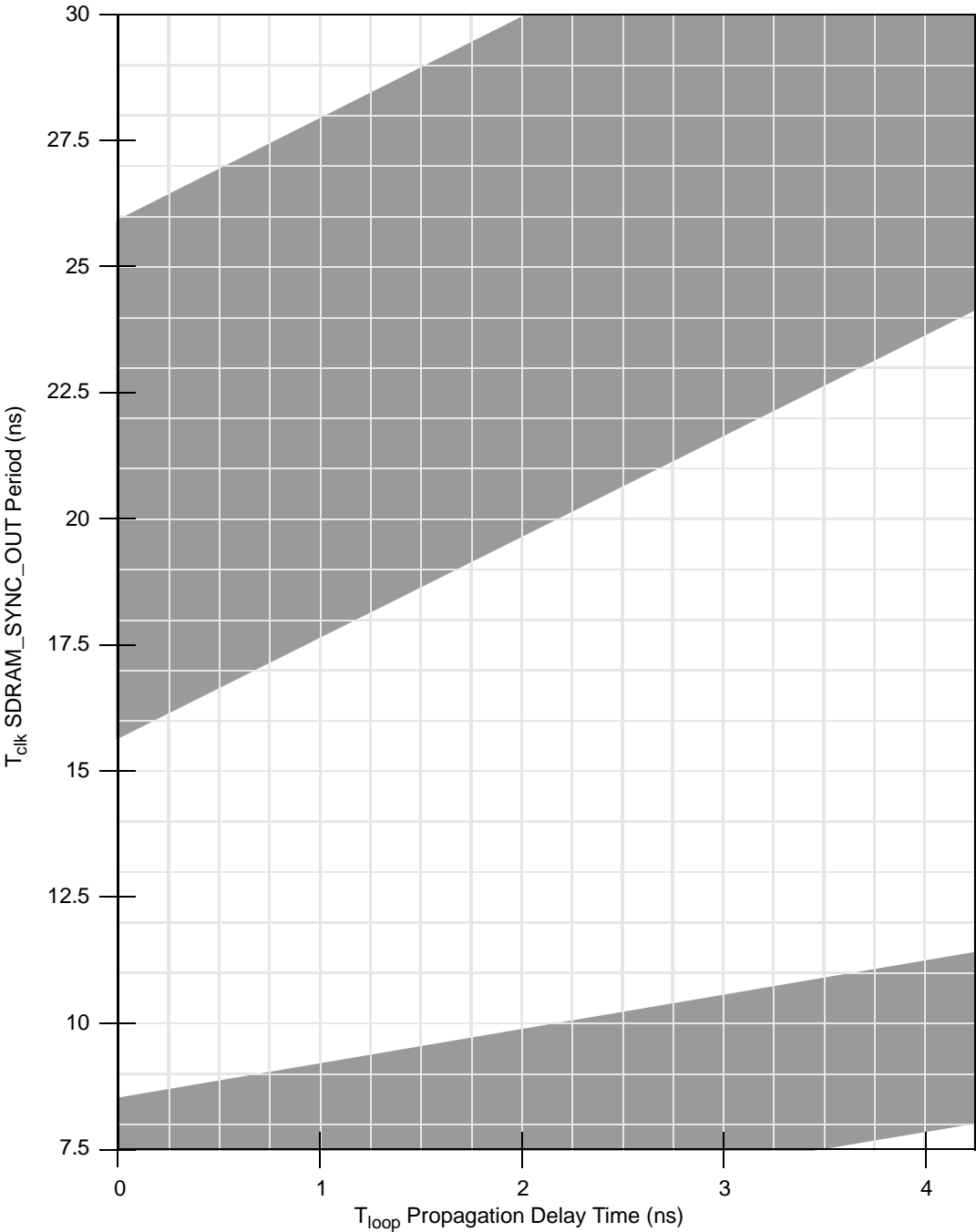
Figure 5. DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend=1 and Normal Tap Delay
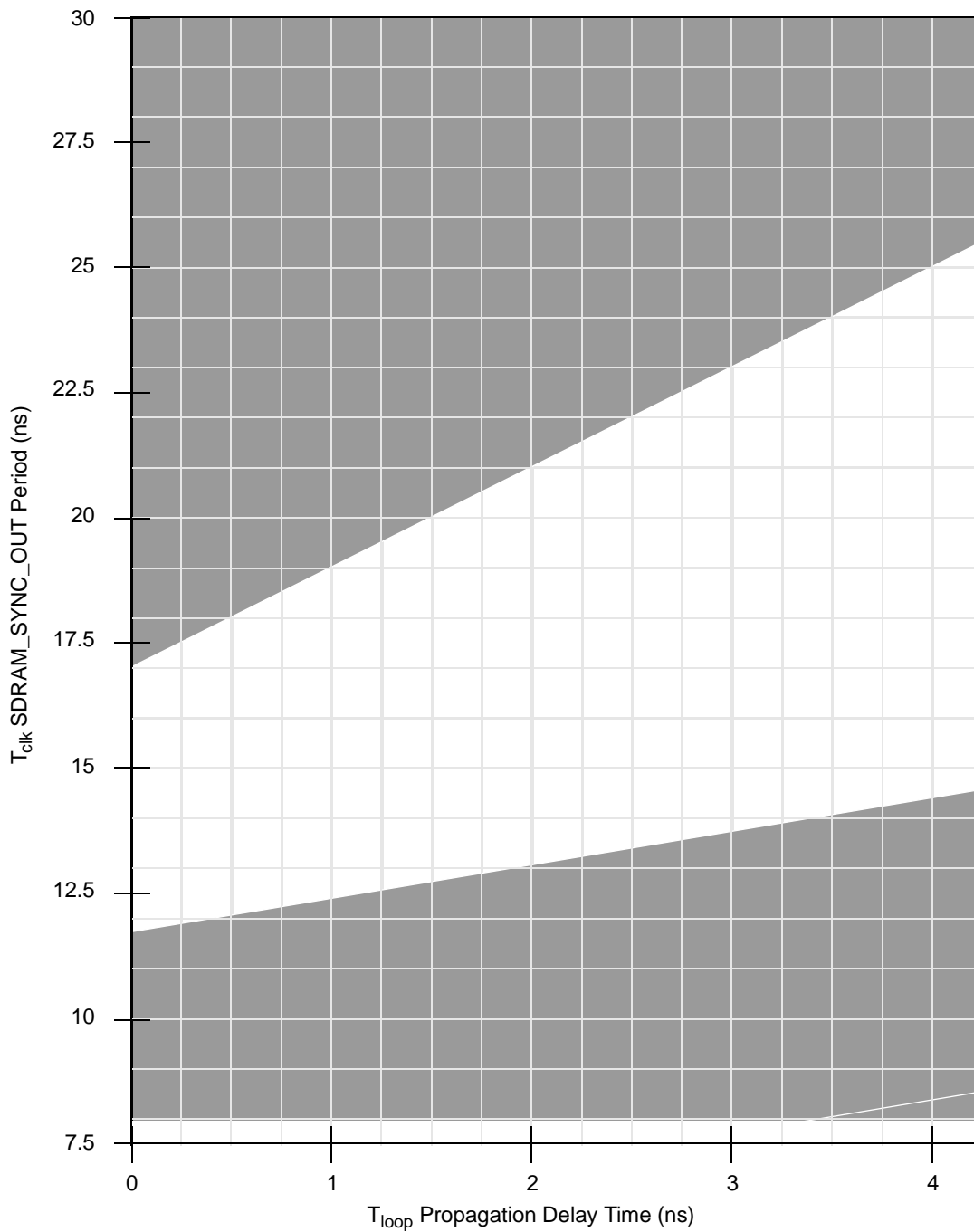
Figure 6. DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend=1 and Tap Max Delay
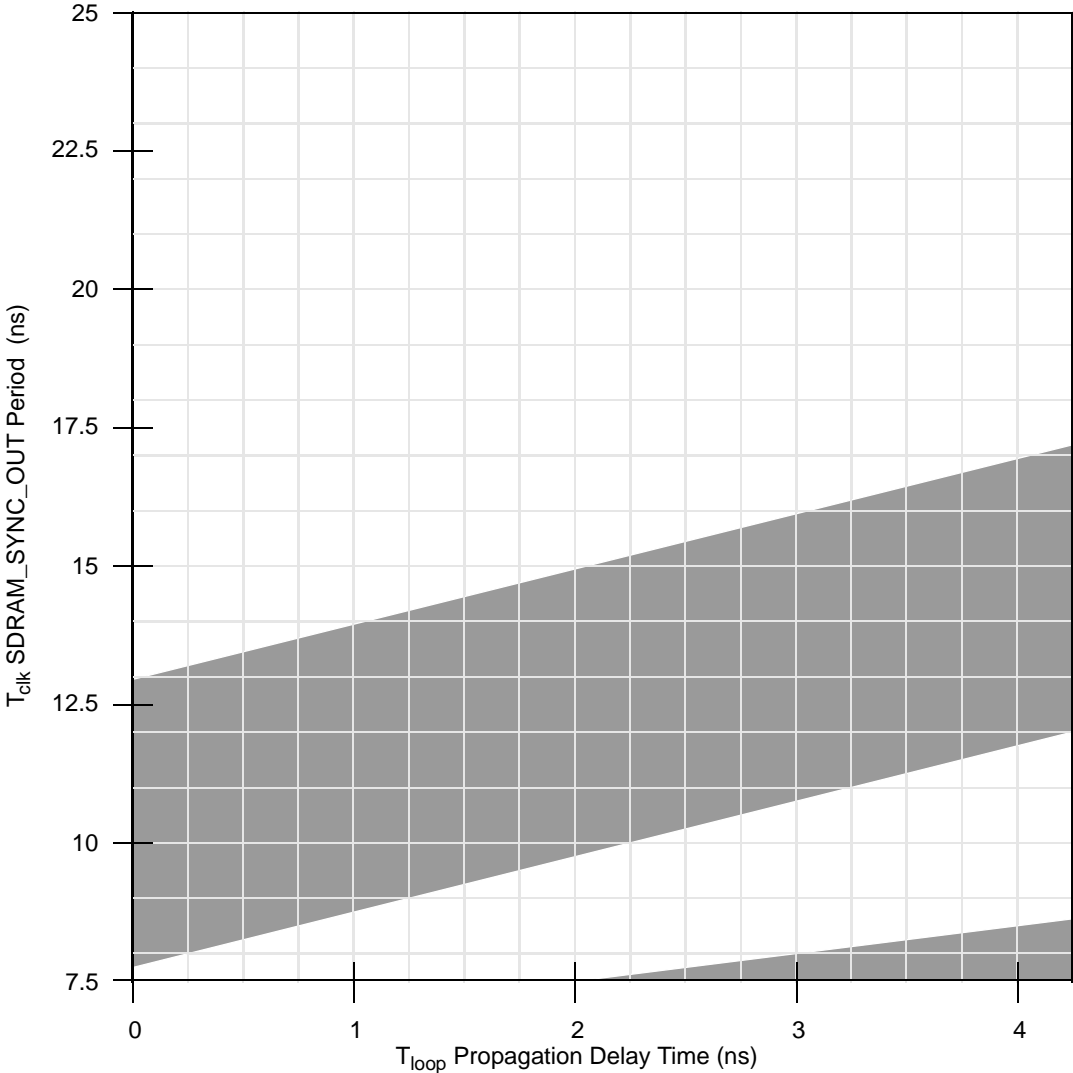
Figure 7. DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend=0 and Normal Tap Delay
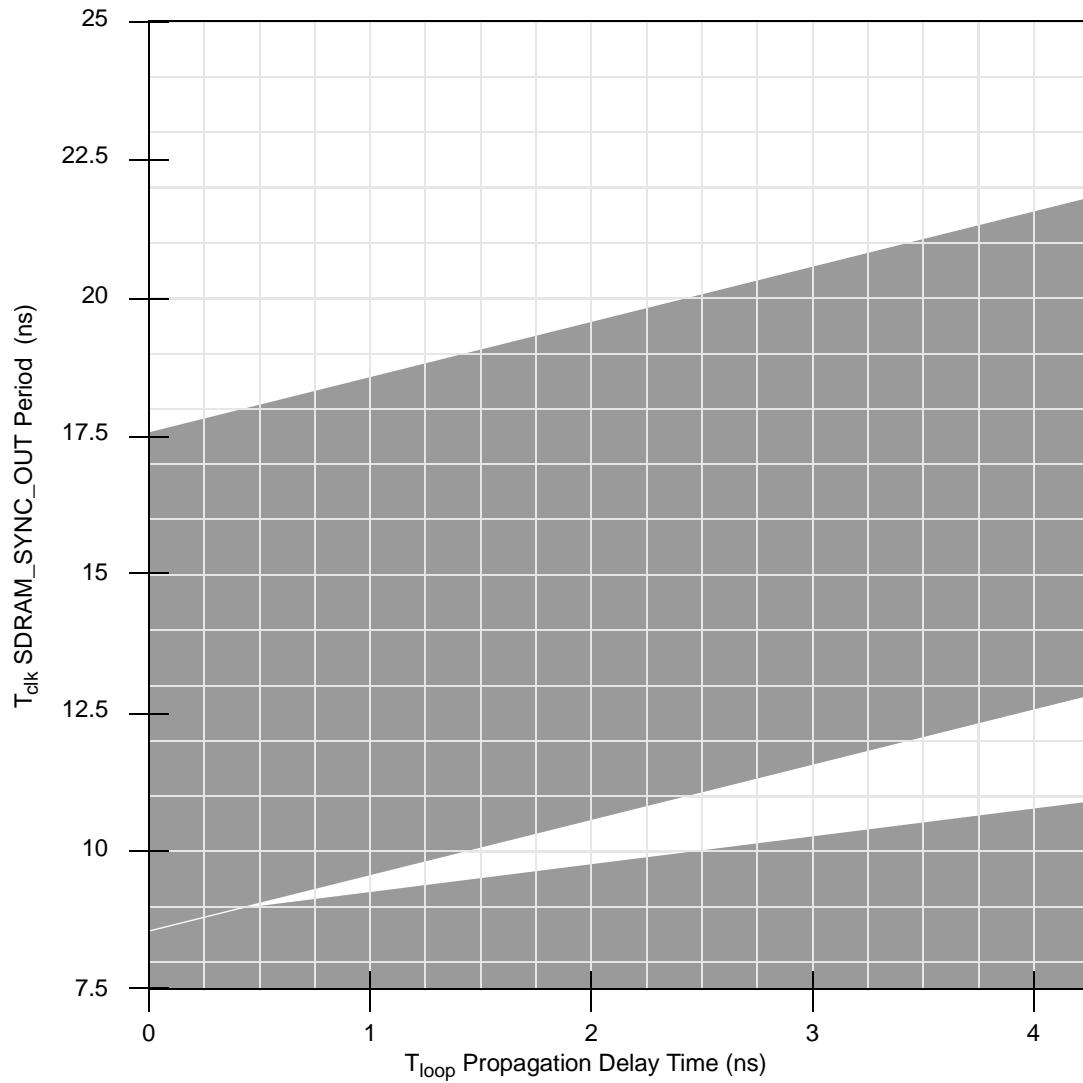
Figure 8. DLL Locking Range Loop Delay vs. Frequency of Operation for DLL_Extend=0 and Max Tap Delay

1.4.3.2 Input AC Timing Specifications

Table 9 provides the input AC timing specifications at recommended operating conditions (see Table 2) with LVdd = 3.3 V ± 0.3 V. See Figure 9 and Figure 10.

Table 9. Input AC Timing Specifications

| Num	Characteristic	Min	Max	Unit	Notes
10a	PCI Input Signals Valid to PCI_SYNC_IN (Input Setup)	3.0	—	ns	1,3
10b	Memory Input Signals Valid to SDRAM_SYNC_IN (Input Setup)				
10b0	Tap 0, Register Offset <0x77>, Bits 5:4 = 0b10	2.6	—	ns	2, 3, 6
10b1	Tap 1, Register Offset <0x77>, Bits 5:4 = 0b11	1.9	—		
10b2	Tap 2, Register Offset <0x77>, Bits 5:4 = 0b00 (Default)	1.2	—		
10b3	Tap 3, Register Offset <0x77>, Bits 5:4 = 0b01	0.5	—		
10c	Epic, Misc. Debug Input Signals Valid to SDRAM_SYNC_IN (Input Setup)	3.0	—	ns	2, 3
10d	I^2C Input Signals Valid to SDRAM_SYNC_IN (Input Setup)	3.0	—	ns	2, 3
10e	Mode Select Inputs Valid to $\overline{HRST\_CPU}/\overline{HRST\_CTRL}$ (Input Setup)	$9 \times t_{CLK}$	—	ns	2, 3–5
11	T_{os} - SDRAM_SYNC_IN to *sys_logic_clk* offset time	0.65	1.0	ns	7
11a	SDRAM_SYNC_IN to Memory Signal Inputs Invalid (Input Hold)				
11a0	Tap 0, Register Offset <0x77>, Bits 5:4 = 0b10	0	—	ns	2, 3, 6
11a1	Tap 1, Register Offset <0x77>, Bits 5:4 = 0b11	0.7	—		
11a2	Tap 2, Register Offset <0x77>, Bits 5:4 = 0b00 (Default)	1.4	—		
11a3	Tap 3, Register Offset <0x77>, Bits 5:4 = 0b01	2.1	—		
11b	$\overline{HRST\_CPU}/\overline{HRST\_CTRL}$ to Mode Select Inputs Invalid (Input Hold)	0	—	ns	2, 3, 5
11c	PCI_SYNC_IN to Inputs Invalid (Input Hold)	1.0	—	ns	1, 2, 3

Notes:
1. All PCI signals are measured from OVdd/2 of the rising edge of PCI_SYNC_IN to $0.4 \times$ OVdd of the signal in question for 3.3 V PCI signaling levels. See Figure 10.
2. All memory and related interface input signal specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the memory bus clock, SDRAM_SYNC_IN. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 9.
3. Input timings are measured at the pin.
4. t_{CLK} is the time of one SDRAM_SYNC_IN clock cycle.
5. All mode select input signals specifications are measured from the TTL level (0.8 or 2.0 V) of the signal in question to the VM = 1.4 V of the rising edge of the $\overline{HRST\_CPU}/\overline{HRST\_CTRL}$ signal. See Figure 11.
6. The memory interface input setup and hold times are programmable to four possible combinations by programming bits 5:4 of register offset <0x77> to select the desired input setup and hold times.
7. T_{os} represents a timing adjustment for SDRAM_SYNC_IN with respect to *sys_logic_clk*. Due to the internal delay present on the SDRAM_SYNC_IN signal with respect to the *sys_logic_clk* inputs to the DLL, the resulting SDRAM clocks become offset by the delay amount. The feedback trace length of SDRAM_SYNC_OUT to SDRAM_SYNC_IN must be shortened by this amount relative to the SDRAM clock output trace lengths to maintain phase-alignment of the memory clocks with respect to *sys_logic_clk*.
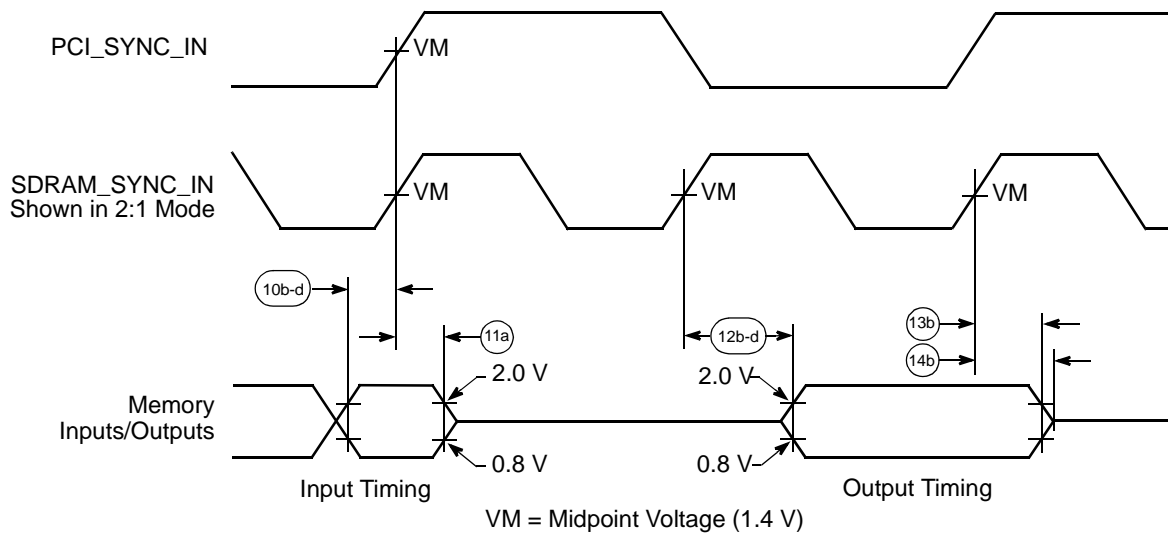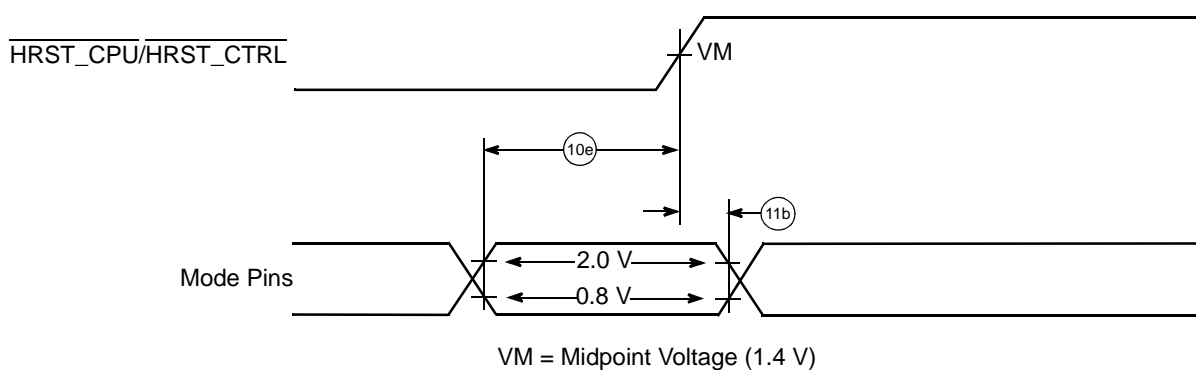
Figure 9. Input/Output Timing Diagram Referenced to SDRAM_SYNC_IN
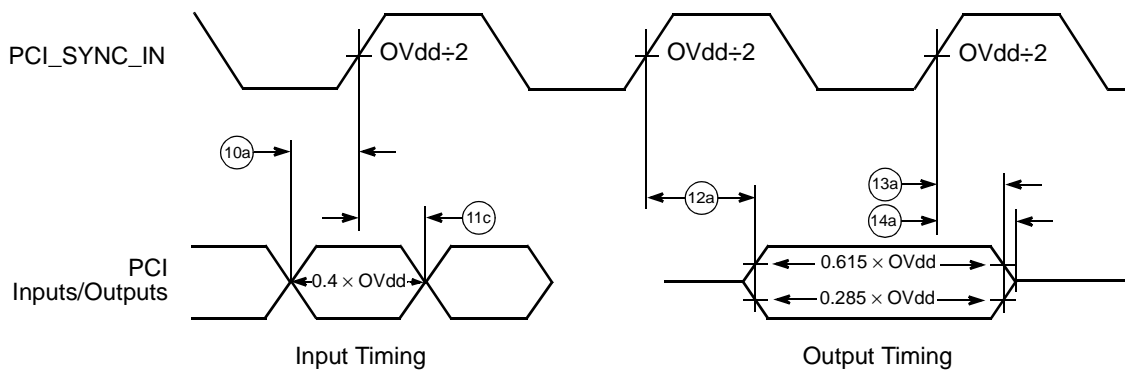
Figure 10. Input/Output Timing Diagram Referenced to PCI_SYNC_IN

Figure 11. Input Timing Diagram for Mode Select Signals

1.4.3.3 Output AC Timing Specification

Table 10 provides the processor bus AC timing specifications for the MPC8245 at recommended operating conditions (see Table 2) with LVdd = 3.3 V ± 0.3V. See Figure 9. All output timings assume a purely resistive 50-Ω load (see Figure 12). Output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system. These specifications are for the default driver strengths indicated in Table 4.

Table 10. Output AC Timing Specifications

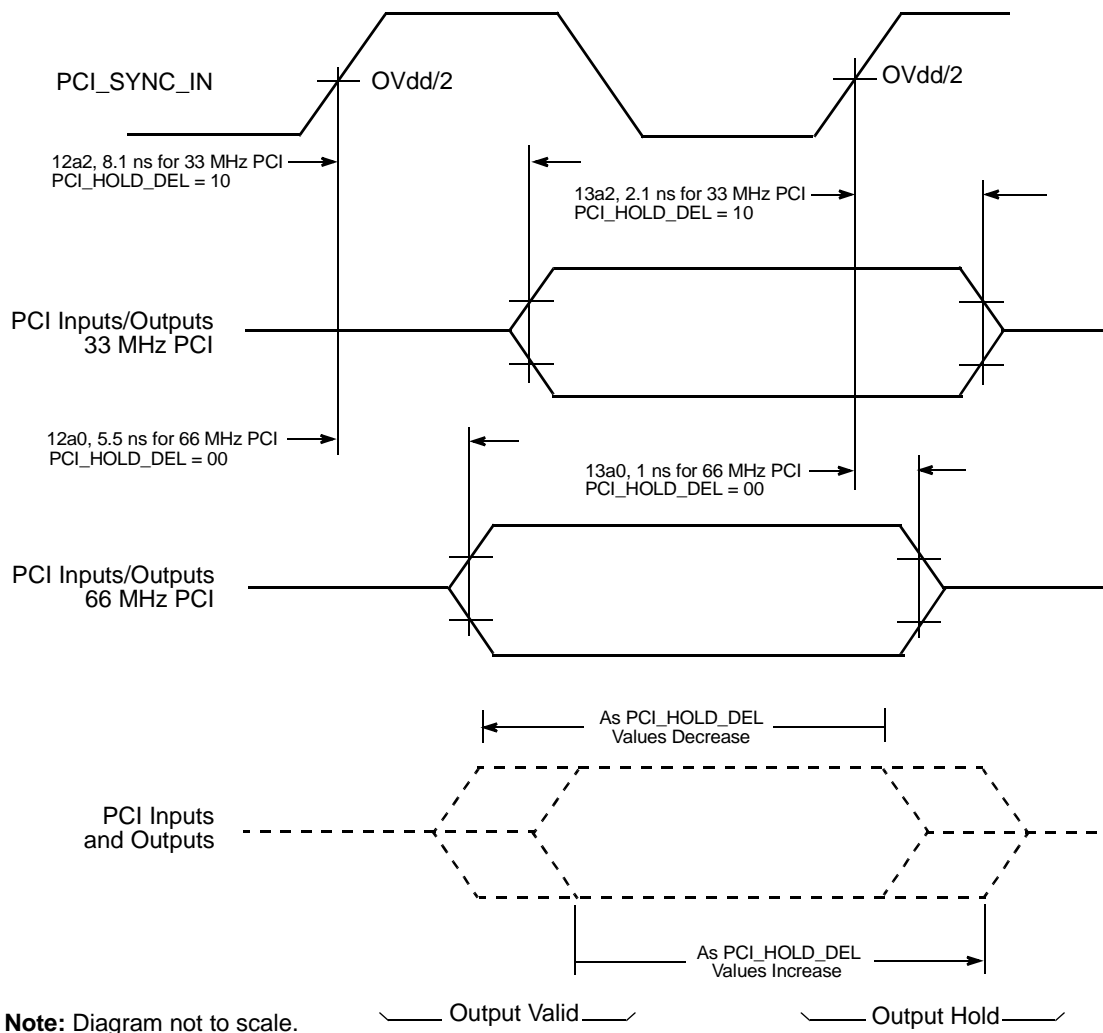| Num	Characteristic	Min	Max	Unit	Notes
12a	PCI_SYNC_IN to Output Valid, see Figure 13				
12a0	Tap 0, PCI_HOLD_DEL=00, [$\overline{MCP}$,CKE] = 11, 66 MHz PCI (Default)	—	6.0	ns	1, 3
12a1	Tap 1, PCI_HOLD_DEL=01, [$\overline{MCP}$,CKE] = 10	—	6.5		
12a2	Tap 2, PCI_HOLD_DEL=10, [$\overline{MCP}$,CKE] = 01, 33 MHz PCI	—	7.0		
12a3	Tap 3, PCI_HOLD_DEL=11, [$\overline{MCP}$,CKE] = 00	—	7.5		
12b	SDRAM_SYNC_IN to Output Valid (Memory Control and Data Signals)	—	4.5	ns	2
12c	SDRAM_SYNC_IN to Output Valid (For All Others)	—	7.0	ns	2
12d	SDRAM_SYNC_IN to Output Valid (For I^{2}C)	—	5.0	ns	2
12e	SDRAM_SYNC_IN to Output Valid (ROM/Flash/PortX)	—	6.0	ns	2
13a	Output Hold (PCI), see Figure 13				
13a0	Tap 0, PCI_HOLD_DEL=00, [$\overline{MCP}$,CKE] = 11, 66 MHz PCI (Default)	2.0	—	ns	1, 3, 4
13a1	Tap 1, PCI_HOLD_DEL=01, [$\overline{MCP}$,CKE] = 10	2.5	—		
13a2	Tap 2, PCI_HOLD_DEL=10, [$\overline{MCP}$,CKE] = 01, 33 MHz PCI	3.0	—		
13a3	Tap 3, PCI_HOLD_DEL=11, [$\overline{MCP}$,CKE] = 00	3.5	—		
13b	Output Hold (All Others)	1.0	—	ns	2
14a	PCI_SYNC_IN to Output High Impedance (For PCI)	—	14.0	ns	1, 3
14b	SDRAM_SYNC_IN to Output High Impedance (For All Others)	—	4.0	ns	2

Notes:
1. All PCI signals are measured from GVdd_OVdd/2 of the rising edge of PCI_SYNC_IN to 0.285 × OVdd or 0.615 × OVdd of the signal in question for 3.3 V PCI signaling levels. See Figure 10.
2. All memory and related interface output signal specifications are specified from the VM = 1.4 V of the rising edge of the memory bus clock, SDRAM_SYNC_IN to the TTL level (0.8 or 2.0 V) of the signal in question. SDRAM_SYNC_IN is the same as PCI_SYNC_IN in 1:1 mode, but is twice the frequency in 2:1 mode (processor/memory bus clock rising edges occur on every rising and falling edge of PCI_SYNC_IN). See Figure 9.
3. PCI bused signals are composed of the following signals: $\overline{LOCK}$, $\overline{IRDY}$, $\overline{C/BE}$[3:0], PAR, $\overline{TRDY}$, $\overline{FRAME}$, $\overline{STOP}$, $\overline{DEVSEL}$, $\overline{PERR}$, $\overline{SERR}$, AD[31:0], $\overline{REQ}$[4:0], $\overline{GNT}$[4:0], IDSEL, $\overline{INTA}$.
4. In order to meet minimum output hold specifications relative to PCI_SYNC_IN for both 33 and 66 MHz PCI systems, the MPC8245 has a programmable output hold delay for PCI signals (the PCI_SYNC_IN to output valid timing is also affected). The initial value of the output hold delay is determined by the values on the $\overline{MCP}$ and CKE reset configuration signals; the values on these two signals are inverted then stored as the initial settings of PCI_HOLD_DEL = PMCR2[5:4] (power management configuration register 2 <0x72>), respectively. Since $\overline{MCP}$ and CKE have internal pull-up resistors, the default value of PCI_HOLD_DEL after reset is 0b00. Further output hold delay values are available by programming the PCI_HOLD_DEL value of the PMCR2 configuration register. See Figure 13.

Output Measurements are Made at the Device Pin

Output — $Z_0 = 50\ \Omega$ — $R_L = 50\ \Omega$ — GVdd_OVdd/2 for PCI or Memory
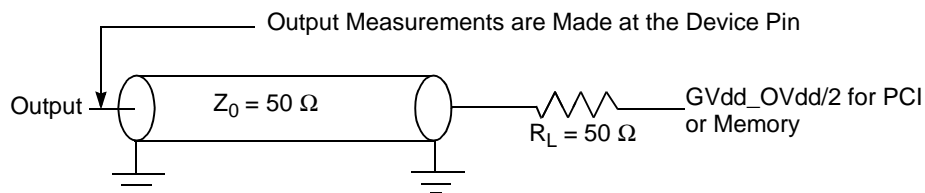
Figure 12. AC Test Load for the MPC8245

PCI_SYNC_IN — OVdd/2 — OVdd/2

12a2, 8.1 ns for 33 MHz PCI
PCI_HOLD_DEL = 10

13a2, 2.1 ns for 33 MHz PCI
PCI_HOLD_DEL = 10

PCI Inputs/Outputs
33 MHz PCI

12a0, 5.5 ns for 66 MHz PCI
PCI_HOLD_DEL = 00

13a0, 1 ns for 66 MHz PCI
PCI_HOLD_DEL = 00

PCI Inputs/Outputs
66 MHz PCI

As PCI_HOLD_DEL
Values Decrease

PCI Inputs
and Outputs

As PCI_HOLD_DEL
Values Increase

Note: Diagram not to scale.   ⎯ Output Valid ⎯   ⎯ Output Hold ⎯

Figure 13. PCI_HOLD_DEL Affect on Output Valid and Hold Time

1.4.3.4 I^{2}C AC Timing Specifications

Table 11 provides the I^{2}C input AC timing specifications for the MPC8245 at recommended operating conditions (see Table 2) with LVdd = 3.3 V $\pm$ 0.3 V.

Table 11. I^{2}C Input AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
1	Start condition hold time	4.0	—	CLKs	1, 2
2	Clock low period (time before the MPC8245 will drive SCL low as a transmitting slave after detecting SCL low as driven by an external master)	$8.0 + (16 \times 2^{FDR[4:2]}) \times (5 - 4(\{FDR[5],FDR[1]\} == b'10) - 3(\{FDR[5],FDR[1]\} == b'11) - 2(\{FDR[5],FDR[1]\} == b'00) - 1(\{FDR[5],FDR[1]\} == b'01))$	—	CLKs	1, 2, 4, 5
3	SCL/SDA rise time (from 0.5 V to 2.4 V)	—	1	ms	
4	Data hold time	0	—	ns	2
5	SCL/SDA fall time (from 2.4 V to 0.5 V)	—	1	ms	
6	Clock high period (time needed to either receive a data bit or generate a START or STOP)	5.0	—	CLKs	1, 2, 5
7	Data setup time	3.0	—	ns	3
8	Start condition setup time (for repeated start condition only)	4.0	—	CLKs	1,2
9	Stop condition setup time	4.0	—	CLKs	1, 2

Notes:
1. Units for these specifications are in SDRAM_CLK units.
2. The actual values depend on the setting of the digital filter frequency sampling rate (DFFSR) bits in the frequency divider register I2CFDR. Therefore, the noted timings in the above table are all relative to qualified signals. The qualified SCL and SDA are delayed signals from what is seen in real time on the I^{2}C bus. The qualified SCL, SDA signals are delayed by the SDRAM_CLK clock times DFFSR times 2 plus 1 SDRAM_CLK clock. The resulting delay value is added to the value in the table (where this note is referenced). See Figure 15.
3. Timing is relative to the sampling clock (not SCL).
4. FDR[*x*] refers to the frequency divider register I2CFDR bit *x*.
5. Input clock low and high periods in combination with the FDR value in the frequency divider register (I2CFDR) determine the maximum I^{2}C input frequency. See Table 12.

Table 12 provides the I^{2}C frequency divider register (I2CFDR) information for the MPC8245.

Table 12. MPC8245 Maximum I²C Input Frequency

FDR Hex [2]	Divider [2] (Dec)	Max I²C Input Frequency [1]		
		SDRAM_CLK @ 33 MHz	SDRAM_CLK @ 50 MHz	SDRAM_CLK @ 100 MHz
20, 21	160, 192	1.13 MHz	1.72 MHz	3.44 MHz
22, 23, 24, 25	224, 256, 320, 384	733	1.11 MHz	2.22 MHz
0, 1	288, 320	540	819	1.63 MHz
2, 3, 26, 27, 28, 29	384, 448, 480, 512, 640, 768	428	649	1.29 MHz
4, 5	576, 640	302	458	917
6, 7, 2A, 2B, 2C, 2D	768, 896, 960, 1024, 1280, 1536	234	354	709
8, 9	1152, 1280	160	243	487
A, B, 2E, 2F, 30, 31	1536, 1792, 1920, 2048, 2560, 3072	122	185	371
C, D	2304, 2560	83	125	251
E, F, 32, 33, 34, 35	3072, 3584, 3840, 4096, 5120, 6144	62	95	190
10, 11	4608, 5120	42	64	128
12, 13, 36, 37, 38, 39	6144, 7168, 7680, 8192, 10240, 12288	31	48	96
14, 15	9216, 10240	21	32	64
16, 17, 3A, 3B, 3C, 3D	12288, 14336, 15360, 16384, 20480, 24576	16	24	48
18, 19	18432, 20480	10	16	32
1A, 1B, 3E, 3F	24576, 28672, 30720, 32768	8	12	24
1C, 1D	36864, 40960	5	8	16
1E, 1F	49152, 61440	4	6	12

Notes:
1. Values are in kHz unless otherwise specified.
2. FDR Hex and Divider (Dec) values are listed in corresponding order.
3. Multiple Divider (Dec) values will generate the same input frequency, but each Divider (Dec) value will generate a unique output frequency as shown in Table 13.

Table 13 provides the I²C output AC timing specifications for the MPC8245 at recommended operating conditions (see Table 2) with LVdd = 3.3 V ± 0.3 V.

Table 13. I²C Output AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
1	Start condition hold time	$(FDR[5] == 0) \times (D_{FDR}/16)/2N + (FDR[5] == 1) \times (D_{FDR}/16)/2M$	—	CLKs	1, 2, 3
2	Clock low period	$D_{FDR}/2$	—	CLKs	1, 2, 3
3	SCL/SDA rise time (from 0.5 V to 2.4 V)	—	—	ms	4
4	Data hold time	$8.0 + (16 \times 2^{FDR[4:2]}) \times (5 - 4(\{FDR[5],FDR[1]\} == b'10) - 3(\{FDR[5],FDR[1]\} == b'11) - 2(\{FDR[5],FDR[1]\} == b'00) - 1(\{FDR[5],FDR[1]\} == b'01))$	—	CLKs	1, 2, 3
5	SCL/SDA fall time (from 2.4 V to 0.5 V)	—	< 5	ns	5
6	Clock high time	$D_{FDR}/2$	—	CLKs	1, 2, 3
7	Data setup time (MPC8245 as a master only)	$(D_{FDR}/2)$ – (output data hold time)	—	CLKs	1, 3
8	Start condition setup time (for repeated start condition only)	D_{FDR} + (output start condition hold time)	—	CLKs	1, 2, 3
9	Stop condition setup time	4.0	—	CLKs	1, 2

Notes:

1. Units for these specifications are in SDRAM_CLK units.
2. The actual values depend on the setting of the digital filter frequency sampling rate (DFFSR) bits in the frequency divider register I2CFDR. Therefore, the noted timings in the above table are all relative to qualified signals. The qualified SCL and SDA are delayed signals from what is seen in real time on the I²C bus. The qualified SCL, SDA signals are delayed by the SDRAM_CLK clock times DFFSR times 2 plus 1 SDRAM_CLK clock. The resulting delay value is added to the value in the table (where this note is referenced). See Figure 15.
3. D_{FDR} is the decimal divider number indexed by FDR[5:0] value. Refer to Table 10-5 in the *MPC8245 Integrated Processor User's Manual.* FDR[x] refers to the frequency divider register I2CFDR bit *x*. N is equal to a variable number that would make the result of the divide (data hold time value) equal to a number less than 16.
   M is equal to a variable number that would make the result of the divide (data hold time value) equal to a number less than 9.
4. Since SCL and SDA are open-drain type outputs, which the MPC8245 can only drive low, the time required for SCL or SDA to reach a high level depends on external signal capacitance and pull-up resistor values.
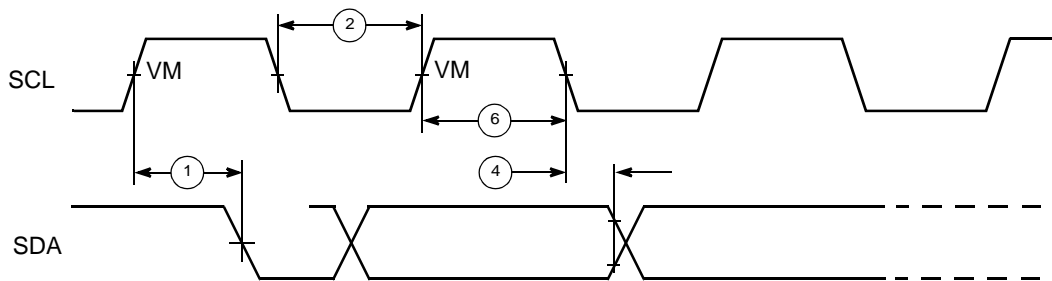5. Specified at a nominal 50 pF load.
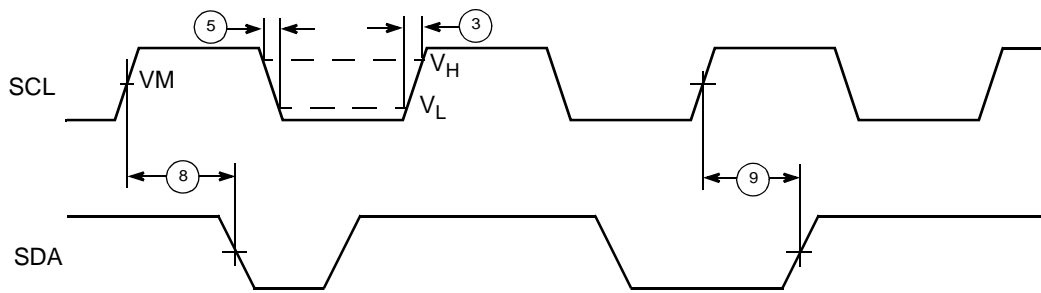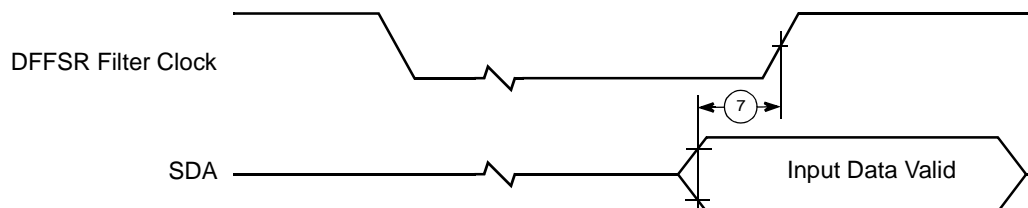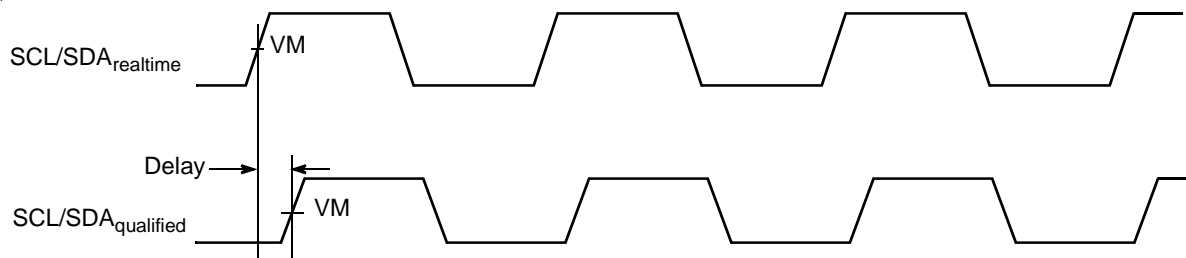

Figure 14. I²C Timing Diagram I

Figure 15. I^{2}C Timing Diagram II

Note: DFFSR filter clock is the SDRAM_CLK clock times DFFSR value.

Figure 16. I^{2}C Timing Diagram III

Note: The delay is the local memory clock times DFFSR times 2 plus 1 local memory clock.

Figure 17. I^{2}C Timing Diagram IV (Qualified Signal)

1.4.3.5   EPIC Serial Interrupt Mode AC Timing Specifications

Table 14 provides the EPIC serial interrupt mode AC timing specifications for the MPC8245 at recommended operating conditions (see Table 2) with GVdd = 3.3 V ±5% and LVdd = 3.3 V ±0.3 V.

Table 14. EPIC Serial Interrupt Mode AC Timing Specifications

Num	Characteristic	Min	Max	Unit	Notes
1	S_CLK Frequency	1/14 SDRAM_SYNC_IN	1/2 SDRAM_SYNC_IN	MHz	1
2	S_CLK Duty Cycle	40	60	%	—
3	S_CLK Output Valid Time	—	6	ns	—
4	Output Hold Time	0	—	ns	—
5	S_FRAME, S_RST Output Valid Time	—	1 *sys_logic_clk* period + 6	ns	2
6	S_INT Input Setup Time to S_CLK	1 *sys_logic_clk* period + 2	—	ns	2
7	S_INT Inputs Invalid (Hold Time) to S_CLK	—	0	ns	2

Notes:

1. See the *MPC8245 Integrated Processor User's Manual* for a description of the EPIC interrupt control register (EICR) describing S_CLK frequency programming.

2. S_RST, S_FRAME, and S_INT shown in Figure 18 and Figure 19, depict timing relationships to *sys_logic_clk* and S_CLK and do not describe functional relationships between S_RST, S_FRAME, and S_INT. See the *MPC8245 Integrated Processor User's Manual* for a complete description of the functional relationships between these signals.

3. The *sys_logic_clk* waveform is the clocking signal of the internal peripheral logic from the output of the peripheral logic PLL; *sys_logic_clk* is the same as SDRAM_SYNC_IN when the SDRAM_SYNC_OUT to SDRAM_SYNC_IN feedback loop is implemented and the DLL is locked. See the *MPC8245 Integrated Processor User's Manual* for a complete clocking description.
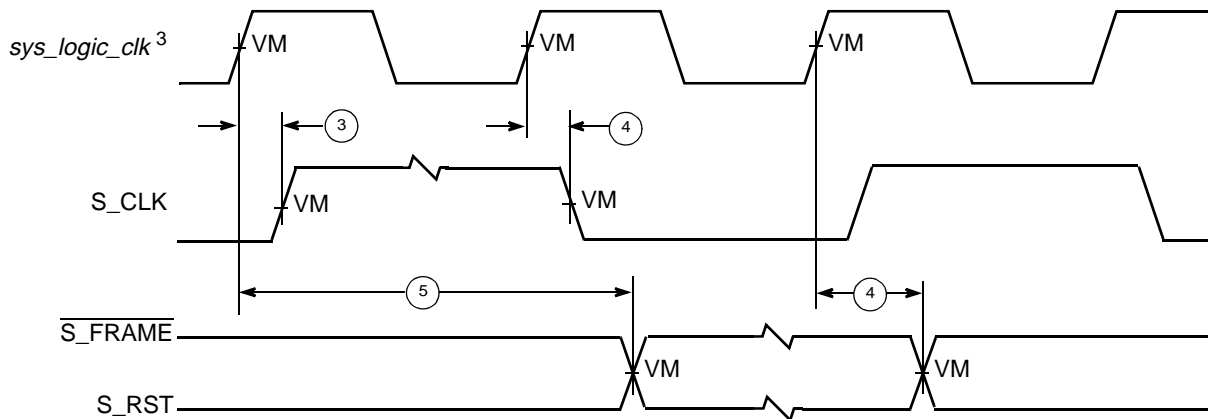

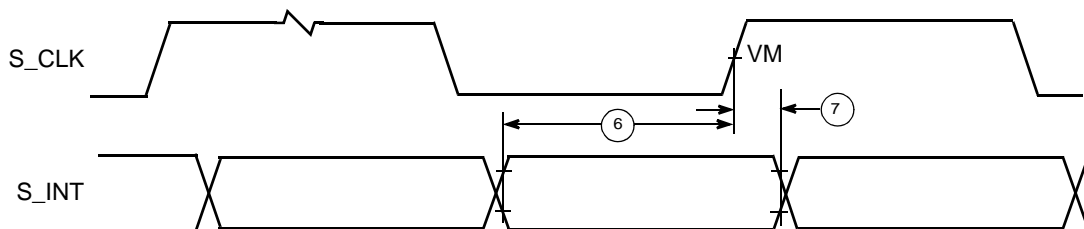**Figure 18. EPIC Serial Interrupt Mode Output Timing Diagram**

Figure 19. EPIC Serial Interrupt Mode Input Timing Diagram

## 1.4.3.6 IEEE 1149.1 (JTAG) AC Timing Specifications

Table 15 provides the JTAG AC timing specifications for the MPC8245 while in the JTAG operating mode at recommended operating conditions (see Table 2) with LVdd = 3.3 V ± 0.3 V. Timings are independent of the system clock (PCI_SYNC_IN).

**Table 15. JTAG AC Timing Specification (Independent of PCI_SYNC_IN)**

Num	Characteristic	Min	Max	Unit	Notes
	TCK Frequency of Operation	0	25	MHz	
1	TCK Cycle Time	40	—	ns	
2	TCK Clock Pulse Width Measured at 1.5 V	20	—	ns	
3	TCK Rise and Fall Times	0	3	ns	
4	$\overline{\text{TRST}}$ Setup Time to TCK Falling Edge	10	—	ns	1
5	$\overline{\text{TRST}}$ Assert Time	10	—	ns	
6	Input Data Setup Time	5	—	ns	2
7	Input Data Hold Time	15	—	ns	2
8	TCK to Output Data Valid	0	30	ns	3
9	TCK to Output High Impedance	0	30	ns	3
10	TMS, TDI Data Setup Time	5	—	ns	
11	TMS, TDI Data Hold Time	15	—	ns	
12	TCK to TDO Data Valid	0	15	ns	
13	TCK to TDO High Impedance	0	15	ns	

Notes:
1. $\overline{\text{TRST}}$ is an asynchronous signal. The setup time is for test purposes only.
2. Nontest (other than TDI and TMS) signal input timing with respect to TCK.
3. Nontest (other than TDO) signal output timing with respect to TCK.

VM = Midpoint Voltage
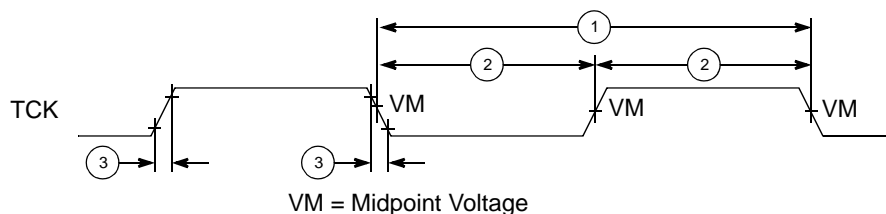
Figure 20. JTAG Clock Input Timing Diagram
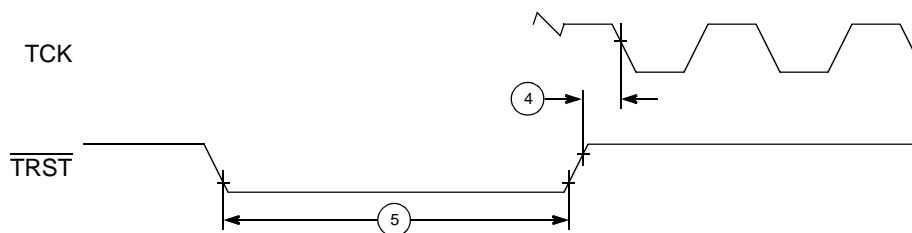
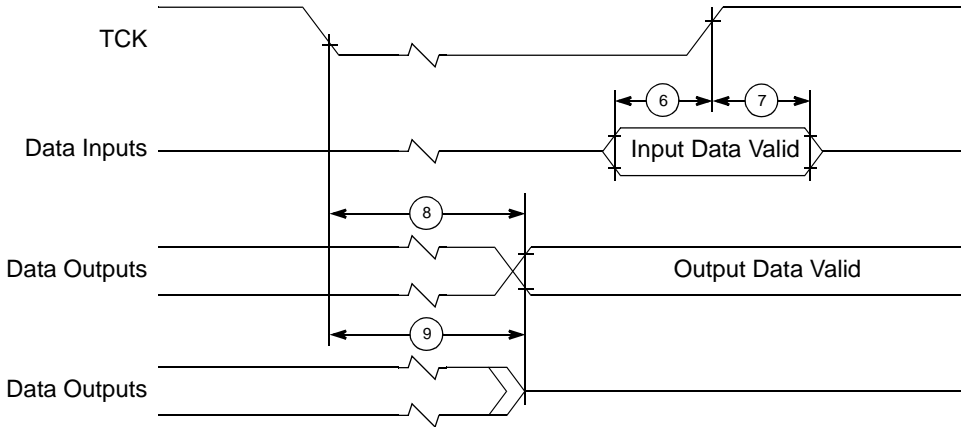**Figure 21. JTAG $\overline{\text{TRST}}$ Timing Diagram**

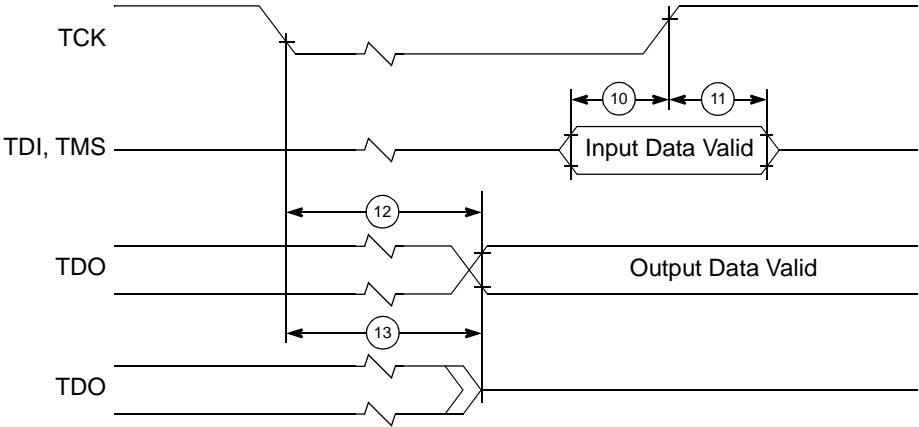**Figure 22. JTAG Boundary Scan Timing Diagram**

Figure 23. Test Access Port Timing Diagram

1.5 Package Description

This section details package parameters, pin assignments, and dimensions.

1.5.1 Package Parameters for the MPC8245

The MPC8245 uses a 35 mm × 35 mm, cavity up, 352-pin plastic ball grid array (PBGA) package. The package parameters are as follows.

Package Outline	35 mm × 35 mm
Interconnects	352
Pitch	1.27mm
Solder Balls	62Sn/36Pb/2Ag
Solder Ball Diameter	0.75 mm
Maximum Module Height	1.65 mm
Co-Planarity Specification	0.15 mm
Maximum Force	6.0 lbs. total, uniformly distributed over package (8 grams/ball)

1.5.2 Pin Assignments and Package Dimensions

Figure 24 shows the top surface, side profile, and pinout of the MPC8245, 352 PBGA package.

Top View

	MIN	MAX
A	34.8	35.2
B	34.8	35.2
C	1.45	1.65
D	.60	.90
G	1.27 BASIC	
H	.85	.95
K	31.75 BASIC	
L	.50	.70

Bottom View

352X ∅ D

Notes:

1. Drawing not to scale.
2. All measurements are in millimeters (mm).
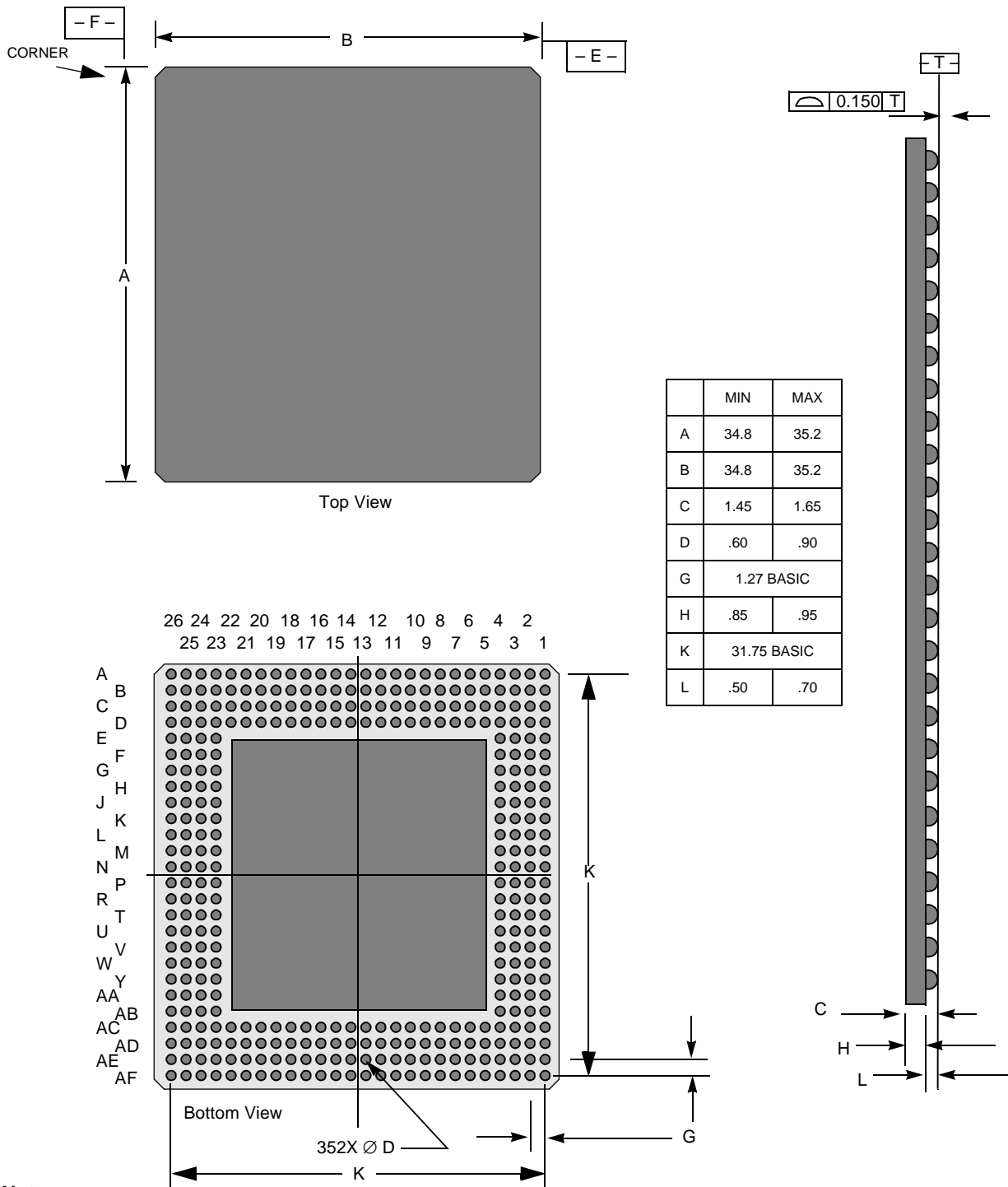
Figure 24. MPC8245 Package Dimensions and Pinout Assignments

1.5.3   Pinout Listings

Table 16 provides the pinout listing for the MPC8245, 352 TBGA package.

Table 16. MPC8245 Pinout Listing

Name	Pin Number	Type	Power Supply	Output Driver Type	Notes
PCI Interface Signals					
C/BE[3:0]	P25 K23 F23 A25	I/O	OVdd	DRV_PCI	6, 15
DEVSEL	H26	I/O3	OVdd	DRV_PCI	8, 15
FRAME	J24	I/O	OVdd	DRV_PCI	8, 15
IRDY	K25	I/O	OVdd	DRV_PCI	8, 15
LOCK	J26	Input	OVdd	—	8
AD[31:0]	V25 U25 U26 U24 U23 T25 T26 R25 R26 N26 N25 N23 M26 M25 L25 L26 F24 E26 E25 E23 D26 D25 C26 A26 B26 A24 B24 D19 B23 B22 D22 C22	I/O3	OVdd	DRV_PCI	6, 15
PAR	G25	I/O	OVdd	DRV_PCI	15
GNT[3:0]	W25 W24 W23 V26	Output	OVdd	DRV_PCI	6, 15
GNT4/DA5	W26	Output	OVdd	DRV_PCI	7, 15, 14
REQ[3:0]	Y25 AA26 AA25 AB26	Input	OVdd	—	6, 12
REQ4/DA4	Y26	I/O	OVdd	—	12, 14
PERR	G26	I/O	OVdd	DRV_PCI	8, 15, 18
SERR	F26	I/O	OVdd	DRV_PCI	8, 15, 16
STOP	H25	I/O	OVdd	DRV_PCI	8, 15
TRDY	K26	I/O	OVdd	DRV_PCI	8, 15
INTA	AC26	Output	OVdd	DRV_PCI	15, 16
IDSEL	P26	Input	OVdd	—	
Memory Interface Signals					
MDL[0:31]	AD17 AE17 AE15 AF15 AC14 AE13 AF13 AF12 AF11 AF10 AF9 AD8 AF8 AF7 AF6 AE5 B1 A1 A3 A4 A5 A6 A7 D7 A8 B8 A10 D10 A12 B11 B12 A14	I/O	GVdd	DRV_STD_MEM	5, 6

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Number	Type	Power Supply	Output Driver Type	Notes
MDH[0:31]	AC17 AF16 AE16 AE14 AF14 AC13 AE12 AE11 AE10 AE9 AE8 AC7 AE7 AE6 AF5 AC5 E4 A2 B3 D4 B4 B5 D6 C6 B7 C9 A9 B10 A11 A13 B13 A15	I/O	GVdd	DRV_STD_MEM	6
DQM[0:7]	AB1 AB2 K3 K2 AC1 AC2 K1 J1	Output	GVdd	DRV_MEM_CTRL	6
C̅S̅[0:7]	Y4 AA3 AA4 AC4 M2 L2 M1 L1	Output	GVdd	DRV_MEM_CTRL	6
FOE	H1	I/O	GVdd	DRV_MEM_CTRL	3, 4
RCS0	N4	Output	GVdd	DRV_MEM_CTRL	3, 4
RCS1	N2	Output	GVdd	DRV_MEM_CTRL	
R̅C̅S̅2̅/TRIG_IN	AF20	I/O	OVdd	—	10, 14
R̅C̅S̅3̅/TRIG_OUT	AC18	Output	GVdd	DRV_MEM_CTRL	14
SDMA[1:0]	W1 W2	I/O	GVdd	DRV_MEM_CTRL	3, 4, 6
SDMA[11:2]	N1 R1 R2 T1 T2 U4 U2 U1 V1 V3	Output	GVdd	DRV_MEM_CTRL	6
DRDY	B20	Input	OVdd	—	9, 14
SDMA12/S̅R̅E̅S̅E̅T̅	B16	I/O	GVdd	DRV_MEM_CTRL	10, 14
SDMA13/TBEN	B14	I/O	GVdd	DRV_MEM_CTRL	10, 14
SDMA14/ CHKSTOP_IN	D14	I/O	GVdd	DRV_MEM_CTRL	10, 14
SDBA1	P1	Output	GVdd	DRV_MEM_CTRL	
SDBA0	P2	Output	GVdd	DRV_MEM_CTRL	
PAR[0:7]	AF3 AE3 G4 E2 AE4 AF4 D2 C2	I/O	GVdd	DRV_STD_MEM	6
SDRAS	AD1	Output	GVdd	DRV_MEM_CTRL	3
SDCAS	AD2	Output	GVdd	DRV_MEM_CTRL	3
CKE	H2	Output	GVdd	DRV_MEM_CTRL	3, 4
WE	AA1	Output	GVdd	DRV_MEM_CTRL	
AS	Y1	Output	GVdd	DRV_MEM_CTRL	3, 4
EPIC Control Signals					
IRQ0/S_INT	C19	Input	OVdd	—	
IRQ1/S_CLK	B21	I/O	OVdd	DRV_PCI	
IRQ2/S_RST	AC22	I/O	OVdd	DRV_PCI	

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Number	Type	Power Supply	Output Driver Type	Notes
IRQ3/$\overline{\text{S\_FRAME}}$	AE24	I/O	OVdd	DRV_PCI	
IRQ4/$\overline{\text{L\_INT}}$	A23	I/O	OVdd	DRV_PCI	
I^{2}C Control Signals					
SDA	AE20	I/O	OVdd	DRV_STD_MEM	10, 16
SCL	AF21	I/O	OVdd	DRV_STD_MEM	10, 16
DUART Control Signals					
SOUT1/PCI_CLK0	AC25	Output	GVdd	DRV_PCI_CLK	13, 14
SIN1/PCI_CLK1	AB25	I/O	GVdd	DRV_PCI_CLK	13, 14
SOUT2/$\overline{\text{RTS1}}$/ PCI_CLK2	AE26	Output	GVdd	DRV_PCI_CLK	13, 14
SIN2/$\overline{\text{CTS1}}$/ PCI_CLK3	AF25	I/O	GVdd	DRV_PCI_CLK	13, 14
Clock-Out Signals					
PCI_CLK0/SOUT1	AC25	Output	GVdd	DRV_PCI_CLK	13, 14
PCI_CLK1/SIN1	AB25	I/O	GVdd	DRV_PCI_CLK	13, 14
PCI_CLK2/$\overline{\text{RTS1}}$/ SOUT2	AE26	Output	GVdd	DRV_PCI_CLK	13, 14
PCI_CLK3/$\overline{\text{CTS1}}$/ SIN2	AF25	I/O	GVdd	DRV_PCI_CLK	13, 14
PCI_CLK4/DA3	AF26	Output	GVdd	DRV_PCI_CLK	13, 14
PCI_SYNC_OUT	AD25	Output	GVdd	DRV_PCI_CLK	
PCI_SYNC_IN	AB23	Input	GVdd	—	
SDRAM_CLK [0:3]	D1 G1 G2 E1	Output	GVdd	DRV_MEM_CTRL or DRV_MEM_CLK	6, 21
SDRAM_SYNC_OUT	C1	Output	GVdd	DRV_MEM_CTRL or DRV_MEM_CLK	21
SDRAM_SYNC_IN	H3	Input	GVdd	—	
CKO/DA1	B15	Output	OVdd	DRV_STD_MEM	14
OSC_IN	AD21	Input	OVdd	—	19
Miscellaneous Signals					
HRST_CTRL	A20	Input	OVdd	—	
HRST_CPU	A19	Input	OVdd	—	
MCP	A17	Output	OVdd	DRV_STD_MEM	3, 4, 17

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Number	Type	Power Supply	Output Driver Type	Notes
NMI	D16	Input	OVdd	—	
SMI	A18	Input	OVdd	—	10
SRESET/SDMA12	B16	I/O	GVdd	DRV_MEM_CTRL	10, 14
TBEN/SDMA13	B14	I/O	GVdd	DRV_MEM_CTRL	10, 14
QACK/DA0	F2	Output	OVdd	DRV_STD_MEM	3, 4, 14
CHKSTOP_IN/ SDMA14	D14	I/O	GVdd	DRV_MEM_CTRL	10, 14
TRIG_IN/RCS2	AF20	I/O	OVdd	—	10, 14
TRIG_OUT/RCS3	AC18	Output	GVdd	DRV_MEM_CTRL	14
MAA[0:2]	AF2 AF1 AE1	Output	GVdd	DRV_STD_MEM	3, 4, 6
MIV	A16	Output	OVdd	—	24
PMAA[0:1]	AD18 AF18	Output	OVdd	DRV_STD_MEM	3, 4, 6, 15
PMAA[2]	AE19	Output	OVdd	DRV_STD_MEM	4, 6, 15
Test/Configuration Signals					
PLL_CFG[0:4]/ DA[10:6]	A22 B19 A21 B18 B17	I/O	OVdd	DRV_STD_MEM	6, 14, 20
TEST0	AD22	Input	OVdd	—	1, 9
DRDY	B20	Input	OVdd	—	9, 10, 14
RTC	Y2	Input	GVdd	—	11
TCK	AF22	Input	OVdd	—	9, 12
TDI	AF23	Input	OVdd	—	9, 12
TDO	AC21	Output	OVdd	—	24
TMS	AE22	Input	OVdd	—	9, 12
TRST	AE23	Input	OVdd	—	9, 12
Power and Ground Signals					
GND	AA2 AA23 AC12 AC15 AC24 AC3 AC6 AC9 AD11 AD14 AD16 AD19 AD23 AD4 AE18 AE2 AE21 AE25 B2 B25 B6 B9 C11 C13 C16 C23 C4 C8 D12 D15 D18 D21 D24 D3 F25 F4 H24 J25 J4 L24 L3 M23 M4 N24 P3 R23 R4 T24 T3 V2 V23 W3	Ground	—	—	

Package Description

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Table 16. MPC8245 Pinout Listing (continued)

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Name	Pin Number	Type	Power Supply	Output Driver Type	Notes
LVdd	AC20 AC23 D20 D23 G23 P23 Y23	Reference Voltage 3.3 V, 5.0 V	LVdd	—	
GVdd	AB3 AB4 AC10 AC11 AC8 AD10 AD13 AD15 AD3 AD5 AD7 C10 C12 C3 C5 C7 D13 D5 D9 E3 G3 H4 K4 L4 N3 P4 R3 U3 V4 Y3	Power for Memory Drivers 3.3 V	GVdd	—	
OVdd	AB24 AD20 AD24 C14 C20 C24 E24 G24 J23 K24 M24 P24 T23 Y24	PCI / Stnd 3.3 V	OVdd	—	
Vdd	AA24 AC16 AC19 AD12 AD6 AD9 C15 C18 C21 D11 D8 F3 H23 J3 L23 M3 R24 T4 V24 W4	Power for Core 1.8/2.0 V	Vdd	—	22
No Connect	D17	—	—	—	23
AVdd	C17	Power for PLL (CPU Core Logic) 1.8/2.0 V	AVdd	—	22
AVdd2	AF24	Power for PLL (Peripheral Logic) 1.8/ 2.0 V	AVdd2	—	22
Debug/Manufacturing Pins					
DA0/$\overline{\text{QACK}}$	F2	Output	OVdd	DRV_STD_MEM	3, 4, 14
DA1/CKO	B15	Output	OVdd	DRV_STD_MEM	14
DA2	C25	Output	OVdd	DRV_PCI	2
DA3/PCI_CLK4	AF26	Output	GVdd	DRV_PCI_CLK	14
DA4/$\overline{\text{REQ4}}$	Y26	I/O	OVdd	—	12, 14
DA5/$\overline{\text{GNT4}}$	W26	Output	OVdd	DRV_PCI	7, 15, 14
DA[10:6]/ PLL_CFG[0:4]	A22 B19 A21 B18 B17	I/O	OVdd	DRV_STD_MEM	6, 14, 20
DA[11]	AD26	Output	OVdd	DRV_PCI	2
DA[12:13]	AF17 AF19	Output	OVdd	DRV_STD_MEM	2, 6

Table 16. MPC8245 Pinout Listing (continued)

Name	Pin Number	Type	Power Supply	Output Driver Type	Notes
DA[14:15]	F1 J2	Output	GVdd	DRV_MEM_CTRL	2, 6

Notes:

1. Place a pull-up resistor of 120 Ω or less on the $\overline{TEST0}$ pin.
2. Treat these pins as no connects (NC) unless using debug address functionality.
3. This pin has an internal pull-up resistor which is enabled only when the MPC8245 is in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a logic 1 is read into configuration bits during reset.
4. This pin is a reset configuration pin.
5. DL[0] is a reset configuration pin and has an internal pull-up resistor which is enabled only when the MPC8245 is in the reset state. The value of the internal pull-up resistor is not guaranteed, but is sufficient to ensure that a logic 1 is read into configuration bits during reset.
6. Multi-pin signals such as AD[31:0] or MDL[0:31] have their physical package pin numbers listed in order, corresponding to the signal names. Example: AD0 is on pin C22, AD1 is on pin D22, ..., AD31 is on pin V25.
7. $\overline{GNT4}$ is a reset configuration pin and has an internal pull-up resistor which is enabled only when the MPC8245 is in the reset state.
8. Recommend a weak pull-up resistor (2 kΩ–10 kΩ) be placed on this PCI control pin to LVdd.
9. V_{IH} and V_{IL} for these signals are the same as the PCI V_{IH} and V_{IL} entries in Table 3.
10. Recommend a weak pull-up resistor (2 kΩ–10 kΩ) be placed on this pin to OVdd.
11. Recommend a weak pull-up resistor (2 kΩ–10 kΩ) be placed on this pin to GVdd.
12. This pin has an internal pull-up resistor which is enabled at all times. The value of the internal pull-up resistor is not guaranteed, but is sufficient to prevent unused inputs from floating.
13. External PCI clocking source or fan-out buffer may be required for system if using the MPC8245 DUART functionality since PCI_CLK[0:3] are not available in DUART mode. Only PCI_CLK4 is available in DUART mode.
14. This pin is a multiplexed signal and appears more than once in this table.
15. This pin is affected by programmable PCI_HOLD_DEL parameter.
16. This pin is an open drain signal.
17. This pin can be programmed to be driven (default) or can be programmed (in PMCR2) to be open drain.
18. This pin is a sustained three-state pin as defined by the *PCI Local Bus Specification.*
19. OSC_IN utilizes the 3.3 V PCI interface driver which is 5 V tolerant, see Table 2 for details.
20. PLL_CFG[0:4] signals are sampled a few clocks after the negation of $\overline{HRST\_CPU}$ and $\overline{HRST\_CTRL}$.
21. SDRAM_CLK[0:3] and SDRAM_SYNC_OUT signals use DRV_MEM_CTRL for chip Rev 1.1 (A). These signals use DRV_MEM_CLK for chip Rev 1.2 (B).
22. The 266 and 300 MHz part offerings can be ran at a source voltage of 1.8 ± 100 mV or 2.0 ± 100 mV. Note that source voltage should be 2.0 ± 100 mV for 333- and 350-MHz parts.
23. This pin was formally LAVDD on the MPC8240. It is a no connect on the MPC8245. This should not pose a problem when replacing an MPC8240 with an MPC8245.
24. The driver capability of this pin is hardwired to 40 Ω and cannot be changed.

1.6 PLL Configuration

The internal PLLs of the MPC8245 are configured by the PLL_CFG[0:4] signals. For a given PCI_SYNC_IN (PCI bus) frequency, the PLL configuration signals set both the peripheral logic/memory bus PLL (VCO) frequency of operation for the PCI-to-memory frequency multiplying and the MPC603e CPU PLL (VCO) frequency of operation for memory-to-CPU frequency multiplying. The PLL configurations for the MPC8245 is shown in Table 17 and Table 18.

Table 17. PLL Configurations (266- and 300-MHz Parts)

Ref	PLL_CFG [0:4][10,13]	266 MHz Part [9]			300 MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range[1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range[1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO)	Mem to CPU (CPU VCO)
0	00000[12]	25 - 35[5]	75 - 105	188 - 263	25 - 40[5]	75 - 120	188 - 300	3 (2)	2.5 (2)
1	00001[12]	25 - 29[5]	75 - 88	225 - 264	25 - 33[5]	75 - 99	225 - 297	3 (2)	3 (2)
2	00010[11]	50[18] - 59[5]	50 - 59	225 - 266	50[18] - 66[1]	50 - 66	225 - 297	1 (4)	4.5 (2)
3	00011[11,14]	50[4] - 66[1]	50 - 66	100 - 133	50[4] - 66[1]	50 - 66	100 - 133	1 (Bypass)	2 (4)
4	00100[12]	25 - 46[4]	50 - 92	100 - 184	25 - 46[4]	50 - 92	100 - 184	2 (4)	2 (4)
5	00101	Reserved			Reserved			Note 20	
6	00110[15]	Bypass			Bypass			Bypass	
7	00111[14]	60[6] - 66[1]	60 - 66	180 - 198	60[6] - 66[1]	60 - 66	180 - 198	1 (Bypass)	3 (2)
8	01000[12]	60[6] - 66[1]	60 - 66	180 - 198	60[6] - 66[1]	60 - 66	180 - 198	1 (4)	3 (2)
9	01001[19]	45[6] - 66[1]	90 - 132	180 - 264	45[6] - 66[1]	90 - 132	180 - 264	2 (2)	2 (2)
A	01010[12]	25 - 29[5]	50 - 58	225 - 261	25 - 33[5]	50 - 66	225 - 297	2 (4)	4.5 (2)
B	01011[19]	45[3] - 59[5]	68 - 88	204 - 264	45[3] - 66[1]	68 - 99	204 - 297	1.5 (2)	3 (2)
C	01100[12]	36[6] - 46[4]	72 - 92	180 - 230	36[6] - 46[4]	72 - 92	180 - 230	2 (4)	2.5 (2)
D	01101[19]	45[3] - 50[5]	68 - 75	238 - 263	45[3] - 57[5]	68 - 85	238 - 298	1.5 (2)	3.5 (2)
E	01110[12]	30[6] - 44[5]	60 - 88	180 - 264	30[6] - 46[4]	60 - 92	180 - 276	2 (4)	3 (2)
F	01111[19]	25[5]	75	263	25 - 28[5]	75 - 85	263 - 298	3 (2)	3.5 (2)
10	10000[12]	30[6] - 44[2,5]	60 - 132	180 - 264	30[6] - 44[2]	60 - 132	180 - 264	3 (2)	2 (2)
11	10001[19]	25 - 26[5]	100 - 106	250 - 266	25 - 29[2]	100 - 116	250 - 290	4 (2)	2.5 (2)
12	10010[12]	60[6] - 66[1]	90 - 99	180 - 198	60[6] - 66[1]	90 - 99	180 - 198	1.5 (2)	2 (2)
13	10011[19]	Not Available			25[2]	100	300	4 (2)	3 (2)
14	10100[12]	26[6] - 38[5]	52 - 76	182 - 266	26[6] - 42[5]	52 - 84	182 - 294	2 (4)	3.5 (2)
15	10101[19]	Not Available			27[3] - 30[5]	68 - 75	272 - 300	2.5 (2)	4 (2)
16	10110[12]	25 - 33[5]	50 - 66	200 - 264	25 - 37[5]	50 - 74	200 - 296	2 (4)	4 (2)
17	10111[19]	25 - 33[5]	100 - 132	200 - 264	25 - 33[2]	100 - 132	200 - 264	4 (2)	2 (2)
18	11000[12]	27[3] - 35[5]	68 - 88	204 - 264	27[3] - 40[5]	68 - 100	204 - 300	2.5 (2)	3 (2)
19	11001[19]	36[6] - 53[5]	72 - 106	180 - 265	36[6] - 59[2]	72 - 118	180 - 295	2 (2)	2.5 (2)
1A	11010[12]	50[18] - 66[1]	50 - 66	200 - 264	50[18] - 66[1]	50 - 66	200 - 264	1 (4)	4 (2)
1B	11011[19]	33[6] - 44[5]	66 - 88	198 - 264	33[6] - 50[5]	66 - 100	198 - 300	2 (2)	3 (2)
1C	11100[12]	44[6] - 59[5]	66 - 88	198 - 264	44[6] - 66[1]	66 - 99	198 - 297	1.5 (2)	3 (2)

Table 17. PLL Configurations (266- and 300-MHz Parts) (continued)

Ref	PLL_CFG [0:4][10,13]	266 MHz Part [9]			300 MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_ SYNC_IN) Range[1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_ SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO)	Mem to CPU (CPU VCO)
1D	11101[12]	48[6] - 66[1]	72 - 99	180 - 248	48[6] - 66[1]	72 - 99	180 - 248	1.5 (2)	2.5 (2)
1E	11110[8]	Not Usable			Not Usable			Off	Off
1F	11111[8]	Not Usable			Not Usable			Off	Off

Notes:
1. Limited by maximum PCI input frequency (66 MHz).
2. Limited by maximum system memory interface operating frequency (100 MHz @ 350 MHz CPU).
3. Limited by minimum memory VCO frequency (133 MHz).
4. Limited due to maximum memory VCO frequency (372 MHz).
5. Limited by maximum CPU operating frequency (266 MHz).
6. Limited by minimum CPU VCO frequency (360 MHz).
7. Limited by maximum CPU VCO frequency (800 MHz).
8. In clock off mode, no clocking occurs inside the MPC8245 regardless of the PCI_SYNC_IN input.
9. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
10. PLL_CFG[0:4] settings not listed (01011, 01101, 01111, 10001, 10011, 10101, 11001, and 11011) are reserved.
11. Multiplier ratios for this PLL_CFG[0:4] setting are different from the MPC8240 and are not backwards-compatible.
12. PCI_SYNC_IN range for this PLL_CFG[0:4] setting is different from the MPC8240 and may not be fully backwards-compatible.
13. Bits 7– 4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
14. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in PLL bypass mode.
15. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in dual PLL bypass mode.
16. Limited by maximum system memory interface operating frequency (133 MHz @ 266 MHz CPU).
17. Limited by minimum CPU operating frequency (100 MHz).
18. Limited by minimum memory bus frequency (50 MHz).
19. PCI_SYNC_IN range for this PLL_CFG[0:4] setting does not exist on the MPC8240 and may not be fully backwards-compatible.
20. No longer supported.

Table 18. PLL Configurations (333- and 350-MHz Parts)

Ref	PLL_CFG [0:4][10,13]	333 MHz Part [9]			350 MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO)	Mem to CPU (CPU VCO)
0	00000[12]	25 - 44[16]	75 - 132	188 - 330	25 - 44[16]	75 - 132	188 - 330	3 (2)	2.5 (2)
1	00001[12]	25 - 37[5]	75 - 111	225 - 333	25 - 38[5]	75 - 114	225 - 342	3 (2)	3 (2)
2	00010[11]	50[18] - 66[1]	50 - 66	225 - 297	50[18] - 66[1]	50 - 66	225 - 297	1 (4)	4.5 (2)
3	00011[11,14]	50[4] - 66[1]	50 - 66	100 - 133	50[4] - 66[1]	50 - 66	100 - 133	1 (Bypass)	2 (4)
4	00100[12]	25 - 46[4]	50 - 92	100 - 184	25 - 46[4]	50 - 92	100 - 184	2 (4)	2 (4)
5	00101	Reserved			Reserved			Note 20	
6	00110[15]	Bypass			Bypass			Bypass	
7	00111[14]	60[6] - 66[1]	60 - 66	180 - 198	60[6] - 66[1]	60 - 66	180 - 198	1 (Bypass)	3 (2)
8	01000[12]	60[6] - 66[1]	60 - 66	180 - 198	60[6] - 66[1]	60 - 66	180 - 198	1 (4)	3 (2)
9	01001[19]	45[6] - 66[1]	90 - 132	180 - 264	45[6] - 66[1]	90 - 132	180 - 264	2 (2)	2 (2)
A	01010[12]	25 - 37[5]	50 - 74	225 - 333	25 - 38[5]	50 - 76	225 - 342	2 (4)	4.5 (2)
B	01011[19]	45[3] - 66[1]	68 - 99	204 - 297	45[3] - 66[1]	68 - 99	204 - 297	1.5 (2)	3 (2)
C	01100[12]	36[6] - 46[4]	72 - 92	180 - 230	36[6] - 46[4]	72 - 92	180 - 230	2 (4)	2.5 (2)
D	01101[19]	45[3] - 63[5]	68 - 95	238 - 333	45[3] - 66[1]	68 - 99	238 - 347	1.5 (2)	3.5 (2)
E	01110[12]	30[6] - 46[4]	60 - 92	180 - 276	30[6] - 46[4]	60 - 92	180 - 276	2 (4)	3 (2)
F	01111[19]	25 - 31[5]	75 - 93	263 - 326	25 - 33[5]	75 - 99	263 - 347	3 (2)	3.5 (2)
10	10000[12]	30[6] - 44[2]	60 - 132	180 - 264	30[6] - 44[2]	60 - 132	180 - 264	3 (2)	2 (2)
11	10001[19]	25 - 33[2]	100 - 132	250 - 330	25 - 33[2]	100 - 132	250 - 330	4 (2)	2.5 (2)
12	10010[12]	60[6] - 66[1]	90 - 99	180 - 198	60[6] - 66[1]	90 - 99	180 - 198	1.5 (2)	2 (2)
13	10011[19]	25 - 27[5]	100 - 108	300 - 324	25 - 29[5]	100 - 116	300 - 348	4 (2)	3 (2)
14	10100[12]	26[6] - 47[4]	52 - 94	182 - 329	26[6] - 47[4]	52 - 94	182 - 329	2 (4)	3.5 (2)
15	10101[19]	27[3] - 33[5]	68 - 83	272 - 332	27[3] - 34[5]	68 - 85	272 - 340	2.5 (2)	4 (2)
16	10110[12]	25 - 41[5]	50 - 82	200 - 328	25 - 43[5]	50 - 86	200 - 344	2 (4)	4 (2)
17	10111[19]	25 - 33[2]	100 - 132	200 - 264	25 - 33[2]	100 - 132	200 - 264	4 (2)	2 (2)
18	11000[12]	27[3] - 44[5]	68 - 110	204 - 330	27[3] - 46[5]	68 - 115	204 - 345	2.5 (2)	3 (2)
19	11001[19]	36[6] - 66[1]	72 - 132	180 - 330	36[6] - 66[1]	72 - 132	180 - 330	2 (2)	2.5 (2)
1A	11010[12]	50[18] - 66[1]	50 - 66	200 - 264	50[18] - 66[1]	50 - 66	200 - 264	1 (4)	4 (2)
1B	11011[19]	33[6] - 55[5]	66 - 110	198 - 330	33[6] - 58[5]	66 - 116	198 - 348	2 (2)	3 (2)

Table 18. PLL Configurations (333- and 350-MHz Parts) (continued)

Ref	PLL_ CFG [0:4][10,13]	333 MHz Part [9]			350 MHz Part [9]			Multipliers	
		PCI Clock Input (PCI_ SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI Clock Input (PCI_ SYNC_IN) Range [1] (MHz)	Periph Logic/ Mem Bus Clock Range (MHz)	CPU Clock Range (MHz)	PCI to Mem (Mem VCO)	Mem to CPU (CPU VCO)
1C	11100[12]	44[6] - 66[1]	66 - 99	198 - 297	44[6] - 66[1]	66 - 99	198 - 297	1.5 (2)	3 (2)
1D	11101[12]	48[6] - 66[1]	72 - 99	180 - 248	48[6] - 66[1]	72 - 99	180 - 248	1.5 (2)	2.5(2)
1E	11110[8]	Not Usable			Not Usable			Off	Off
1F	11111[8]	Not Usable			Not Usable			Off	Off

Notes:
1. Limited by maximum PCI input frequency (66 MHz).
2. Limited by maximum system memory interface operating frequency (100 MHz @ 350 MHz CPU).
3. Limited by minimum memory VCO frequency (133 MHz).
4. Limited due to maximum memory VCO frequency (372 MHz).
5. Limited by maximum CPU operating frequency (266 MHz).
6. Limited by minimum CPU VCO frequency (360 MHz).
7. Limited by maximum CPU VCO frequency (800 MHz).
8. In clock off mode, no clocking occurs inside the MPC8245 regardless of the PCI_SYNC_IN input.
9. Range values are shown rounded down to the nearest whole number (decimal place accuracy removed) for clarity.
10. PLL_CFG[0:4] settings not listed (01011, 01101, 01111, 10001, 10011, 10101, 11001, and 11011) are reserved.
11. Multiplier ratios for this PLL_CFG[0:4] setting are different from the MPC8240 and are not backwards-compatible.
12. PCI_SYNC_IN range for this PLL_CFG[0:4] setting is different from the MPC8240 and may not be fully backwards-compatible.
13. Bits 7–4 of register offset <0xE2> contain the PLL_CFG[0:4] setting value.
14. In PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal processor directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI:Mem) mode operation. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in PLL bypass mode.
15. In dual PLL bypass mode, the PCI_SYNC_IN input signal clocks the internal peripheral logic directly, the peripheral logic PLL is disabled, and the bus mode is set for 1:1 (PCI_SYNC_IN:Mem) mode operation. In this mode, the OSC_IN input signal clocks the internal processor directly in 1:1 (OSC_IN:CPU) mode operation, and the processor PLL is disabled. The PCI_SYNC_IN and OSC_IN input clocks must be externally synchronized. This mode is intended for hardware modeling support. The AC timing specifications given in this document do not apply in dual PLL bypass mode.
16. Limited by maximum system memory interface operating frequency (133 MHz @ 333 MHz CPU).
17. Limited by minimum CPU operating frequency (100 MHz).
18. Limited by minimum memory bus frequency (50 MHz).
19. PCI_SYNC_IN range for this PLL_CFG[0:4] setting does not exist on the MPC8240 and may not be fully backwards-compatible.
20. No longer supported.

1.7   System Design Information

This section provides electrical and thermal design recommendations for successful application of the MPC8245.

1.7.1   PLL Power Supply Filtering

The AVdd and AVdd2 power signals are provided on the MPC8245 to provide power to the peripheral logic/memory bus PLL and the MPC603e processor PLL. To ensure stability of the internal clocks, the power supplied to the AVdd and AVdd2 input signals should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLLs. Two separate circuits similar to the one shown in Figure 25 using surface mount capacitors with minimum effective series inductance (ESL) is recommended for AVdd and AVdd2 power signal pins. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over using multiple values.

The circuits should be placed as close as possible to the respective input signal pins to minimize noise coupled from nearby circuits. Routing directly as possible from the capacitors to the input signal pins with minimal inductance of vias is important.
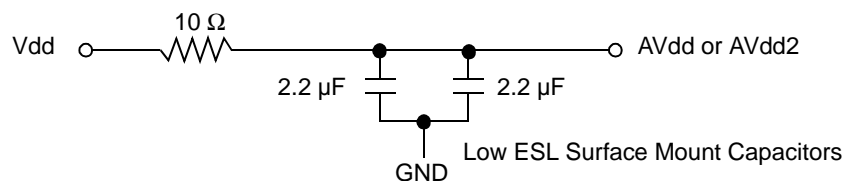
Figure 25. PLL Power Supply Filter Circuit

1.7.2   Power Supply Sizing

The power consumption numbers provided in Table 5 do not reflect power from the OVdd and GVdd power supplies which are non-negligible for the MPC8245. In typical application measurements, the OVdd power ranged from 200 to 500 mW and the GVdd power ranged from 300 to 600 mW. The ranges' low-end power numbers were results of the MPC8245 performing cache resident integer operations at the slowest frequency combination of 33:66:200 (PCI:Mem:CPU) MHz. The OVdd high end range's value resulted from the MPC8245 operating at the fastest frequency combination of 66:100:350 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros to PCI memory. The GVdd high-end range's value resulted from the MPC8245 operating at the fastest frequency combination of 66:100:350 (PCI:Mem:CPU) MHz and performing continuous flushes of cache lines with alternating ones and zeros on 64-bit boundaries to local memory.

1.7.3   Decoupling Recommendations

Due to its dynamic power management feature, the large address and data buses, and its high operating frequencies, the MPC8245 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8245 system, and the MPC8245 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each Vdd, OVdd, GVdd, and LVdd pin of the MPC8245. It is also recommended that these decoupling capacitors receive their power from separate Vdd, OVdd, GVdd, and GND power planes in the PCB, utilizing short

traces to minimize inductance. These capacitors should have a value of 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603, oriented such that connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the Vdd, OVdd, GVdd, and LVdd planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100–330 µF (AVX TPS tantalum or Sanyo OSCON).

1.7.4   Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active-low inputs should be tied to OVdd. Unused active-high inputs should be connected to GND. All NC (no connect) signals must remain unconnected.

Power and ground connections must be made to all external Vdd, OVdd, GVdd, LVdd, and GND pins of the MPC8245.

The PCI_SYNC_OUT signal is intended to be routed halfway out to the PCI devices and then returned to the PCI_SYNC_IN input of the MPC8245.

The SDRAM_SYNC_OUT signal is intended to be routed halfway out to the SDRAM devices and then returned to the SDRAM_SYNC_IN input of the MPC8245. The trace length may be used to skew or adjust the timing window as needed. See Motorola application notes AN1849/D and AN2164/D for more information on this topic. Note that there is an SDRAM_SYNC_IN to PCI_SYNC_IN time requirement. (See Table 9.)

1.7.5   Pull-Up/Pull-Down Resistor Requirements

The data bus input receivers are normally turned off when no read operation is in progress; therefore, they do not require pull-up resistors on the bus. The data bus signals are: MDH[0:31], MDL[0:31], and PAR[0:7].

If the 32-bit data bus mode is selected, the input receivers of the unused data and parity bits (MDL[0:31] and PAR[4:7]) will be disabled, and their outputs will drive logic zeros when they would otherwise normally be driven. For this mode, these pins do not require pull-up resistors and should be left unconnected by the system to minimize possible output switching.

The $\overline{\text{TEST0}}$ pin requires a pull-up resistor of 120 Ω or less connected to OVdd.

It is recommended that RTC have weak pull-up resistors (2 kΩ–10 kΩ) connected to GVdd_OVdd.

It is recommended that the following signals be pulled up to OVdd with weak pull-up resistors (2 kΩ–10 kΩ): SDA, SCL, $\overline{\text{SMI}}$, $\overline{\text{SRESET}}$/SDMA12, TBEN/SDMA13, $\overline{\text{CHKSTOP\_IN}}$/SDMA14, TRIG_IN/$\overline{\text{RCS2}}$, and $\overline{\text{DRDY}}$

It is recommended that the following PCI control signals be pulled up to LVdd with weak pull-up resistors (2 kΩ–10 kΩ): $\overline{\text{DEVSEL}}$, $\overline{\text{FRAME}}$, $\overline{\text{IRDY}}$, $\overline{\text{LOCK}}$, $\overline{\text{PERR}}$, $\overline{\text{SERR}}$, $\overline{\text{STOP}}$, and $\overline{\text{TRDY}}$. The resistor values may need to be adjusted stronger to reduce induced noise on specific board designs.

The following pins have internal pull-up resistors enabled at all times: $\overline{\text{REQ}}$[3:0], $\overline{\text{REQ4}}$/DA4, TCK, TDI, TMS, and $\overline{\text{TRST}}$. See Table 16 for more information.

The following pins have internal pull-up resistors enabled only while device is in the reset state: $\overline{\text{GNT4}}$/DA5, MDL0, $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, MAA[0:2], PMAA[0:2], and $\overline{\text{QACK}}$/DA0. See Table 16 for more information.

The following pins are reset configuration pins: $\overline{\text{GNT4}}$/DA5, MDL[0], $\overline{\text{FOE}}$, $\overline{\text{RCS0}}$, CKE, $\overline{\text{AS}}$, $\overline{\text{MCP}}$, $\overline{\text{QACK}}$/DA0, MAA[0:2], PMAA[0:2], SDMA[1:0], MDH[16:31], and PLL_CFG[0:4]/DA[10:15]. These pins are sampled during reset to configure the device. The PLL_CFG[0:4] signals are sampled a few clocks after the negation of $\overline{\text{HRST\_CPU}}$ and $\overline{\text{HRST\_CTRL}}$.

Reset configuration pins should be tied to GND via 1-kΩ pull-down resistors to ensure a logic zero level is read into the configuration bits during reset if the default logic-one level is not desired.

Any other unused active low input pins should be tied to a logic-one level via weak pull-up resistors (2 kΩ–10 kΩ) to the appropriate power supply listed in Table 16. Unused active high input pins should be tied to GND via weak pull-down resistors (2 kΩ–10 kΩ).

1.7.6 PCI Reference Voltage—LVdd

The MPC8245 PCI reference voltage (LVdd) pins should be connected to 3.3 ± 0.3 V power supply if interfacing the MPC8245 into a 3.3-V PCI bus system. Similarly, the LVdd pins should be connected to 5.0 V $\pm 5\%$ power supply if interfacing the MPC8245 into a 5-V PCI bus system. For either reference voltage, the MPC8245 always performs 3.3-V signaling as described in the *PCI Local Bus Specification* (Rev. 2.2). The MPC8245 tolerates 5-V signals when interfaced into a 5-V PCI bus system.

1.7.7 MPC8245 Compatibility with MPC8240

The MPC8245 AC timing specifications are backwards-compatible with those of the MPC8240, except for the requirements of item 11 in Table 9. Timing adjustments are needed as specified for T_{OS} (SDRAM_SYNC_IN to *sys_logic_clk* offset) time requirements.

The MPC8245 does not support the SDRAM flow-through memory interface.

The nominal core Vdd power supply changes from 2.5 V on the MPC8240 to 1.8/2.0 V on the MPC8245. See Table 2 for details.

The MPC8245 PLL_CFG[0:4] setting 0x02 (0b00010) has a different 'PCI to Mem' and 'Mem to CPU' multiplier ratio than the same setting on the MPC8240, and thus, is not backwards-compatible. See Table 17 for details.

The MPC8245 PLL_CFG[0:4] settings 0x08 (0b01000), 0x0C (0b01100), 0x12 (0b10010), 0x18 (0b11000), 0x1C (0b11100), and 0x1D (0b11101) are capable of accepting a subset of the PCI_SYNC_IN input frequency range of that of the MPC8240, and thus, may not be fully backwards-compatible. See Table 17 for details.

There are two additional reset configuration signals on the MPC8245 which are not used as reset configuration signals on the MPC8240: SDMA0 and SDMA1.

The SDMA0 reset configuration pin selects between the MPC8245 DUART or the MPC8240 backwards compatible mode PCI_CLK[0:4] functionality on these multiplexed signals. The default state (logic 1) of SDMA0 selects the MPC8240 backwards compatible mode of PCI_CLK[0:4] functionality while a logic 0 state on the SDMA0 signal selects DUART functionality. Note if using the DUART mode, four of the five PCI clocks, PCI_CLK[0:3], are not available.

The SDMA1 reset configuration pin selects between MPC8245 extended ROM functionality or MPC8240 backwards-compatible functionality on the multiplexed signals: TBEN, $\overline{\text{CHKSTOP\_IN}}$, $\overline{\text{SRESET}}$, TRIG_IN, and TRIG_OUT. The default state (logic 1) of SDMA1 selects the MPC8240 backwards compatible mode functionality, while a logic 0 state on the SDMA1 signal selects extended ROM functionality. Note if using the extended ROM mode, TBEN, $\overline{\text{CHKSTOP\_IN}}$, $\overline{\text{SRESET}}$, TRIG_IN, and TRIG_OUT functionality are not available.

The driver names and capability of the pins for the MPC8245 and that of the MPC8240 vary slightly. Please refer to the Drive Capability table (for the ODCR register at 0x73) in the *MPC8240 Integrated Processor Hardware Specifications* and Table 4 for more details.

The programmable PCI output valid and output hold feature controlled by bits in the power management configuration register 2 (PMCR2) <0x72> has changed slightly in the MPC8245. For the MPC8240, three bits, PMCR2[6:4] = PCI_HOLD_DEL, are used to select one of eight possible PCI output timing configurations. PMCR2[6:5] are software controllable but initially are set by the reset configuration state of the $\overline{\text{MCP}}$ and CKE signals, respectively; PMCR2[4] can be changed by software. The default configuration for PMCR2[6:4] = 0b110 since the $\overline{\text{MCP}}$ and CKE signals have internal pull-up resistors, but this default configuration does not select 33 or 66 MHz PCI operation output timing parameters for the MPC8240; this choice is made by software. For the MPC8245, only 2 bits in the power management configuration register 2 (PMCR2), PMCR2[5:4] = PCI_HOLD_DEL, control the variable PCI output timing. PMCR2[5:4] are software controllable but initially are set by the inverted reset configuration state of the $\overline{\text{MCP}}$ and CKE signals, respectively. The default configuration for PMCR2[5:4] = 0b00 since the $\overline{\text{MCP}}$ and CKE signals have internal pull-up resistors and the values from these signals are inverted; this default configuration selects 66 MHz PCI operation output timing parameters. There are four programmable PCI output timing configurations on the MPC8245, see Table 10 for details.

Voltage sequencing requirements for the MPC8245 are similar to those for the MPC8240; however, there are two changes which are applicable for the MPC8245. First, there is an additional requirement for the MPC8245 that the non-PCI input voltages (V_{IN}) must not be greater than GVdd or OVdd by more than 0.6 V at all times including during power-on reset (see caution 5 in Table 2). Second, for the MPC8245, LVdd must not exceed OVdd by more than 3.0 V at any time including during power-on reset (see caution 10 in Table 2); the allowable separation between LVdd and OVdd is 3.6 V for the MPC8240.

There is no LAVdd input voltage supply signal on the MPC8245 since the SDRAM clock delay-locked loop (DLL) has power supplied internally. Signal D17 should be treated as a no connect for the MPC8245.

1.7.8 JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 26 allows the COP to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted ensuring that the JTAG scan chain is initialized during power-on.

The COP header shown in Figure 26 adds many benefits—breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface—and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header).

There is no standardized way to number the COP header shown in Figure 26; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin 1 (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 26 is common to all known emulators.
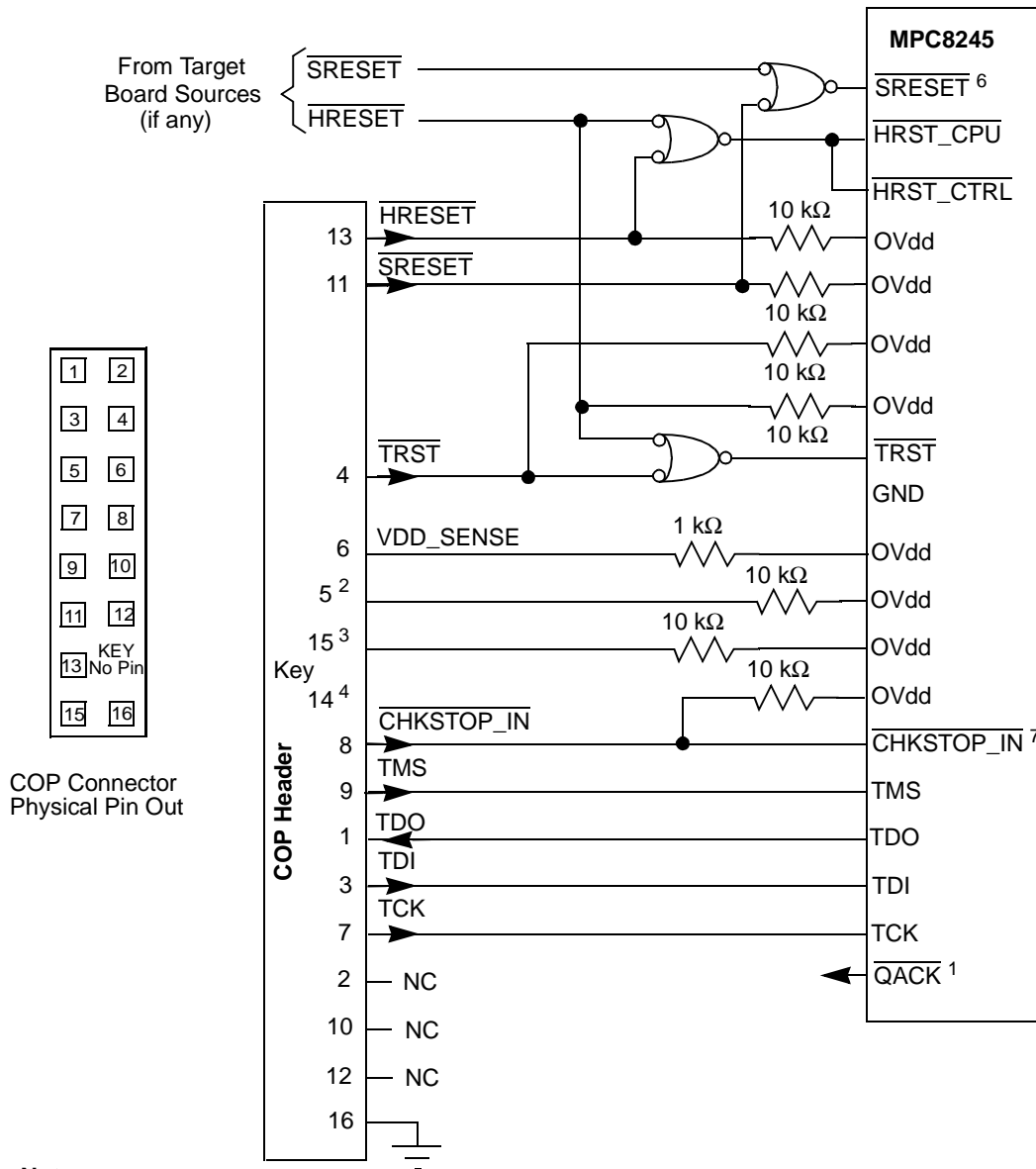
Notes:

1. $\overline{\text{QACK}}$ is an output on the MPC8245 and is not required at the COP header for emulation.
2. RUN/$\overline{\text{STOP}}$ normally found on pin 5 of the COP header is not implemented on the MPC8245. Connect pin 5 of the COP header to OVdd with a 1- kΩ pull-up resistor.
3. $\overline{\text{CKSTP\_OUT}}$ normally found on pin 15 of the COP header is not implemented on the MPC8245. Connect pin 15 of the COP header to OVdd with a 10-kΩ pull-up resistor.
4. Pin 14 is not physically present on the COP header.
5. Component not populated.
6. $\overline{\text{SRESET}}$ functions as output SDMA12 in extended ROM mode.
7. CHKSTOP_IN functions as output SDMA14 in extended ROM mode.

Figure 26. COP Connector Diagram

1.7.9 Thermal Management Information

This section provides thermal management information for the tape ball grid array (TBGA) package for air-cooled applications. Depending on the application environment and the operating frequency, heat sinks may be required to maintain junction temperature within specifications. Proper thermal control design is primarily dependent upon the system-level design: the heat sink, airflow, and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods: adhesive, spring clip to holes in the printed-circuit board or package, or mounting clip and screw assembly; see Figure 27.
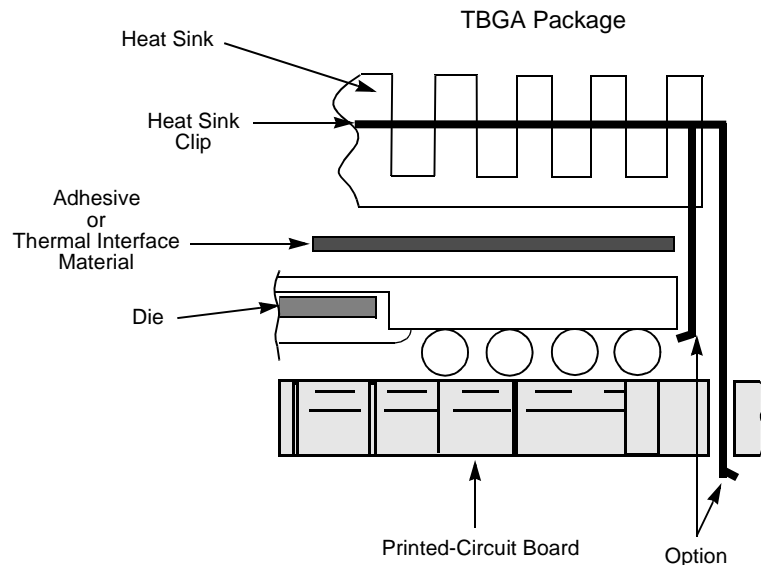
Figure 27. Package Exploded Cross-Sectional View with Several Heat Sink Options

Figure 28 depicts the die junction-to-ambient thermal resistance for four typical cases:

- A heat sink is not attached to the TBGA package and there exists a high board-level thermal loading from adjacent components.
- A heat sink is not attached to the TBGA package and there exists a low board-level thermal loading from adjacent components.
- A heat sink (for example, ChipCoolers #HTS255-P) is attached to the PBGA package and there exists high board-level thermal loading from adjacent components.
- A heat sink (for example, ChipCoolers #HTS255-P) is attached to the TBGA package and there exists low board-level thermal loading from adjacent components.
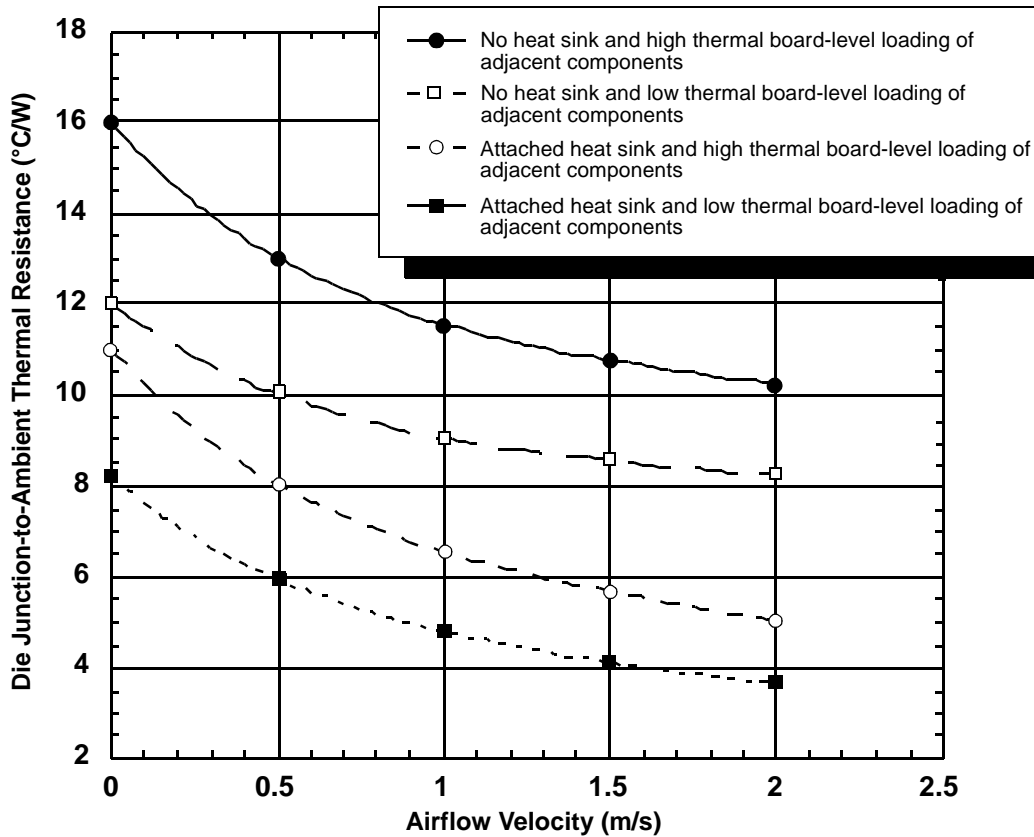
Figure 28. Die Junction-to-Ambient Resistance

The board designer can choose between several types of heat sinks to place on the MPC8245. There are several commercially available heat sinks for the MPC8245 provided by the following vendors:

Aavid Thermalloy	603-224-9988
80 Commercial St.	
Concord, NH 03301	
Internet: www.aavidthermalloy.com	
Alpha Novatech	408-749-7601
473 Sapena Ct. #15	
Santa Clara, CA 95054	
Internet: www.alphanovatech.com	
The Bergquist Company	800-347-4572
18930 West 78th St.	
Chanhassen, MN 55317	
Internet: www.bergquistcompany.com	
International Electronic Research Corporation (IERC)	818-842-7277
413 North Moss St.	
Burbank, CA 91502	
Internet: www.ctscorp.com	

Tyco Electronics   800-522-6752
Chip Coolers™
P.O. Box 3668
Harrisburg, PA 17105-3668
Internet: www.chipcoolers.com

Wakefield Engineering   603-635-5102
33 Bridge St.
Pelham, NH 03076
Internet: www.wakefield.com

Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost. Other heat sinks offered by Aavid Thermalloy, Alpha Novatech, The Bergquist Company, IERC, Chip Coolers, and Wakefield Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need airflow.

1.7.9.1   Internal Package Conduction Resistance

For the TBGA, cavity down, packaging technology, shown in Figure 29, the intrinsic conduction thermal resistance paths are as follows:

- The die junction-to-case thermal resistance
- The die junction-to-ball thermal resistance

Figure 29 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

(Note the internal versus external package resistance)
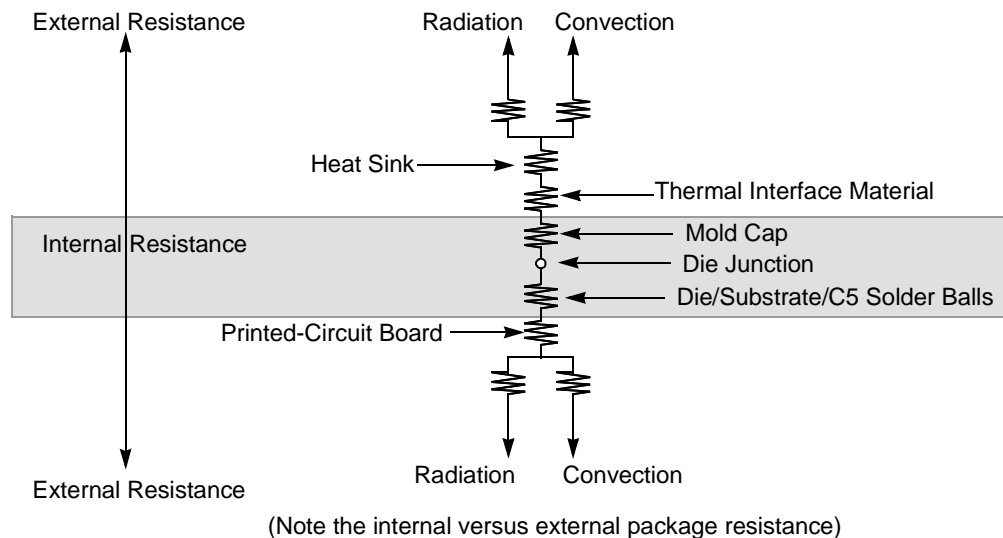
Figure 29. PBGA Package with Heat Sink Mounted to a Printed-Circuit Board

For this die-up, wire-bond PBGA package, heat generated on the active side of the chip is conducted mainly through the mold cap, the heat sink attach material (or thermal interface material), and finally through the heat sink where it is removed by forced-air convection.

1.7.9.2   Adhesives and Thermal Interface Materials

A thermal interface material is recommended between the top of the mold cap and the bottom of the heat sink to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 30 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately seven times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 30). Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure. Of course, the selection of any thermal interface material depends on many factors: thermal performance requirements, manufacturability, service temperature, dielectric properties, cost, etc.
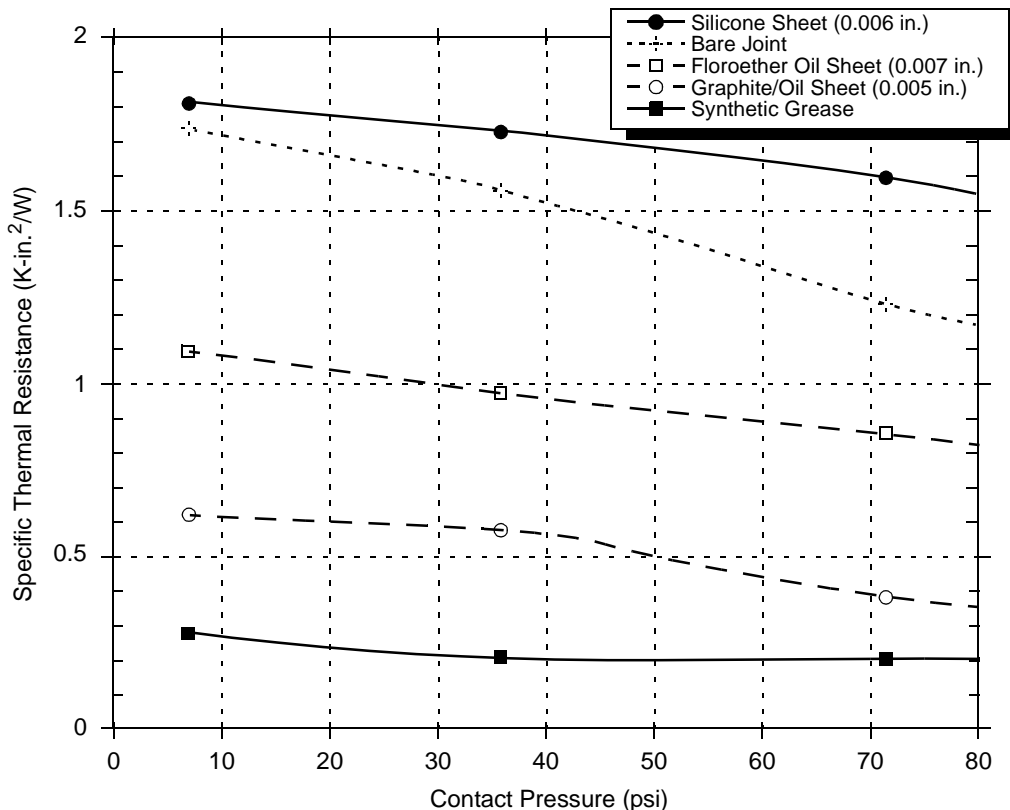
Figure 30. Thermal Performance of Select Thermal Interface Material

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements. There are several commercially-available thermal interfaces and adhesive materials provided by the following vendors:

Chomerics, Inc.   781-935-4850
77 Dragon Ct.
Woburn, MA 01888-4014
Internet: www.chomerics.com

Dow-Corning Corporation   800-248-2481
Dow-Corning Electronic Materials
2200 W. Salzburg Rd.
Midland, MI 48686-0997
Internet: www.dow.com

Shin-Etsu MicroSi, Inc.   888-642-7674
10028 S. 51st St.
Phoenix, AZ 85044
Internet: www.microsi.com

Thermagon Inc.   888-246-9050
4707 Detroit Ave.
Cleveland, OH 44102
Internet: www.thermagon.com

1.7.9.3   Heat Sink Usage

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where

T_A = ambient temperature for the package (°C)
$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
P_D = power dissipation in the package (W)

The junction-to-ambient thermal resistance is an industry-standard value that provides a quick and easy estimation of thermal performance. Unfortunately, two values are in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed-circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where

$R_{\theta JA}$ = junction-to-ambient thermal resistance (°C/W)
$R_{\theta JC}$ = junction-to-case thermal resistance (°C/W)
$R_{\theta CA}$ = case-to-ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on the printed-circuit board, or the thermal dissipation on the printed-circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the thermal characterization parameter (θ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\theta_{JT} \times P_D)$$

where:

T_T = thermocouple temperature atop the package (°C)
θ_{JT} = thermal characterization parameter (°C/W)
P_D = power dissipation in package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

When a heat sink is used, the junction temperature is determined from a thermocouple inserted at the interface between the case of the package and the interface material. A clearance slot or hole is normally required in the heat sink. Minimizing the size of the clearance is important to minimize the change in thermal performance caused by removing part of the thermal interface to the heat sink. Because of the experimental difficulties with this technique, many engineers measure the heat sink temperature and then back calculate the case temperature using a separate measurement of the thermal resistance of the interface. From this case temperature, the junction temperature is determined from the junction-to-case thermal resistance.

In many cases, it is appropriate to simulate the system environment using a computational fluid dynamics thermal simulation tool. In such a tool, the simplest thermal model of a package which has demonstrated reasonable accuracy (about 20%) is a two-resistor model consisting of a junction-to-board and a junction-to-case thermal resistance. The junction-to-case covers the situation where a heat sink will be used or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed-circuit board.

1.7.10 References

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Mountain View, CA 94043
(415) 964-5111

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

1.8 Document Revision History

Table 19 provides a revision history for this hardware specification.

Table 19. Revision History Table

Revision No.	Substantive Change(s)
0.0	Initial release.
0.1	Made Vdd/AVdd/AVdd2 = 1.8 V ± 100 mV information for 133 MHz memory interface operation to Section 1.3, Table 2, Table 5, Table 9, Table 17, and Section 1.7.2. Pin D17, formerly LAVdd (supply voltage for DLL), is a No Connect on the MPC8245 since the DLL voltage is supplied internally. Eliminated all references to LAVdd; updated Section 1.7.1. Previous Note 4 of Table 2 did not apply to the MPC8245 (MPC8240 document legacy). New Note 4 added in reference to max CPU speed at reduced Vdd voltage. Updated the Programmable Output Impedance of DEV_MEM_ADDR in Table 4 to 6 Ω to reflect characterization data. Updated Table 5 to reflect reduced power consumption when operating Vdd/AVdd/AVdd2 = 1.8 V ±100 mV. Changed Notes 2, 3, and 4 to reflect Vdd at 1.9 V. Changed Note 5 to represent Vdd = AVdd = 1.8 V. Updated Table 7 to reflect Vdd/AVdd/AVdd2 voltage level operating frequency dependencies; changed 250 MHz device column to 266 MHz; modified Note 1 eliminating VCO references; added Note 2. Changed 250 MHz processor frequency offering to 266 MHz. Changed Spec 12b for memory output valid time in Table 10 from 5.5 ns to 4.5 ns; this is a key specification change to enable 133 MHz memory interface designs. Updated Pinout Table 16 with the following changes: • Pin Types for $\overline{\text{RCS0}}$, $\overline{\text{RCS3}}$/TRIG_OUT and DA[11:15] were erroneously listed as I/O, changed Pin Types to Output. • Pin Types for $\overline{\text{REQ4}}$/DA4, $\overline{\text{RCS2}}$/TRIG_IN, and PLL_CFG[0:4]/DA[10:6] were erroneously listed as Input, changed Pin Types to I/O. • Changed Pin D17 from LAVdd to No Connect; deleted Note 21 and references. • Notes 3, 5, and 7 contained references to the MPC8240 (MPC8240 document legacy); changed these references to MPC8245. • Previous Notes 13 and 14 did not apply to the MPC8245 (MPC8240 document legacy), these notes were deleted; moved Note 19 to become new Note 13; moved Note 20 to become new Note 14; updated associated references. • Added Note 3 to SDMA[1:0] signals about internal pull-up resistors during reset state. • Reversed vector ordering for the PCI Interface Signals: $\overline{\text{C/BE}}$[0:3] changed to $\overline{\text{C/BE}}$[3:0], AD[0:31] changed to AD[31:0], $\overline{\text{GNT}}$[0:3] changed to $\overline{\text{GNT}}$[3:0], and $\overline{\text{REQ}}$[0:3] changed to $\overline{\text{REQ}}$[3:0]. The package pin number orderings were also reversed meaning that pin functionality did NOT change. For example, AD0 is still on signal C22, AD1 is still on signal D22, ..., AD31 is still on signal V25. This change was made to make the vectored PCI signals in this hardware specification consistent with the *PCI Local Bus Specification* and the *MPC8245 Integrated Processor User's Manual* vector ordering. • Changed $\overline{\text{TEST1}}$/$\overline{\text{DRDY}}$ signal on pin B20 to $\overline{\text{DRDY}}$. • Changed $\overline{\text{TEST2}}$ signal on pin Y2 to RTC for performance monitor use. Updated PLL Table 17 with the following changes for 133 MHz memory interface operation: • Added Ref. 9 (01001) and Ref. 17 (10111) details; removed these settings from Note 10 (reserved settings list). • Enhanced range of Ref. 10 (10000). • Updated Note 13, changed bits 16–20 erroneous information to correct bits 23–19. • Added Notes 16 and 17. Added information to Section 1.7.8, in reference to $\overline{\text{CHKSTOP\_IN}}$ and $\overline{\text{SRESET}}$ not being available in extended ROM mode.

Table 19. Revision History Table (continued)

Revision No.	Substantive Change(s)
0.2	Changed core supply voltage to 2.0 ± 100 mV in Section 1.3. (Supply voltage of 1.8 ± 100 mV is no longer recommended.) Changed rows 2, 5, and 6 of Table 2 to 2.0 ± 100 mV in the "Recommended Value" column. Changed the power consumption numbers in Table 5 to reflect the power values for Vdd = 2.0 V. (Notes 2, 3, 4, and 5 of the table were also updated to reflect the new value of Vdd.) Updated Table 9 for Vdd/AVdd/AVdd2 to 2.0 ± 100 mV. Table 8: Vdd/AVdd/AVdd2 was changed to 2.0 V for both CPU frequency offerings. Note 2 was updated by removing the "at reduced voltage..." statement. Table 10: Update maximum time of the rows 12a0 through 12a3. Table 16: Fixed overbars for the active-low signals. Changed pin type information for Vdd, AVdd, and AVdd2 to 2.0 V. Changed note 16 of Table 17 to a value of 2.0 V for Vdd/AVdd/AVdd2. Removed second sentence of the second paragraph in Section 1.7.2, because it referenced information about a 1.8-V design. Removed reference to 1.8 V in third sentence of Section 1.7.7.
0.3	Section 1.4.1.5: Changed Max-FP value for 33/133/266 of Table 5, from 2.3 to 2.1 watts, to represent characterizaiton data. Changed Note 4 to say Vdd = 2.1 for power measurements (for 2-V part). Changed numbers for maximum I/O power supplies for OVdd and GVdd to represent characterization data. Section 1.4.3.1: Added four graphs (Figures 5–8) and description for DLL Locking Range vs. Frequency of Operation to replace Figure 5 of Rev 0.2 document. Section 1.4.3.2: Added row (item 11: T_{su}—SDRAM_SYNC_IN to PCI_SYNC_IN timing) to Table 9, to include offset change requirement. Section 1.5.3: Changed Note 4 of PLL_CFG pins in Table 16 to Note 20. Section 1.7.2: Added diode (MUR420) to Figure 27, Voltage Sequencing Circuit. This is to compensate for voltage extremes in design. Section 1.7.5: Added sentence with regards to SDRAM_SYNC_IN to PCI_SYNC_IN timing requirement (T_{su}) as a connection recommendation. Section 1.7.8 : Mention of T_{su} offset timing, and driver capability differences between the MPC8240 and the MPC8245.
0.4	Section 1.2: Changed Features list (format) to match with the features list of the *MPC8245 Integrated Processor User's Manual*. Section 1.4.1.2 Updated Table 2 to include 1.8 ± 100mV numbers. Section 1.4.3: Changed Table 7 to include new part offerings of 333 and 350 MHz. Added rows to include VCO frequency ranges for all parts for both memory VCO and CPU VCO. Section 1.4.1.5: Updated power consumption table to include 1.8 V (Vdd) and higher frequency numbers. Section 1.4.3: Updated Table 7 to include higher frequency offerings and CPU VCO frequency range. Section 1.4.3.1: Changed lettering to caps for DLL_EXTEND and DLL_MAX_DELAY in graph description section. Section 1.4.3.2: Changed name of item 11 from T_{su}—SDRAM_SYNC_IN to PCI_SYNC_IN Time to T_{os}—SDRAM_SYNC_IN to *sys_logic_clk* Offset Time. Changed name to T_{os} in Note 7 as well. Section 1.6: Updated notes in Table 17. Included minimum and maximum VCO numbers for memory VCO. Changed Note 13 for location of PLL_CFG[0:4] to correct bits location. Bits 7–4 of register offset <0xE2>. Added Table 18 to cover PLL configuration of higher frequency part offerings. Section: 1.7 Changed frequency ranges for reference numbers 0, 9, 10, and 17, for the 300 MHz part, to include the higher memory bus frequencies when operating at lower CPU bus frequencies. Added Table 18 to include PLL configurations for the 333 MHz and the 350 MHz CPU part offerings. Added VCO multiplers in Tables 17 and 18. Section 1.7.8: Changed T_{su}—SDRAM_SYNC_IN to PCI_SYNC_IN Time to T_{os}—SDRAM_SYNC_IN to *sys_logic_clk* Offset Time." Section 1.7.10: Added vendor (Cool Innovations, Inc.) to list of Heat Sink vendors.

Table 19. Revision History Table (continued)

Revision No.	Substantive Change(s)
0.5	Corrected labels for Figures 5 through 8.
1.0	Updated document template. Section 1.4.1.4—Changed the driver type names in Table 6 to match with the names used in the MPC8245 User's Manual. Section 1.5.3—Updated driver type names for signals in Table 16 to match with names used in the *MPC8245 Integrated Processor User's Manual*. Section 1.4.1.2—Updated Table 7 to refer to new PLL Tables for VCO limits. Section 1.4.3.3—Added item 12e to Table 10 for SDRAM_SYNC_IN to Output Valid timing. Section 1.5.1—Updated Solder Balls information to 62Sn/36PB/2Ag. Section 1.6—Updated PLL Tables 17 and 18 and appropriate notes to reflect changes of VCO ranges for memory and CPU frequencies. Section 1.7—Updated voltage sequencing requirements in Table 2 and removed Section 1.7.2. Section 1.7.8—Updated TRST inforrmation and Figure 26. New Section 1.7.2—Updated the range of I/O power consumption numbers for OVDD and GVDD to correct values as in Table 5. Updated fastest frequency combination to 66:100:350 MHz. Section 1.7.9—Updated list for Heat Sink and Thermal Interface vendors. Section 1.9—Changed format of Ordering Information section. Added tables to reflect part number specifications also available. Added Sections 1.9.2 and 1.9.3.

1.9 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 1.9.1, "Part Numbers Fully Addressed by This Document." Section 1.9.2, "Part Numbers Not Fully Addressed by This Document," lists the part numbers which do not fully conform to the specifications of this document. These special part numbers require an additional document called a part number specification.

1.9.1 Part Numbers Fully Addressed by This Document

Table 20 provides the Motorola part numbering nomenclature for the MPC8245. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Motorola sales office. In addition to the processor frequency, the part numbering scheme also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 20. Part Numbering Nomenclature

XPC	*nnnn*	L	*xx*	*nnn*	*x*	*x*
Product Code	**Part Identifier**	**Process Descriptor**	**Package** [1]	**Processor Frequency** [2]	**Application Modifier**	**Revision Level**
XPC	8245	L = Standard Spec.	ZU = TBGA	266 300	L: 1.8/2.0 V ± 100 mV 0° to 105°C	Contact Local Motorola Sales Office (Revisions A, B)
XPC	8245	L = Standard Spec.	ZU = TBGA	333 350	L: 2.0 V ± 100 mV 0° to 105°C	Contact Local Motorola Sales Office (Revisions A, B)

Notes:
1. See Section 1.5, "Package Description," for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by part number specifications may support other maximum core frequencies.

1.9.2 Part Numbers Not Fully Addressed by This Document

Parts with application modifiers or revision levels not fully addressed in this specification document are described in separate part number specifications which supplement and supersede this document; see Table 21.

Table 21. Part Numbers with Separate Documentation

Part Number Series	Operating Conditions	Document Order Number of Applicable Specification
XPC8245**T**ZU*nnn*x	2.0 V ± 100 mV, **–40° to 105°C** 266 MHz, 300 MHz, 333 MHz, 350 MHz	MPC8245TZUPNS/D
XPC8245**R**ZU*nnn*x	**2.1 V ± 100 mV, 0° to 85°C** 400 MHz	MPC8245RZUPNS/D

Note: For other differences, see applicable specifications.

1.9.3 Part Marking

Parts are marked as the example shown in Figure 31.
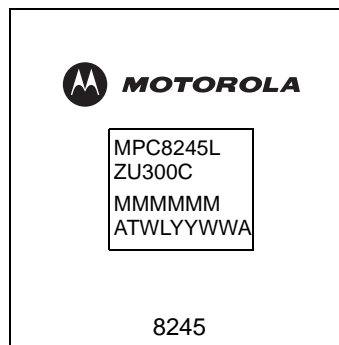
Notes:

MMMMMM is the 6-digit mask number.
ATWLYYWWA is the traceability code.
CCCCC is the country of assembly. This space is left blank if parts are assembled in the United States.

Figure 31. Part Marking for TBGA Device

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