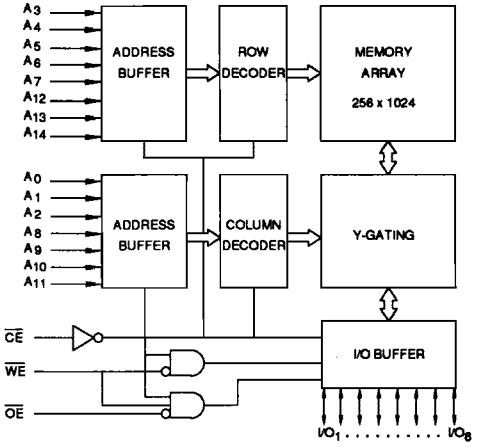
Features

- **Fast Read Access Time - 20 ns**
- **Low Power**
  - **100 mA Maximum (Active)**
  - **0.1 mA Maximum (Standby)**
- **Fully Static: No Clock Required**
- **Two Control Inputs ($\overline{CE}$ and $\overline{OE}$)**
- **TTL Compatible Inputs and Outputs**
- **5 V ± 10% Supply**
- **28-Lead Dual In-line and Surface Mount Packages**
- **JEDEC Pinout**
- **Commercial and Industrial Temperature Ranges**

256K (32K x 8) CMOS SRAM

Block Diagram



Description

The AT38H256 is a high performance CMOS static Random Access Memory. Its 256K of memory is organized as 32768 words by eight bits. Manufactured with an advanced CMOS technology, the AT38H256 offers access times down to 20 ns. When the AT38H256 is deselected, the standby current is just 0.1 mA.

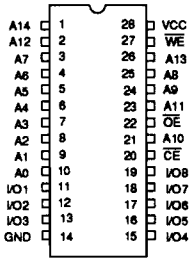
The AT38H256 powers down to the standby mode when deselected ($\overline{CE}$ is HIGH). The I/O pins remain in the high impedance state unless the chip is selected (CE is LOW), the outputs are enabled ($\overline{OE}$ is LOW), and Write Enable is not active ($\overline{WE}$ is HIGH).

The AT38H256 is completely TTL compatible and requires a single five-volt power supply. The device is fully static and does not need any clocks or refresh control signals for operation.

Pin Configurations

For .300 DIP/.600 DIP/.300 SOJ

Pin Name	Function
A_0-A_{14}	Addresses
I/O_1-I/O_8	Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}, GND	Power, Ground



Absolute Maximum Ratings*

Temperature Under Bias	-55° C to 125° C
Storage Temperature	-65° C to 150° C
All Input Voltages (including NC Pins) with Respect to Ground	-0.3 V[(1)] to V_{CC} + 0.3 V
All Output Voltages with Respect to Ground	-0.3 V[(1)] to V_{CC} + 0.3 V
Maximum Supply Voltage	+7.0 V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note:
1. Minimum input voltages are -3.5 V for pulse width less than 20 ns.

Device Operation

READ: When $\overline{CE}$ is LOW, $\overline{OE}$ is LOW, and $\overline{WE}$ is HIGH, the eight bits of data stored at the memory location determined by the address input (pins A_0 through A_{14}) are inserted on the data outputs (pins I/O_1 through I/O_8).

WRITE: When $\overline{CE}$ is LOW and $\overline{WE}$ is LOW, the eight bits of data placed on the input pins (I/O_1 through I/O_8) are stored at the memory location determined by the address input (pins A_0 through A_{14}).

Operating Modes

MODE\PIN	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	L	L	H	D_{OUT}
Write	L	X[(1)]	L	D_{IN}
Standby (Not Selected)	H	X	X	High Z
Output Disable (High Impedance)	X	H	X	High Z

Note: 1. X can be L (Low) or H (High)

D.C. and A.C. Operating Range

		AT38H256
Operating Temperature (Ambient)	Commercial	0°C - 70°C
	Industrial	-40°C - 85°C
V_{CC} Power Supply		5 V ± 10%

D.C. and Operating Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0 to V_{CC}				2	µA
I_{LO}	Output Leakage Current	$\overline{CE}$ = 2.2 V to V_{CC} + 0.3 V or $\overline{OE}$ = 2.2 V to V_{CC} + 0.3 V or $\overline{WE}$ = -0.3 V to 0.8 V $V_{I/O}$ = 0 to V_{CC}				2	µA
I_{SB1}	Standby Current (CMOS)	$\overline{CE} \geq V_{CC}$ - 0.2 V, $V_{IN} = (V_{CC} - 0.2\ V)$ or ≤ 0.2 V	Com.			0.1	mA
			Ind.			1.0	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = 2.2 V to V_{CC} +0.3 V, $V_{IN} = V_{IL}$ or V_{IH}				25	mA
I_{CC}	V_{CC} Active Current (TTL)	$\overline{CE}$ = -0.3 V to 0.8 V, I_{OUT} = 0 mA, min cycle				100	mA
V_{IL} (1)	Input Low Voltage			-0.3(2)		0.8	V
V_{IH} (1)	Input High Voltage			2.2 V		V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA				0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4.0 mA		2.4			V

Note: 1. These are voltages with repect to device GND.
2. V_{IL} = -3.0 V for pulse width less than 20 ns.

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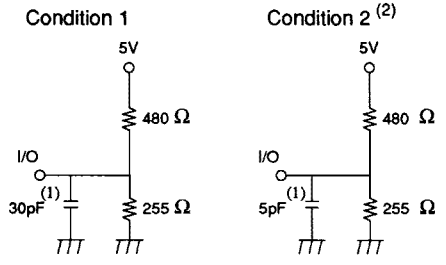
Pin Capacitance (f = 1 MHz, T = 25°C) (1)

Symbol	Parameter	Conditions	Min	Max	Units
C_{OUT}	Input/Output Capacitance	V_{OUT} = 0 V		10	pF
C_{IN}	Input Capacitance	V_{IN} = 0 V		10	pF

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

Output Test Load

Figure 1



Item	Condition
Input pulse "High" level	V_{IH} = 3.0 V
Input pulse "Low" level	V_{IL} = 0 V
Input rise time	t_R = 5 ns
Input fall time	t_F = 5 ns
Input and output reference level	1.5 V
Output load	See Figure 1

Notes: 1. Capacitance Load includes scope and jig capacitances.
2. For t_{COE}, t_{OOE}, t_{COD}, t_{OOD}, t_{WOE}, t_{WOD}.

A.C. Characteristics for Read

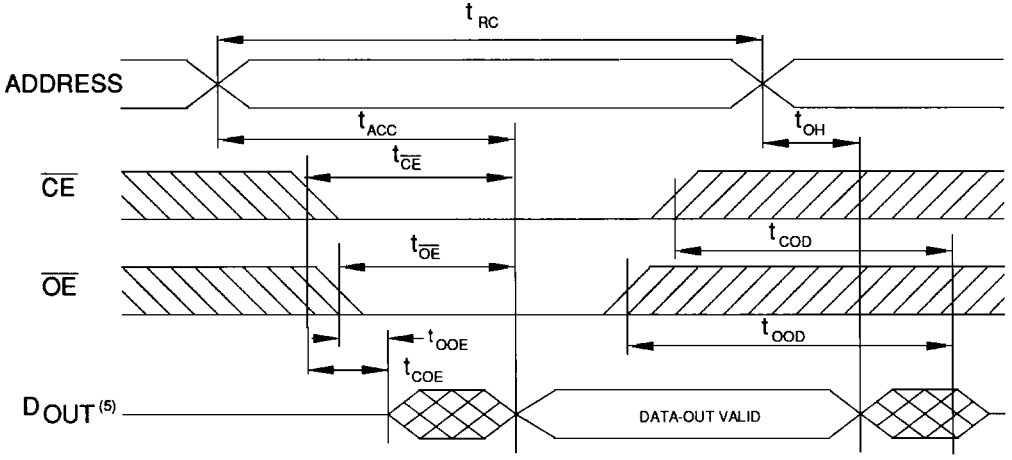
Symbol	Parameter	AT38H256-20		AT38H256-25		AT38H256-35		Units
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	20		25		35		ns
t_{ACC}	Address Access Time		20		25		35	ns
$t_{\overline{CE}}$	$\overline{CE}$ Access Time		20		25		35	ns
$t_{\overline{OE}}$	$\overline{OE}$ Access Time		12		12		20	ns
t_{OH}	Output Hold Time	5		5		5		ns
t_{COE} (1)	$\overline{CE}$ Output Enable Time	5		5		5		ns
t_{OOE} (1)	$\overline{OE}$ Output Enable Time	0		0		0		ns
t_{COD} (1)	$\overline{CE}$ Output Disable Time		10		10		15	ns
t_{OOD} (1)	$\overline{OE}$ Output Disable Time		13		13		15	ns

A.C. Characteristics for Write

Symbol	Parameter	AT38H256-20		AT38H256-25		AT38H256-35		Units
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	20		25		35		ns
t_{AS}	Address Setup Time	0		0		0		ns
t_{WP}	Write Pulse Width	15		20		30		ns
t_{CW}	$\overline{CE}$ Setup Time	15		20		30		ns
t_{WR}	Write Recovery Time	2		2		2		ns
t_{DS}	Data Setup Time	12		12		15		ns
t_{DH}	Data Hold Time	0		0		0		ns
t_{WOE} (1)	$\overline{WE}$ Output Enable Time	0		0		0		ns
t_{WOD} (1)	$\overline{WE}$ Output Disable Time		8		13		15	ns

Note: 1. Transition is measured by ±500 mV from the normal state with the output test load circuit, condition 2. This parameter is sampled and is not 100% tested.

A.C. Waveforms for Read Cycle [1]



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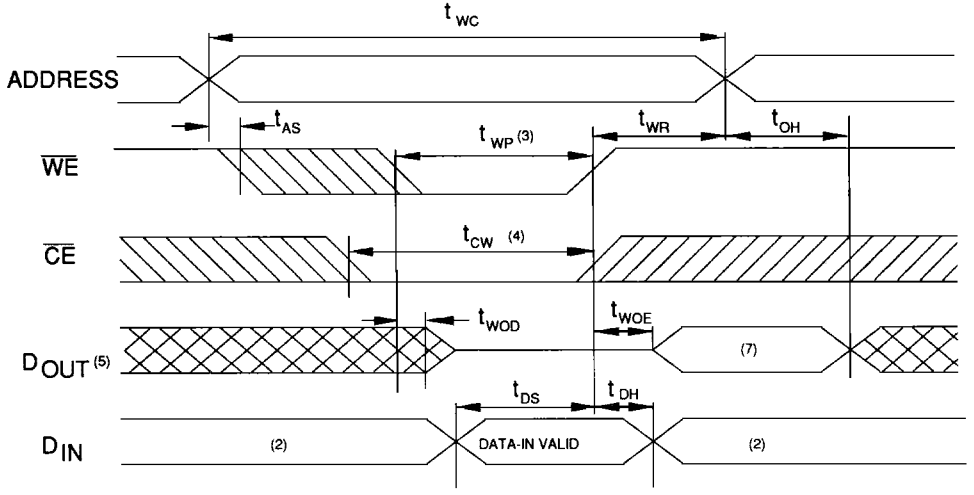
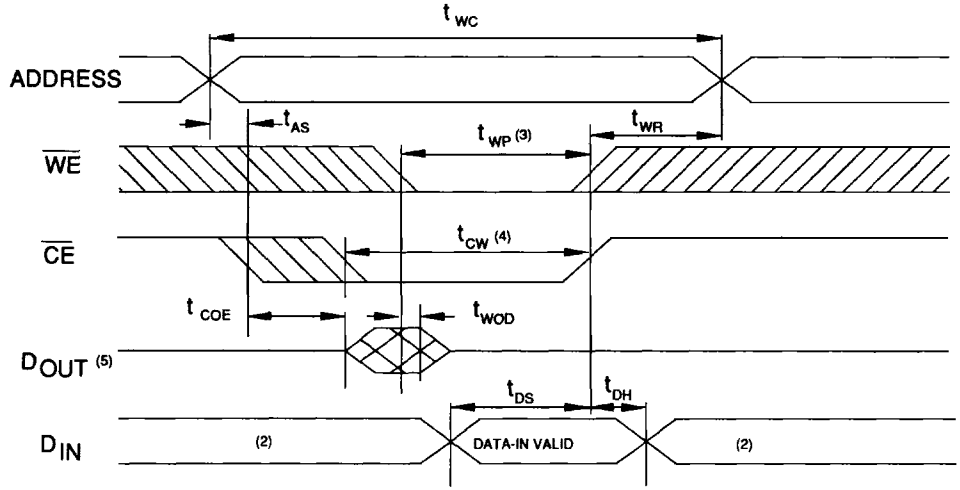
A.C. Waveforms for Write Cycle 1 ($\overline{WE}$ Write) [6]



A.C. Waveforms for Write Cycle 2 ($\overline{WE}$ Write) [6]



Notes:
1. During a Read Cycle, $\overline{WE}$ should be HIGH.
2. During this period, I/O pins are in the output state.
3. A Write occurs when $\overline{CE}$ and $\overline{WE}$ are LOW at the same time.
   A Write begins at the latest transition among $\overline{CE}$ going LOW, and $\overline{WE}$ going LOW.
   A Write ends at the earliest transition among $\overline{CE}$ going HIGH, and $\overline{WE}$ going HIGH.
   t_{WP} is measured from the beginning of Write to the end of Write.
4. t_{CW} is measured from the later of $\overline{CE}$ going LOW or going HIGH to the end of Write.
5. If $\overline{CE}$ or $\overline{OE}$ is HIGH, or $\overline{WE}$ is LOW, D_{OUT} goes to a high impedance state.
6. During a write cycle, $\overline{OE} = V_{IH}$ or V_{IL}.
7. D_{OUT} is equal to the Input Data written during the same cycle.

Ordering Information

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
20	100	0.1	AT38H256-20NC AT38H256-20XC	28P3 28S2	Commercial (0° to 70°C)
20	100	1.0	AT38H256-20NI AT38H256-20XI	28P3 28S2	Industrial (-40° to 85°C)
25	100	0.1	AT38H256-25NC AT38H256-25XC	28P3 28S2	Commercial (0° to 70°C)
25	100	1.0	AT38H256-25NI AT38H256-25XI	28P3 28S2	Industrial (-40° to 85°C)
35	100	0.1	AT38H256-35NC AT38H256-35XC	28P3 28S2	Commercial (0° to 70°C)
35	100	1.0	AT38H256-35NI AT38H256-35XI	28P3 28S2	Industrial (-40° to 85°C)

Package Type	
28P3	28 Lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
28S2	28 Lead, 0.300" Wide, Plastic J-Leaded Small Outline (SOJ)