DENSE-PAC MICROSYSTEMS

32 Megabyte CMOS DRAM

DP3ED8MX32RSW

ADVANCED INFORMATION

DESCRIPTION:

The DP3ED8MX32RSW is an 8 Meg x 32 Dynamic RAM SO DIMM module. The module is constructed of four 4 Meg x 16 Dynamic RAM's which are surface mounted on an industry standard 72-pin SO DIMM substrate.

The DP3ED8MX32RSW provides for a compatible upgrade path from lower density JEDEC compatible modules. The module features high speed access times, common data inputs, outputs, Address, $\overline{CAS}$, Output and Write Enables, with power decoupling capacitors.

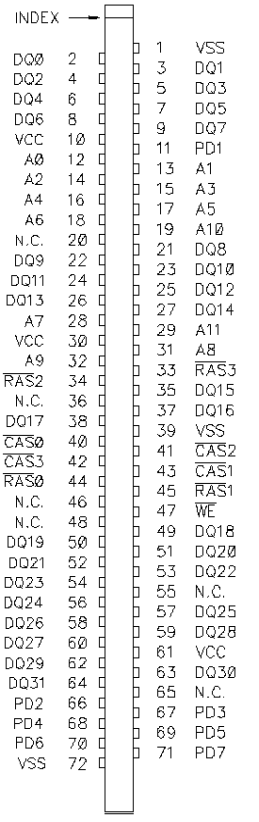
FEATURES:

- Access Times: 50, 60ns (max..)
- Single 3.3V±0.3V Supply
- Common Data Inputs and Outputs
- EDO Operating Mode
- 4096 Cycles / 64 ms
- 3 variations of Refresh:
  - $\overline{RAS}$ only Refresh
  - $\overline{CAS}$ before $\overline{RAS}$ Refresh
  - Hidden Refresh
- Industry Standard: 72-Pin SO DIMM

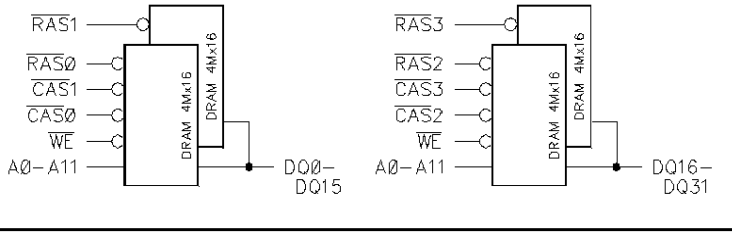
PIN NAMES	
A0 - A11	Row Address: A0 - A11 Column Address: A0 - A9 Refresh Address: A0 - A11
DQ0 - DQ31	Data In / Data Out
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobes
$\overline{RAS0}$ - $\overline{RAS3}$	Row Address Strobes
$\overline{WE}$	Read / Write Enables
V_{CC}	Power Supply (+3.3V)
V_{SS}	Ground
PD1 - PD7	Presence Detects
N.C.	No Connect

PIN-OUT DIAGRAM

BOTTOM VIEW



FUNCTIONAL BLOCK DIAGRAM



ADVANCED INFORMATION

RECOMMENDED OPERATING CONDITIONS					
Symbol	Parameter	Min.	Typ.	Max.	Units
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{IL}	Input Low Voltage	-0.3		0.8	V
V_{IH}	Input High Voltage	2.0		V_{CC}+0.3	V
T_A	Operating Temperature	0	+25	+70	°C

NOTE: All voltages referenced to V_{SS}.

CAPACITANCE: t_A = 25°C, f = 1MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	30	pF	V_{IN} = 0V
C_{CAS}	$\overline{CAS}$ Input	15		
C_{RAS}	$\overline{RAS}$ Input	10		
C_{WE}	Write Enable	30		
$C_{I/O}$	Data Input/Output	20		

PRESENCE DETECT & ID PINS		
PIN	50ns	60ns
PD1	N.C.	N.C.
PD2	N.C.	N.C.
PD3	V_{SS}	V_{SS}
PD4	V_{SS}	V_{SS}
PD5	V_{SS}	N.C.
PD6	V_{SS}	N.C.
PD7	N.C.	N.C.

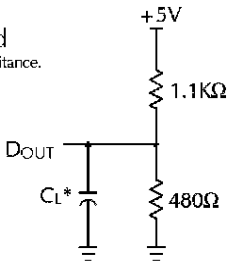
ABSOLUTE MAXIMUM RATINGS			
Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	-55 to +125	°C
$V_{I/O}$	Voltage on Any Pin	-0.5 to min. (V_{CC}+0.5, 4.6)	V
V_{CC}	V_{CC} Supply Voltage	-0.5 to +6.4	V
I_{OUT}	Output Current	50	mA

AC TEST CONDITIONS	
Input Pulse Levels	0V to 2.4V
Input Pulse Rise and Fall Times	5ns *
Input Timing Reference Levels	1.2V
Output Timing Reference Levels	1.2V

* Transition measured between 0.8V and 2.0V.

OUTPUT LOAD		
Load	CL	Parameters Measured
1	100pF	except t_{CLZ}
2	5pF	t_{CLZ}

Figure 1. Output Load
** Including Scope and Jig Capacitance.



DC OPERATING CHARACTERISTICS							
Symbol	Characteristic	Conditions	50ns		60ns		Units
			Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	$\overline{CAS}$0 - $\overline{CAS}$3	-4	+4	-4	+4	µA
		A0-A11, $\overline{WE}$	-16	+16	-16	+16	
		$\overline{RAS}$0 - $\overline{RAS}$2	-8	+8	-8	+8	
I_{OUT}	Output Leakage Current		-5	+5	-5	+5	µA
I_{CC1}	Operating Current	$\overline{RAS}$ and $\overline{CAS}$ cycling @ t_{RC} = min.		880		800	mA
I_{CC2}	Standby Current	$\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{IH}		8		8	mA
I_{CC3}	$\overline{RAS}$ - Only Refresh Current	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @ t_{RC} = min.		880		800	mA
I_{CC4}	Extended Data Out Mode	$\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = min.		880		800	mA
I_{CC5}	Standby Current	$\overline{RAS}$ = $\overline{CAS}$ = $\overline{WE}$ = V_{CC} -0.2V		4		4	mA
I_{CC6}	$\overline{CAS}$ - Before - $\overline{RAS}$ Refresh Current	$\overline{RAS}$ and $\overline{CAS}$ Cycling @ t_{RC} = min.		880		800	mA
V_{OL}	Output Low Voltage	I_{OL} = 2.0mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -2mA	2.4		2.4		V

A.C. OPERATING AND CHARACTERISTICS (V_{CC} = 3.3V ± 0.3V, T_A = 0°C to 70°C)

No.	Symbol	Parameter	50ns		60ns		Unit
			Min.	Max.	Min.	Max.	
1	t_{RC}	Random Read or Write Cycle Time	84		104		ns
2	t_{RWC}	Read Modify Write Cycle Time	116		140		ns
3	t_{RAC}	Access Time from $\overline{RAS}$ [3, 4, 10]		50		60	ns
4	t_{CAC}	Access Time from $\overline{CAS}$ [3, 4, 5]		13		15	ns
5	t_{AA}	Access Time from Column Address [3, 10]		25		30	ns
6	t_{CLZ}	$\overline{CAS}$ to Output in LOW-Z [3]	3		3		ns
7	t_{CEZ}	Output Buffer Turn-Off Delay From $\overline{CAS}$ [6,11]	3	13	3	15	ns
8	t_T	Transition Time (rise and fall) [2]	2	50	2	50	ns
9	t_{RP}	$\overline{RAS}$ Precharge Time	30		40		ns
10	t_{RAS}	$\overline{RAS}$ Pulse Width	50	10,000	60	10,000	ns
11	t_{RSH}	$\overline{RAS}$ Hold Time	13		15		ns
12	t_{CSH}	$\overline{CAS}$ Hold Time	38		45		ns
13	t_{CAS}	$\overline{CAS}$ Pulse Width [12]	8	10,000	10	10,000	ns
14	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time[4]	20	37	20	45	ns
15	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time [10]	15	25	15	30	ns
16	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		ns
17	t_{ASR}	Row Address Setup Time	0		0		ns
18	t_{RAH}	Row Address Hold Time	10		10		ns
19	t_{ASC}	Column Address Setup Time	0		0		ns
20	t_{CAH}	Column Address Hold Time	8		10		ns
21	t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25		30		ns
22	t_{RCS}	Read Command Setup Time	0		0		ns
23	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$ [8]	0		0		ns
24	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$ [8]	0		0		ns
25	t_{WCH}	Write Command Hold Time	10		10		ns
26	t_{WP}	Write Command Pulse Width	10		10		ns
27	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	13		15		ns
28	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	8		10		ns
29	t_{DS}	Data-In Setup Time [9]	0		0		ns
30	t_{DH}	Data-In Hold Time [9]	8		10		ns
31	t_{REF}	Refresh Period		32		32	ms
32	t_{WCS}	Write Command Setup Time [7]	0		0		ns
33	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time [7]	30		34		ns
34	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time [7]	67		79		ns
35	t_{AWD}	Column Address to $\overline{WE}$ Delay Time [7]	42		54		ns
36	t_{CSR}	$\overline{CAS}$ Set Up time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	5		5		ns

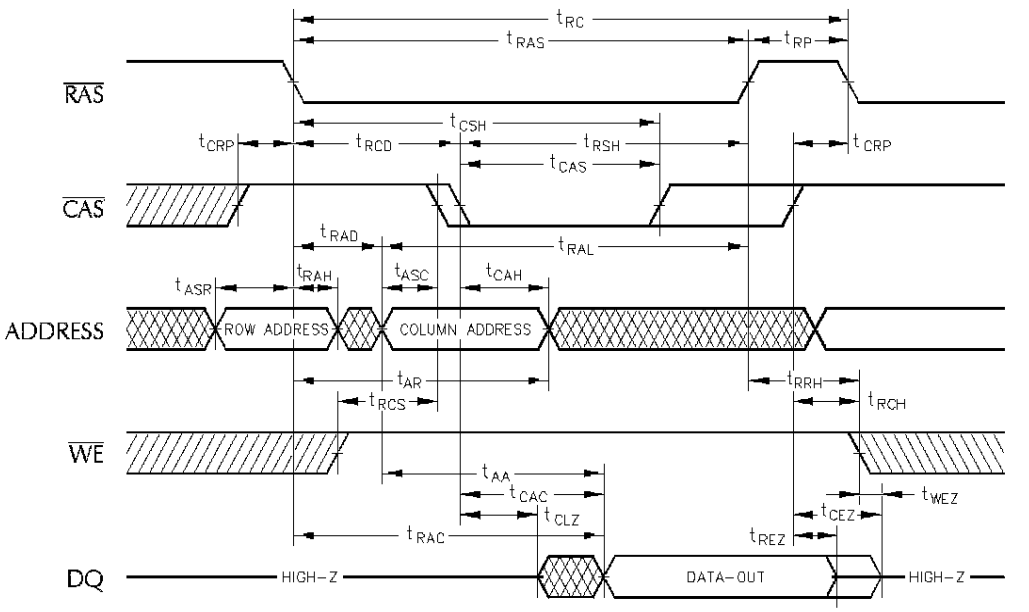
A.C. OPERATING AND CHARACTERISTICS (V_{DD} = 5.0V±10%, T_A = 0°C to 70°C) (Continued)							
No.	Symbol	Parameter	50ns		60ns		Unit
			Min.	Max.	Min.	Max.	
37	t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh) [14]	10		10		ns
38	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ precharge time	5		5		ns
39	t_{CPA}	Access time From $\overline{CAS}$ Precharge [3]		28		35	ns
40	t_{HPC}	Hyper Page Cycle Time [13]	20		25		ns
41	t_{HPRWC}	Hyper Page Read Modify Write Cycle [13]	47		56		ns
42	t_{CP}	$\overline{CAS}$ Precharge Time (Hyper Page Cycle)	8		10		ns
43	t_{RASP}	$\overline{RAS}$ Pulse Width (Hyper Page Cycle)	50	200,000	60	200,000	µs
44	t_{RHCP}	$\overline{RAS}$ Hold Time From $\overline{CAS}$ Precharge	30		35		ns
45	t_{CPWD}	$\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	47		54		ns
46	t_{WRP}	$\overline{WE}$ to $\overline{RAS}$ Precharge time ($\overline{C}$-B-$\overline{R}$ Refresh)	10		10		ns
47	t_{WRH}	$\overline{WE}$ to $\overline{RAS}$ Hold Time ($\overline{C}$-B-$\overline{R}$ Refresh)	10		10		ns
48	t_{DOH}	Output Data Hold Time	5		5		ns
49	t_{REZ}	Output Buffer Turn Off Delay From $\overline{RAS}$ [6, 12]	3	13	3	15	ns
50	t_{WEZ}	Output Buffer Turn Off Delay From $\overline{WE}$ [6]	3	13	3	15	ns
51	t_{WED}	$\overline{WE}$ to Data Delay	15		15		ns
52	t_{WPE}	$\overline{WE}$ Pulse Width (Hyper Page Cycle)	5		5		ns

NOTES:

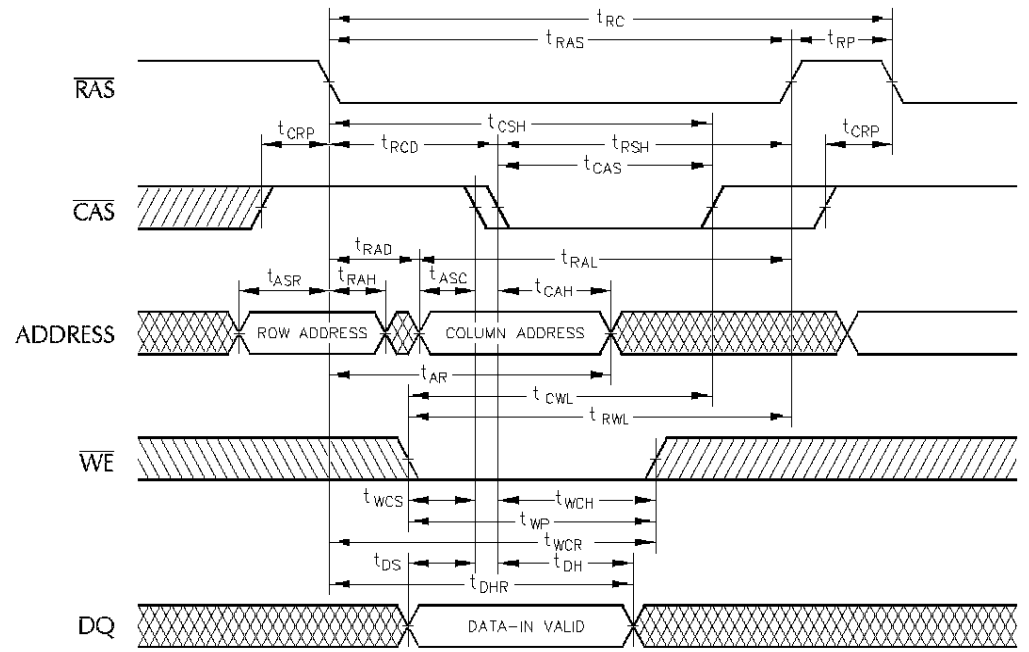
1. An initial pause of 200µs is required after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-ONLY or CBR) before proper operation is assured.
2. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} (min.) and V_{IL} (max.) and are assumes to be 2ns for all inputs.
3. Measured with the load equivalent to (1) one TTL load and 100pF.
4. Operation within the t_{RCD} (max.) limit ensures that t_{RAC} (max.) and can be met. t_{RCD} (max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max.).
6. This parameter defines the time at which the output achieves the open circuit conditions and is not referenced to V_{OL} or V_{OH}.
7. t_{WCS}, t_{RWC}, t_{CWD} and t_{AWD} are non restrictive operating parameters. They are included in the data sheet as electric characteristics only. If $t_{WCS} \geq t_{AWD}$ (min), the cycles is an early write cycle and the data output will remain high impedance for the duration of the cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), then the cycle is a read-modify-write cycle and the data output will contain the data read from the selected address. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to the $\overline{CAS}$ leading edge in early write cycles.
10. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled by t_{AA}.
11. t_{CEZ} (max.) and t_{REZ} (max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage level.
12. If $\overline{RAS}$ goes high before $\overline{CAS}$ high going, the open circuit condition of the output is achieved by $\overline{CAS}$ high going. If $\overline{CAS}$ goes high before $\overline{RAS}$ high going, the open circuit condition of the output is achieved by $\overline{RAS}$ high going.
13. $t_{ASC} \geq$ 6ns. Assume t_T = 2.0ns
14. It can get less $\overline{CAS}$ before $\overline{RAS}$ current loss if $t_{CHR} \geq t_{RAS}$ or $\overline{CAS} \leq$ 0.2V at $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

ADVANCED INFORMATION

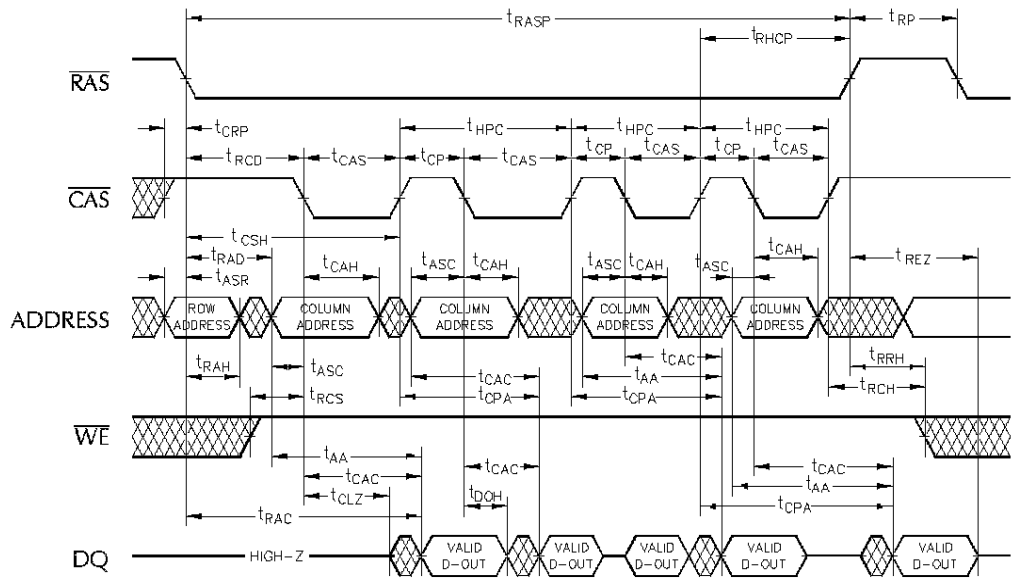
READ CYCLE



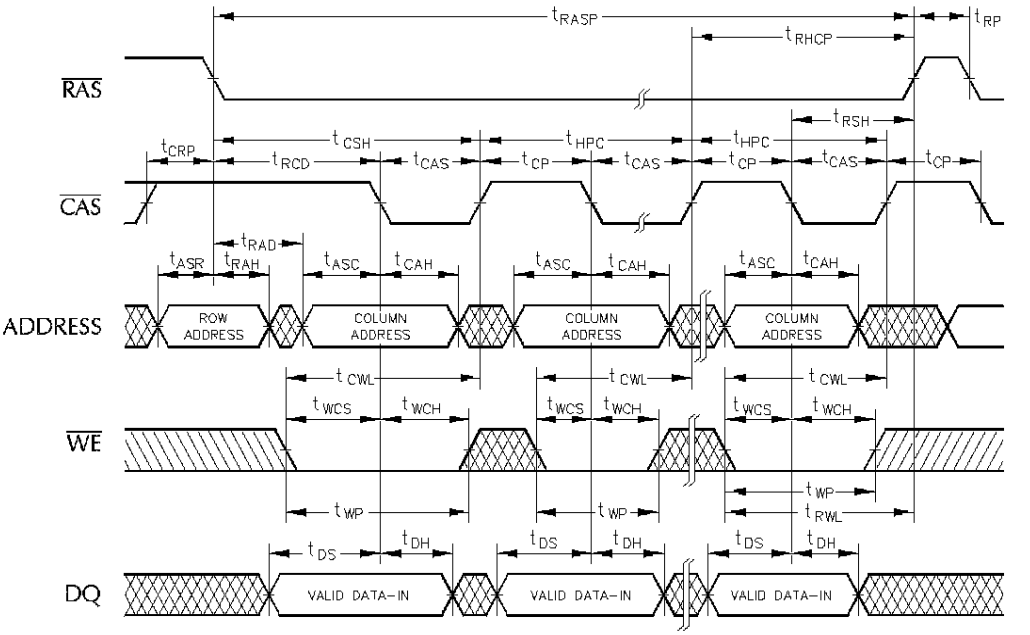
WRITE CYCLE (EARLY WRITE): D_{OUT} = OPEN



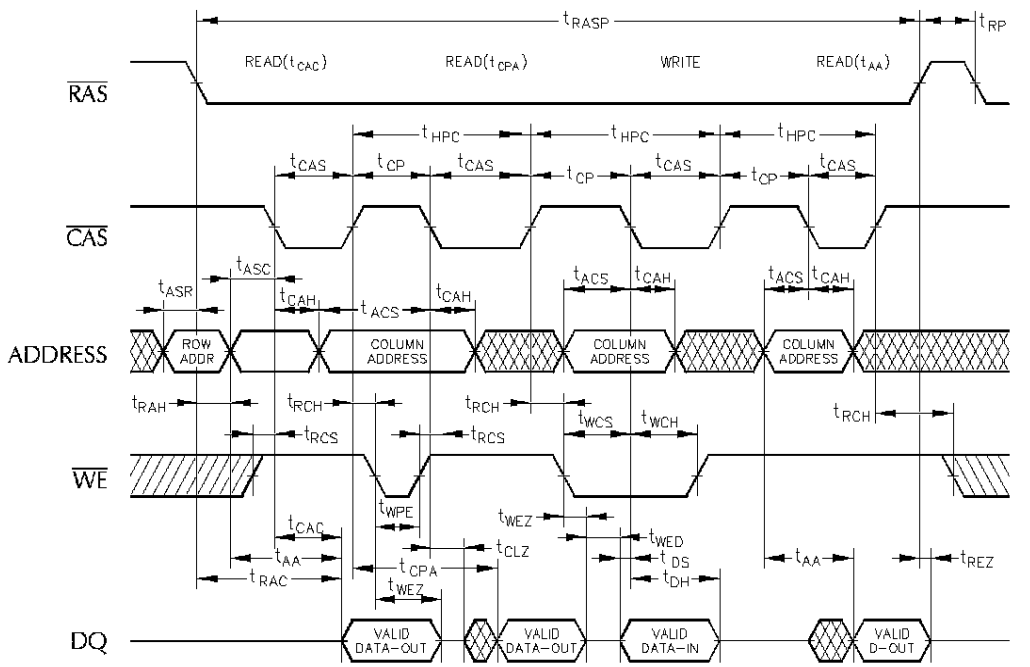
HYPER PAGE READ CYCLE



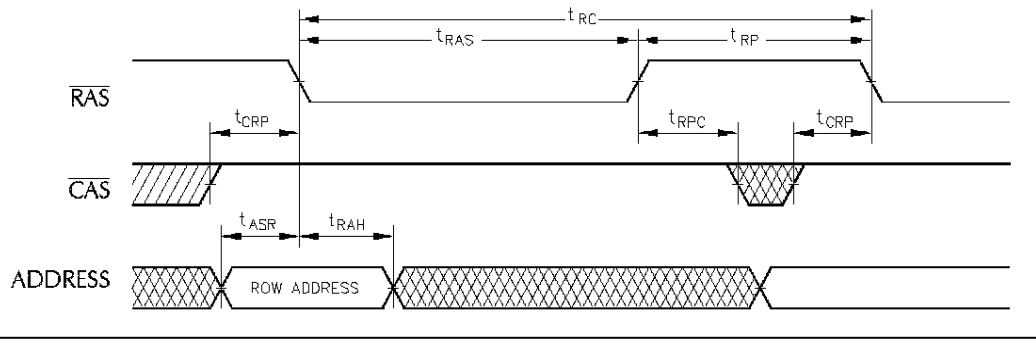
HYPER PAGE WRITE CYCLE (EARLY WRITE): D_{OUT} = OPEN



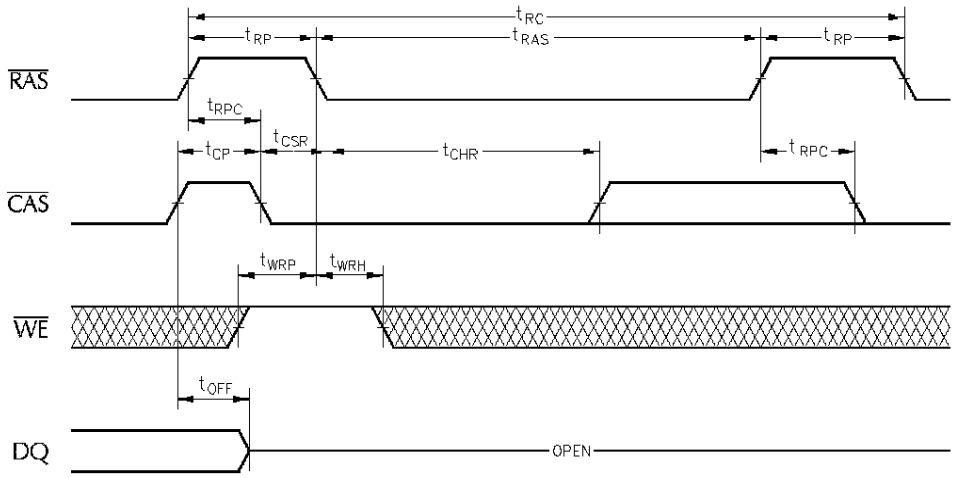
HYPER PAGE READ AND WRITE MIXED CYCLE



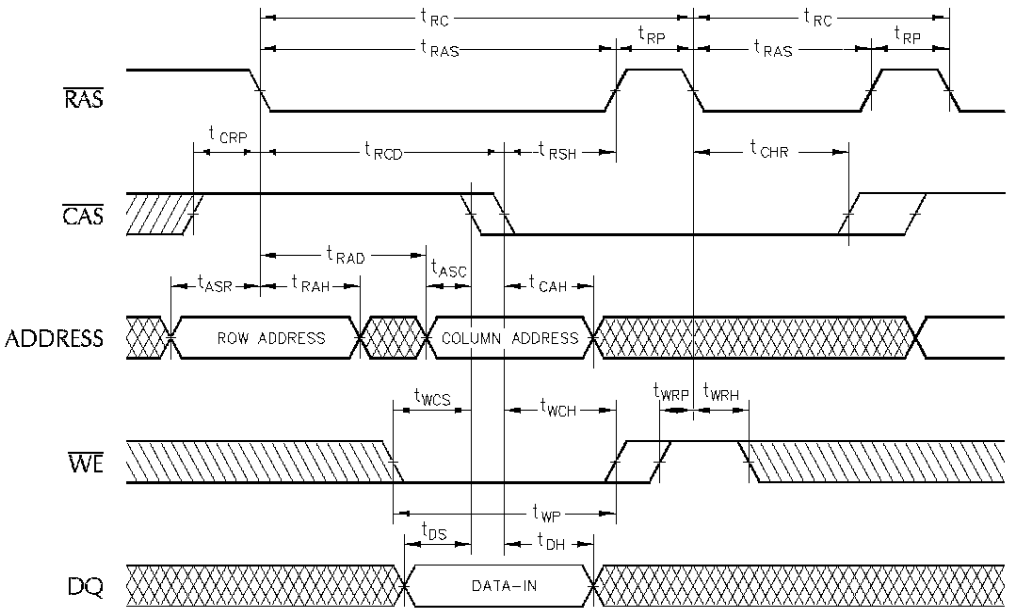
RAS - ONLY REFRESH CYCLE: WE, DIN = Don't Care: DOUT = Open



$\overline{CAS}$ - BEFORE- $\overline{RAS}$ REFRESH CYCLE: $\overline{WE}$, Address = Don't Care



HIDDEN REFRESH CYCLE (WRITE): D_{OUT} = Open



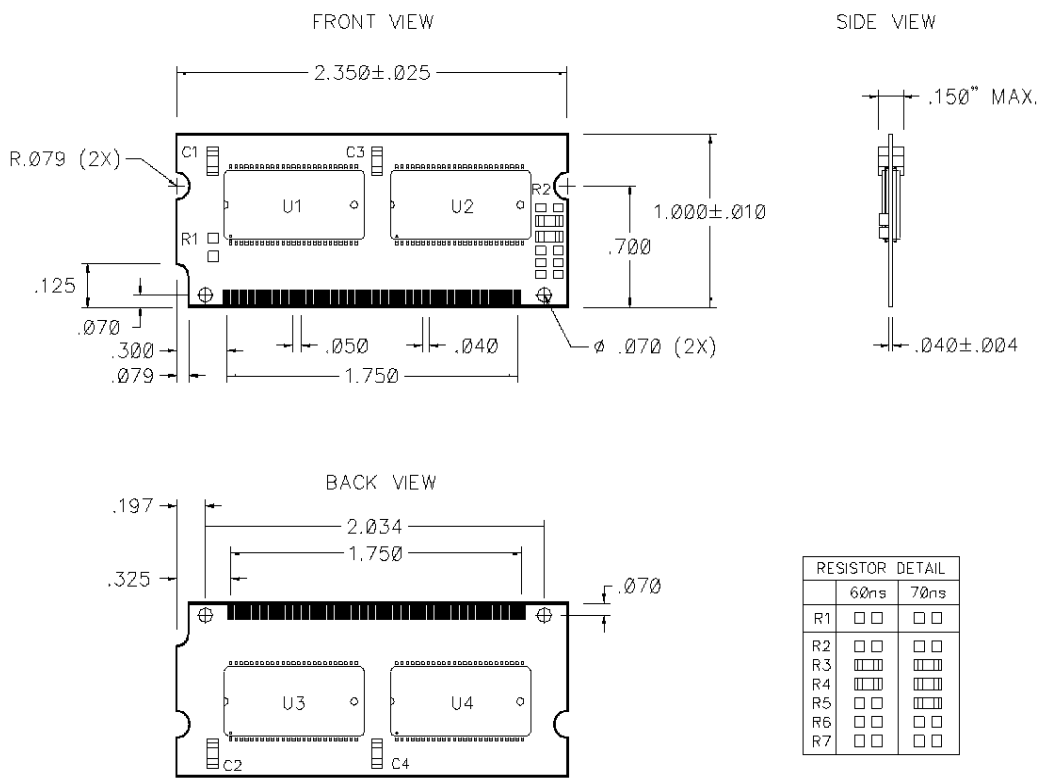
ADVANCED INFORMATION

ORDERING INFORMATION

DP	3ED	8M	X	32	R	SW	– XX	C	I
PREFIX	TYPE	MEMORY DEPTH	DESIG	MEMORY WIDTH	DESIG	PACKAGE	SPEED	GRADE	DESIG

- I: Blank GOLD CONTACTS; T TIN CONTACTS
- C: C COMMERCIAL 0°C to +70°C
- SPEED: 50 50ns; 60 60ns
- PACKAGE: SW 72-PIN SO DIMM
- DESIG: R 16 MEGABIT BASED
- DESIG: X MEMORY MODULE WITHOUT SUPPORT LOGIC
- TYPE: 3ED 3.3 VOLT, EDO MODE, DRAM

MECHANICAL DRAWING



RESISTOR DETAIL		
	60ns	70ns
R1	□□	□□
R2	□□	□□
R3	▥	▥
R4	▥	▥
R5	□□	▥
R6	□□	□□
R7	□□	□□

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