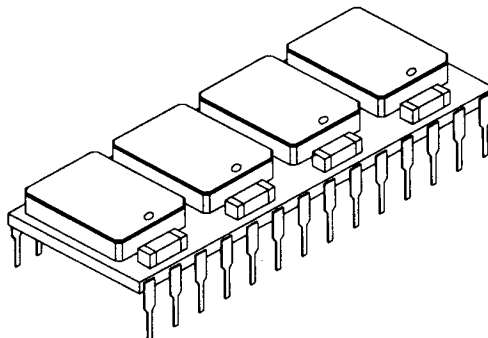


NOT RECOMENDED FOR NEW DESIGNS

DESCRIPTION:

The DPS88H16 is a 16K X 8 SRAM module built with eight 4K X 8 CMOS SRAMs in ceramic LCC packages surface mounted on a 28-pin, 0.600" wide Co-Fired DIP substrate. The memory utilizes asynchronous circuitry and may be maintained in any state for an indefinite period of time. All pins are TTL compatible, and a single +5V power supply is required.

The DPS88H16 is ideal for use in microprocessor systems and applications where high speed and/or board space is a prime concern.

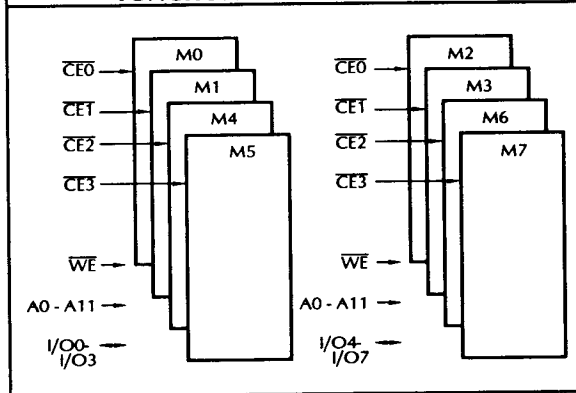


FEATURES:

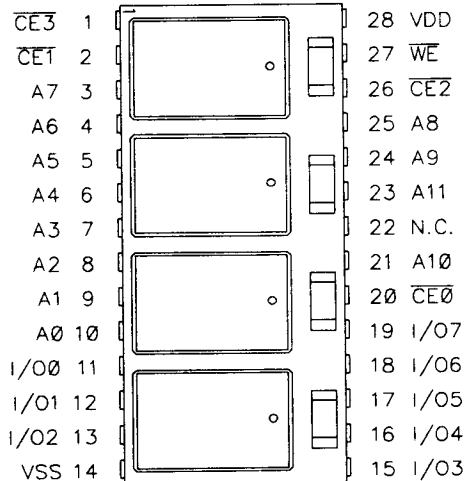
- 16K X 8 Organization
- Access Times: 25, 35, 45, 55ns (max.)
- Fully Static Operation; No Clock or Refresh Required
- TTL-compatible Inputs and Outputs
- Common Data Inputs and Outputs
- Single +5V Operation ($\pm 10\%$ Tolerance)
- Available with All Semiconductor Components used in the Construction of the Module Compliant to MIL-STD-883; Class B
- 28-Pin, 600 Mil Wide Ceramic DIP Package

PIN NAMES	
A0 - A11	Address Inputs
I/O0 - I/O7	Data Input/Output
$\overline{CE}0 - \overline{CE}3$	Chip Enables
$\overline{WE}$	Write Enable
VDD	Power (+5V)
Vss	Ground
N.C.	No Connect

FUNCTIONAL BLOCK DIAGRAM



PIN-OUT DIAGRAM



RECOMMENDED OPERATING RANGE¹

Symbol	Characteristic	Min.	Typ.	Max.	Unit
V _{DD}	Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input HIGH Voltage	2.2		V _{DD} +0.3	V
V _{IL}	Input LOW Voltage	-0.5 ²		0.8	V
T _A	Temperature Range	0		+70	°C

ABSOLUTE MAXIMUM RATINGS³

Symbol	Parameter	Value	Unit
T _{STG}	Storage Temperature	-65 to +150	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	°C
V _{DD}	Supply Voltage ¹	-0.5 to +7.0	V
V _{I/O}	Input/Output Voltage ¹	-0.5 to V _{DD} +0.5	V

TRUTH TABLE

Mode	$\overline{CE}$	$\overline{WE}$	I/O	Supply Current
Not Selected	H	X	HIGH-Z	Standby
Read	L	H	DOUT	Active
Write	L	L	DIN	Active

H = HIGH

L = LOW

X = Don't Care

CAPACITANCE ⁴: T_A = 25°C, F = 1.0MHz

Symbol	Parameter	Max.	Unit	Condition
C _{ADR}	Address Input	80	pF	V _{IN} = 0V
C _{CE}	Chip Enable	30		
C _{WE}	Write Enable	80		
C _{I/O}	Data Input/Output	60		

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

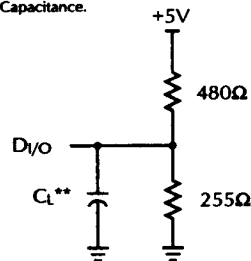
* Transition between 0.8V and 2.2V.

OUTPUT LOAD

Load	C _L	Parameters Measured
1	30 pF	except t _{CLZ} , t _{CHZ} , t _{WHZ} , and t _{WLZ}
2	5 pF	t _{CLZ} , t _{CHZ} , t _{WHZ} , and t _{WLZ}

Figure 1. Output Load

** Including Probe and jig Capacitance.



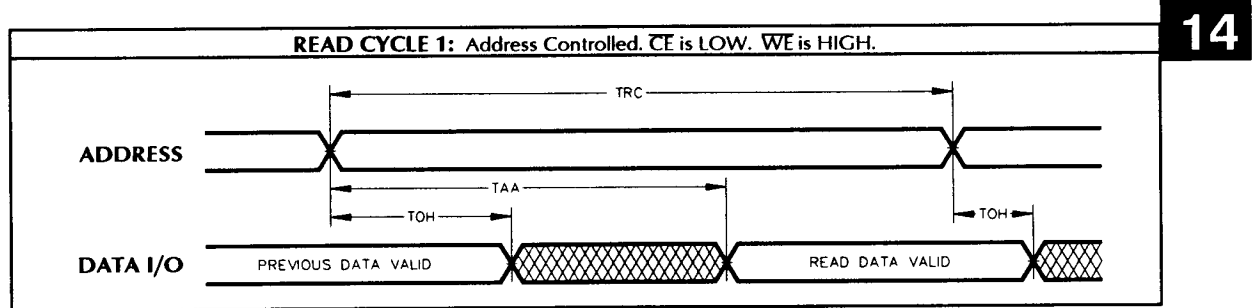
DC OPERATING CHARACTERISTICS: Over operating ranges

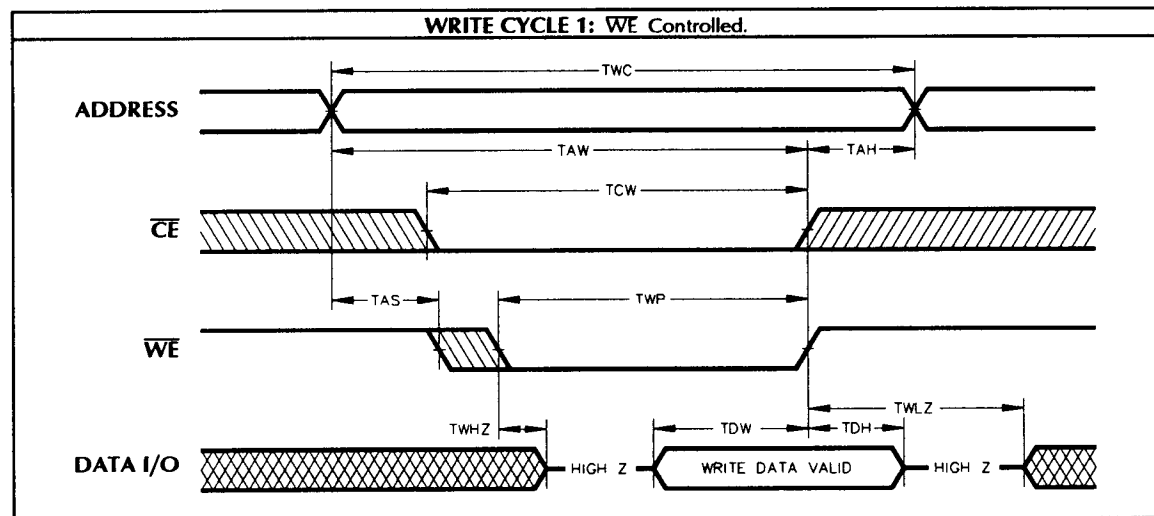
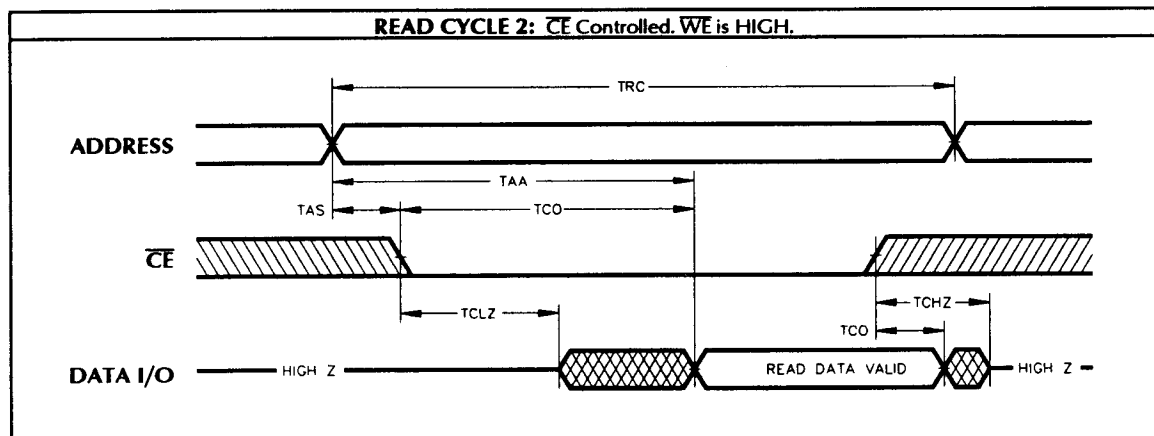
Symbol	Characteristics	Test Conditions	C		I		M/B		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
I _{IN}	Input Leakage Current	V _{IN} = 0V to V _{DD}	-20	+20	-20	+20	-20	+20	μA
I _{OUT}	Output Leakage Current	V _{I/O} = 0V to V _{DD} , CE = V _{IH} or WE = V _{IL}	-20	+20	-20	+20	-20	+20	μA
I _{CC1}	Active Supply Current	CE = V _{IL} , V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 0mA		220		250		280	mA
I _{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I _{OUT} = 0mA		290		310		370	mA
I _{SB1}	Full Standby Supply Current (CMOS)	V _{IN} ≤ 0.2V or V _{IN} ≥ V _{DD} - 0.2V, CE ≥ V _{DD} - 0.2V		15		20		3-0	mA
I _{SB2}	Standby Current (TTL)	CE = V _{IH} , V _{IN} = V _{IH} or V _{IL}		90		95		100	mA
V _{OL}	Output Low Voltage	I _{OUT} = 2.1mA		0.4		0.4		0.4	V
V _{OH}	Output High Voltage	I _{OUT} = -1.0mA	2.4		2.4		2.4		V

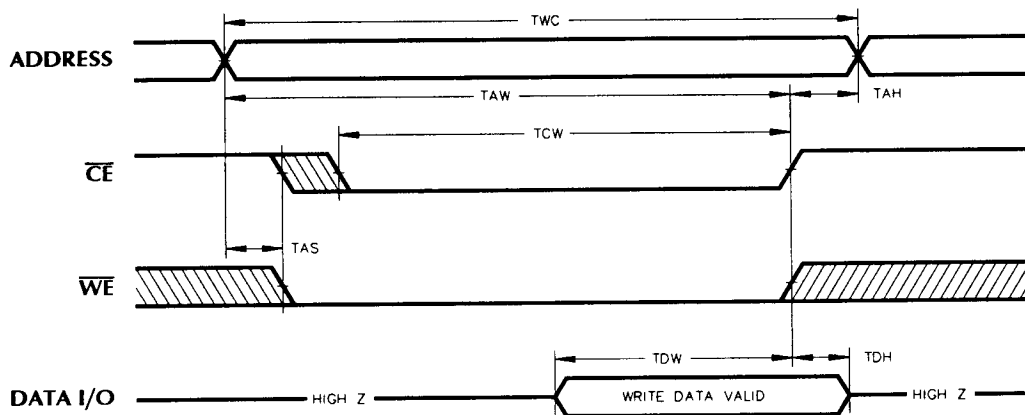
AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges											
No.	Symbol	Parameter	-25		-35		-45		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	trc	Read Cycle Time	25		35		45		55		ns
2	tAA	Address Access Time		25		35		45		55	ns
3	tCO	Chip Enable to Output Valid		25		35		45		55	ns
4	tOH	Output Hold from Address Change	5		5		5		5		ns
5	tCLZ	Chip Enable to Output in LOW-Z ^{4, 5}	5		5		5		5		ns
6	tCHZ	Chip Enable to Output in HIGH-Z ^{4, 5}	0	15	0	20	0	20	0	25	ns
7	tAS	Address Set-up Time *	0		0		0		0		ns
8	tOC	Output Hols from Chip Enable	0		0		0		0		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges ⁷											
No.	Symbol	Parameter	-25		-35		-45		-55		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
9	tWC	Write Cycle Time	25		35		45		55		ns
10	tAW	Address Valid to End of Write	20		30		40		50		ns
11	tCW	Chip Enable to End of Write	20		30		40		50		ns
12	tDW	Data Valid to End of Write	10		15		20		25		ns
13	tDH	Data Hold Time	3		3		3		3		ns
14	tWP	Write Pulse Width	20		30		40		50		ns
15	tAH	Address Hold Time	0		0		0		0		ns
16	tWHZ	Write Enable to Output in HIGH-Z ^{4, 5}	0	15	0	15	0	20	0	25	ns
17	tWLZ	Write Enable to Output in LOW-Z ^{4, 5}	5		5		5		5		ns

* Valid for both Read and Write cycles.





WRITE CYCLE 2: $\overline{CE}$ Controlled.

NOTES:

1. All voltages are with respect to V_{SS} .
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of $\pm 500\text{mV}$ from steady state voltage.
6. When $\overline{CE}$ is LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state, and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

WAVEFORM KEY

Data Valid

Transition from HIGH to LOW

Transition from LOW to HIGH

Data Undefined or Don't Care

ORDERING INFORMATION

DP S88H16 - XX X
PREFIX DEVICE TYPE SPEED GRADE

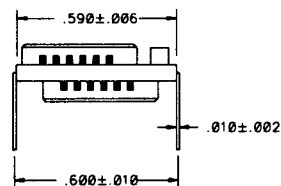
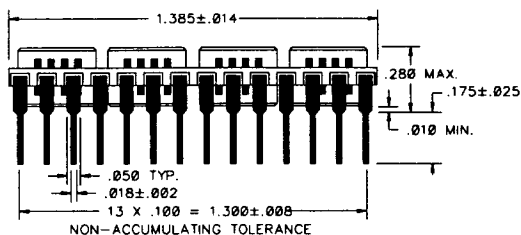
C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	-40°C to +85°C
M	MILITARY	-55°C to +125°C
B*	MIL-PROCESSED	-55°C to +125°C

25	25ns
35	35ns
45	45ns
55	55ns

16KX8 CMOS SRAM 28-PIN CERAMIC DIP

* B grade modules built with 883 devices.

MECHANICAL DRAWING



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