

1 Gigabit Synchronous DRAM

DPD256MX4XY5

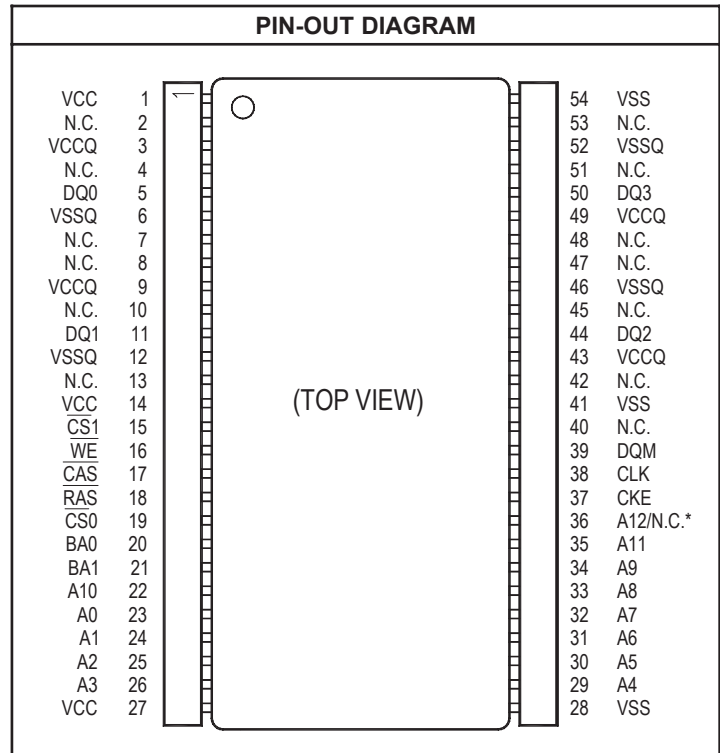
DESCRIPTION:

The Memory Stack™ series is a family of interchangeable memory devices. The 1 Gigabit Synchronous DRAM assembly utilizes the space saving LP-Stack™ technology to increase memory density. This stack is constructed with two 512Mb (128M x 4) SDRAMs.

This 1Gb LP-Stack™ has been designed to fit in the same footprint as the 512Mb (128M x 4) SDRAM TSOPII monolithic. This stack allows for system upgrade while providing an alternative low cost memory solution.

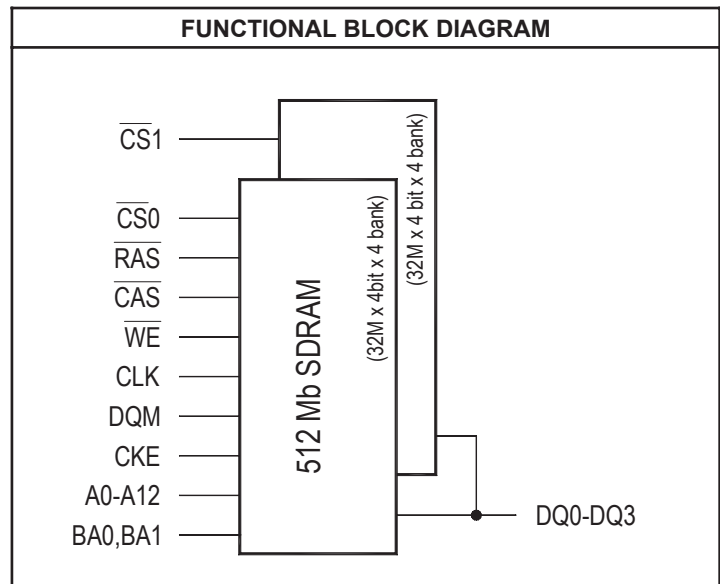
FEATURES:

- Electrical characteristics meet semiconductor manufacturers' datasheets
- Memory organization:
(2) 512Mb memory devices. Each device arranged as 128M x 4 bits (32M x 4 bits x 4 banks)
- Memory stack organization:
256M x 4 bits (64M x 4 bits x 4 banks)
- JEDEC approved, 2 Rank stack pinout and footprint (with 2 CSs, 1 CKE)
- Optimized for RDIMMs
- IPC-A-610, class 2, manufacturing standards
- Lead free manufacturing process
- Package: 54-Pin TSOPII stack



* N.C. on 4K Refresh Stacks.

PIN NAMES	
A0-A12	Row Address: A0-A12 Column Address: A0-A9, A11, A12
BA0, BA1	Bank Select Address
DQ0-DQ3	Data In/Data Out
CAS	Column Address Strobe
RAS	Row Address Strobe
WE	Data Write Enable
DQM	Data Input/Output Mask
CKE	Clock Enable
CLK	System Clock
CS0, CS1	Chip Selects
Vcc/Vss	Power Supply/Ground
Vccq/Vssq	Data Output Power/Ground
NC	No Connect



ORDERING INFORMATION												
DP PREFIX	SD TYPE	256M MEMORY DEPTH	X DESIG	4 MEMORY WIDTH	X DESIG	Y5 PACKAGE	- SUPPLIER	DP MFR ID	XX MEMORY REVISION	X CYCLE TIME	XXX	
												P12 PC100 / CL2
												P13 PC100 / CL3
												12 12ns (83MHz)
												10 10ns (100MHz)
												08 8ns (125MHz)
												75 7.5ns (133MHz) CL3
												75P2 7.5ns (133MHz) CL2
												70 7ns (143MHz) CL3
												70P2 7ns (133MHz) CL2
												60 6ns (166MHz) CL2
												55 5.5ns (183MHz) CL3
												BLANK REVISION NOT SPECIFIED
												n PER MANUFACTURER DIE REVISION
												MANUFACTURER CODE *
												SUPPLIER CODE*
												STACKABLE TSOP
												512 MEGABIT LVTTTL BASED
												MEMORY MODULE WITHOUT SUPPORT LOGIC
												SYNCHRONOUS DRAM

* Contact your sales representative for supplier and manufacturer codes.

NOTE:

1. AC Parameters of base memory are unchanged from device manufacturers' specifications.
2. DC Parameters may be affected by stacking. Please refer to application note 53A004-00 for further information.
3. For assembly and inspection procedures, refer to application note 53A001-00.
4. Maximum reflow temperature recommendation is 215°C.

