FAIRCHILD SEMICONDUCTOR®

January 2005

FMS6146
Low Cost Six Channel 4th Order Standard Definition Video Filter Driver

Features

- Six fourth-order 8MHz (SD) filters
- Transparent input clamping
- Dual video load drive (2Vpp, 75Ω)
- AC or DC-coupled inputs
- AC or DC-coupled outputs
- DC-coupled outputs eliminate AC-coupling capacitors
- 5V only
- Lead (Pb) Free TSSOP-14 package

Applications

- Cable set top boxes
- Satellite set top boxes
- DVD players
- HDTV
- Personal video recorders (PVR)
- Video on demand (VOD)

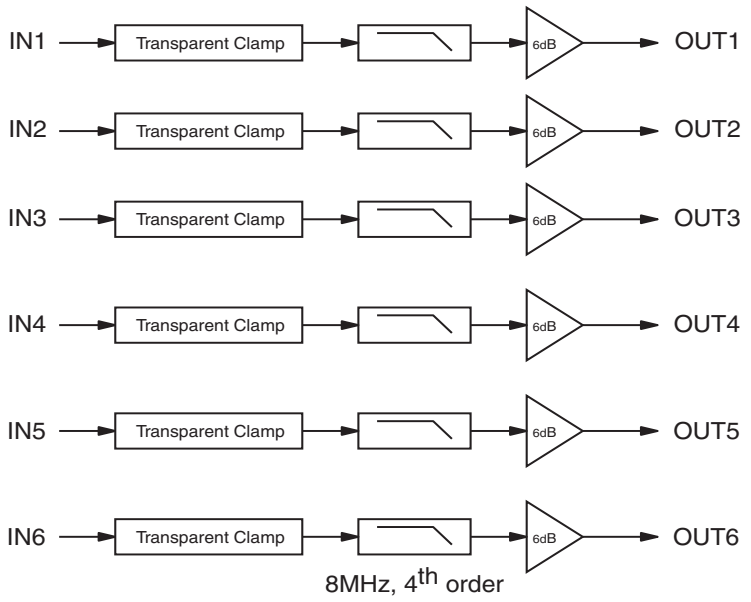
Description

The FMS6146 Low Cost Video Filter (LCVF) is intended to replace passive LC filters and drivers with a low-cost integrated device. Six 4th order filters provide improved image quality compared to typical 2nd or 3rd order passive solutions.

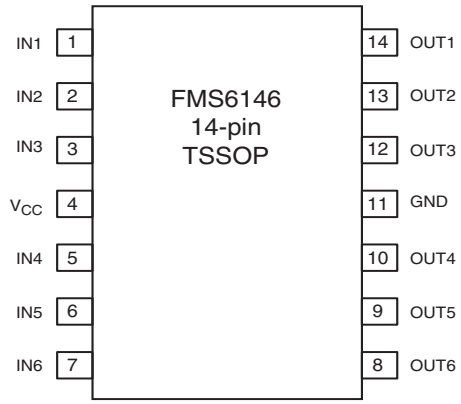
The FMS6146 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if AC-coupled inputs are required (see *Applications* section for details).

The outputs can drive AC or DC-coupled single (150Ω) or dual (75Ω) loads. DC-coupling the outputs removes the need for output coupling capacitors. The input DC levels will be offset approximately +280mV at the output (see *Applications* section for details).

Functional Block Diagram



Pin Configurations



Pin Assignments

Pin#	Pin	Type	Description
1	IN1	Input	Video input, Channel 1
2	IN2	Input	Video input, Channel 2
3	IN3	Input	Video input, Channel 3
4	V_{CC}	Input	+5V supply, do not float
5	IN4	Input	Video input, Channel 4
6	IN5	Input	Video input, Channel 5
7	IN6	Input	Video input, Channel 6
8	OUT6	Output	Filtered video output, Channel 6
9	OUT5	Output	Filtered video output, Channel 5
10	OUT4	Output	Filtered video output, Channel 4
11	GND	Output	Must be tied to ground, do not float
12	OUT3	Output	Filtered output, Channel 3
13	OUT2	Output	Filtered output, Channel 2
14	OUT1	Output	Filtered output, Channel 1

Reliability Information

Parameter	Min.	Typ.	Max.	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			300	°C
Thermal Resistance (θ_{JA}), JEDEC Standard Multi-Layer Test Boards, Still Air		90		°C/W

Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
DC Supply Voltage	-0.3	6	V
Analog and Digital I/O	-0.3	V_{CC} +0.3	V
Output Current Any One Channel, Do Not Exceed		50	mA

Recommemded Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range	0		70	°C
V_{CC} Range	4.75	5.0	5.25	V

DC Electrical Characteristics

Operating Conditions: (T_C = 25°C, V_{CC} = 5.0V, R_{source} = 37.5Ω, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω loads; unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
I_{CC}	Supply Current[1]	FMS6146 no load		35	55	mA
V_{IN}	Video Input Voltage Range	Referenced to GND if DC-coupled		1.4		V_{pp}
PSRR	Power Supply Rejection Ratio	DC (All Channels)		-50		dB

AC Electrical Characteristics

Operating Conditions: (T_C = 25°C, V_{IN} = 1V_{pp}, V_{CC} = 5.0V, R_{source} = 37.5Ω, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω loads; unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max	Units
AV	Channel Gain[1]	All Channels	5.6	6.0	6.6	dB
f_{1dB}	-1dB Bandwidth[1]	All Channels	4.5	6.8		MHz
f_c	-3dB Bandwidth	All Channels		7.8		MHz
f_{SB}	Attenuation (Stopband Reject)	All Channels at f = 27MHz		48		dB
dG	Differential Gain	All Channels		0.3		%
dϕ	Differential Phase	All Channels		0.6		°
THD	Output Distortion (All Channels)	V_{out} = 1.8V_{pp}, 1MHz		0.4		%
X_{TALK}	Crosstalk (Channel-to-Channel)	at 1MHz		-60		dB
SNR	Signal-to-Noise Ratio	All Channels, NTC-7 Weighting: 100kHz to 4.2MHz		75		dB
t_{pd}	Propagation Delay	Delay from Input-to-Output, 4.5MHz		59		ns

Notes:

1. 100% tested at 25°C

Typical Performance Characteristics

Operating Conditions: (T_C = 25°C, V_{CC} = 5.0V, R_{source} = 37.5Ω, all inputs AC coupled with 0.1µF, all outputs AC coupled with 220µF into 150Ω loads; unless otherwise noted)

Figure 1. Frequency Response

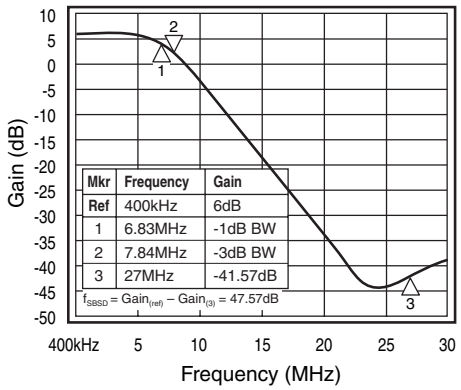


Figure 2. Group Delay vs. Frequency

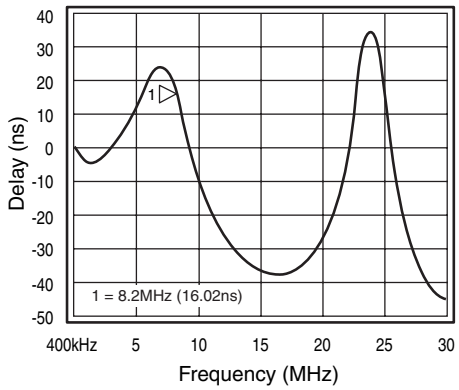


Figure 3. Noise vs. Frequency

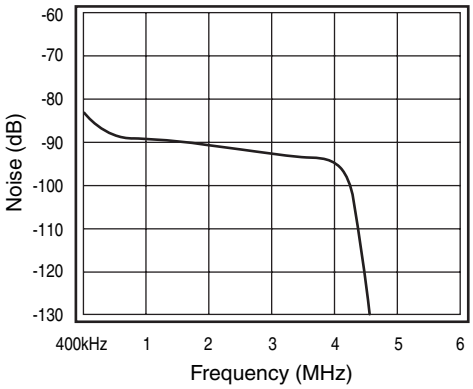


Figure 4. Differential Gain

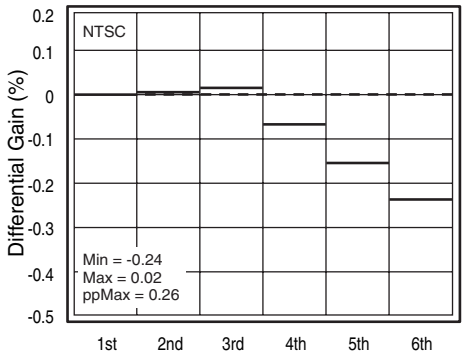
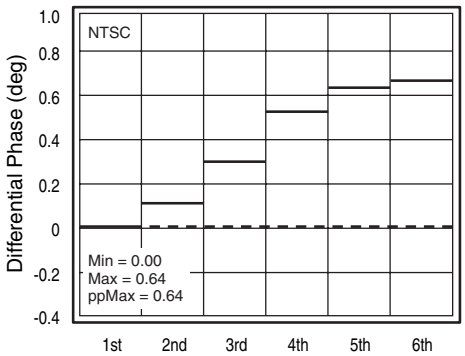


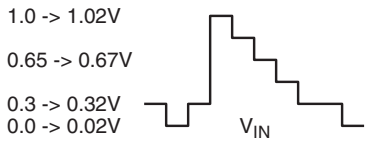
Figure 5. Differential Phase

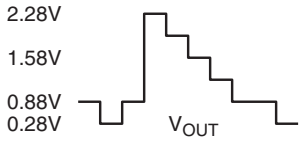


Applications Information

Application Circuits

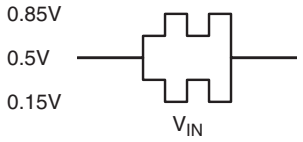
The FMS6146 Low Cost Video Filter (LCVF) provides 6dB gain from input to output. In addition, the input will be slightly offset to optimize the output driver performance. The offset is held to the minimum required value to decrease the standing DC current into the load. Typical voltage levels are shown in the diagram below:

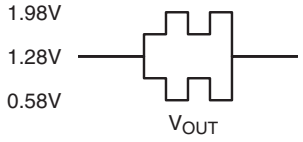




Driven by:
DC-Coupled DAC Outputs
AC-Coupled and Clamped
Y, CV, R, G, B

There will be a 280mV offset from the DC input level to the DC output level. $V_{OUT} = 2 * V_{IN} + 280mV$





Driven by:
AC-Coupled and Biased
U, V, Pb, Pr, C

Figure 6. Typical voltage levels

The FMS6146 provides an internal diode clamp to support AC-coupled input signals. If the input signal does not go below ground, the input clamp will not operate. This allows DAC outputs to directly drive the FMS6146 without an AC coupling capacitor. When the input is AC-coupled, the diode clamp will set the sync tip (or lowest voltage) just below ground. The worst-case sync tip compression due to the clamp will not exceed 7mV. The input level set by the clamp combined with the internal DC offset will keep the output within its acceptable range.

For symmetric signals like Chroma, U, V, Pb and Pr, the average DC bias is fairly constant and the inputs can be AC-coupled with the addition of a pull-up resistor to set the DC input voltage. DAC outputs can also drive these same signals without the AC

coupling capacitor. A conceptual illustration of the input clamp circuit is shown below:

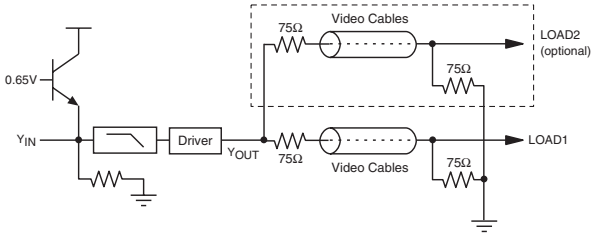


Figure 7. Input clamp circuit

I/O Configurations

For DC-coupled DAC drive with DC-coupled outputs, use this configuration:

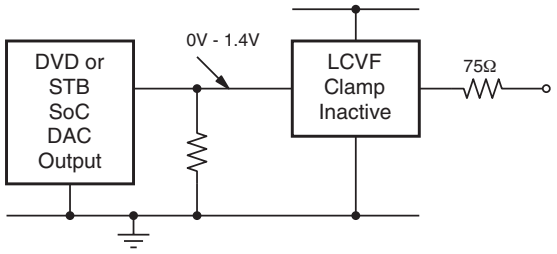


Figure 8. DC-coupled I/O configuration

Alternatively, if the DAC's average DC output level causes the signal to exceed the range of 0V to 1.4V, it can be AC-coupled as follows:

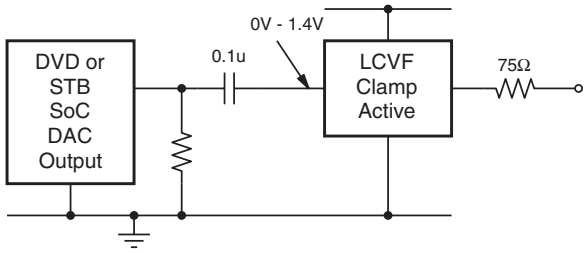


Figure 9. AC-coupled I/O configuration

When the FMS6146 is driven by an unknown external source or a SCART switch with its own clamping circuitry the inputs should be AC-coupled like this:

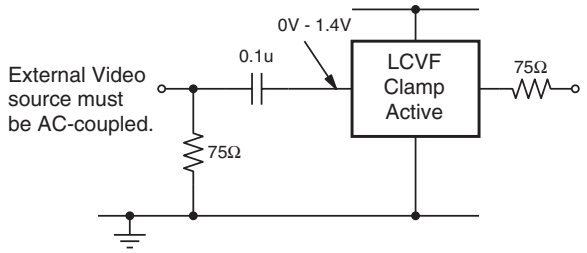


Figure 10. SCART I/O configuration

The same method can be used for biased signals with the addition of a pull-up resistor to make sure the clamp never operates. The internal pull-down resistance is 800kΩ ±20% so the external resistance should be 7.5MΩ to set the DC level to 500mV:

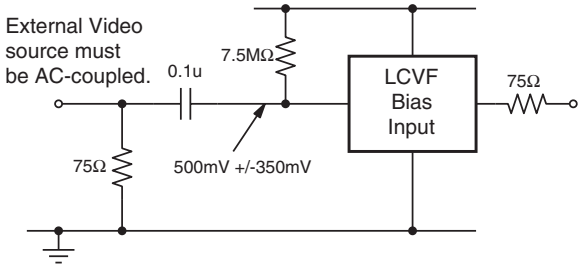


Figure 11. Biased SCART I/O configuration

The same circuits can be used with AC-coupled outputs if desired.

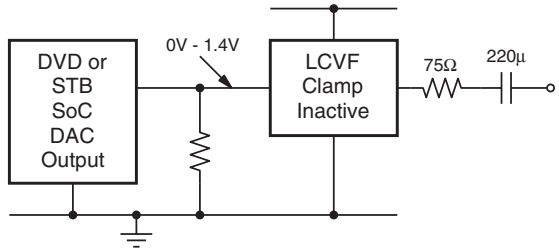


Figure 12. DC-coupled inputs, AC-coupled outputs

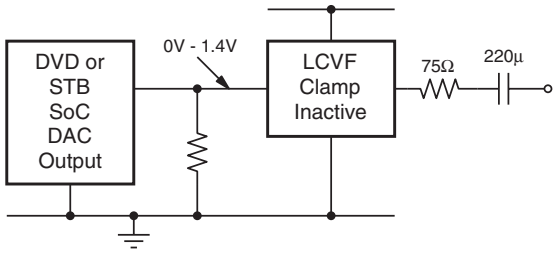


Figure 13. AC-coupled inputs and outputs

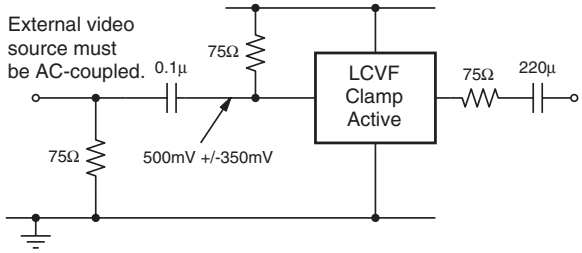


Figure 14. Biased AC-coupled inputs, AC-coupled outputs

NOTE: The video tilt or line time distortion will be dominated by the AC-coupling capacitor. The value may need to be increased beyond 220µF in order to obtain satisfactory operation in some applications.

Power Dissipation

The FMS6146 output drive configuration must be considered when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the FMS6146's power dissipation and internal temperature rise.

$T_j = T_A + P_d \bullet \theta_{JA}$

where: $P_d = P_{CH1} + P_{CH2} + P_{CH3}$ and $P_{CHx} = V_{CC} \bullet I_{CH} - (V_O^2/R_L)$

where: $V_O = 2V_{IN} + 0.280V$

$I_{CH} = (I_{CC}/6) + (V_O/R_L)$

V_{IN} = RMS value of input signal

I_{CC} = 35mA

V_{CC} = 5V

R_L = channel load resistance

Board layout can also affect thermal characteristics. Refer to the *Layout Considerations* section for more information.

The FMS6146 is specified to operate with output currents typically less than 50mA, more than sufficient for a dual (75Ω) video load. Internal amplifiers are current limited to a maximum of 100mA and should withstand brief duration short circuit conditions, however this capability is not guaranteed.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance and thermal characteristics. Fairchild offers a demonstration board, FMS6146DEMO, to use as a guide for layout and to aid in device testing and characterization. The FMS6146DEMO is a 4-layer board with a full power and ground plane. Following this layout configuration will provide the optimum performance and thermal characteristics. For optimum results, follow the steps below as a basis for high frequency layout:

- Include 1µF and 0.1µF ceramic bypass capacitors
- Place the 1µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- For multi-layer boards, use a large ground plane to help dissipate heat
- For 2 layer boards, use a ground plane that extends beyond the device by at least 0.5"
- Minimize all trace lengths to reduce series inductances

Typical Application Diagram

The following circuit may be used for direct DC-coupled drive by DACs with an output voltage range of 0V to 1.4V. AC-coupled or DC-coupled outputs may be used with AC-coupled outputs offering slightly lower power dissipation

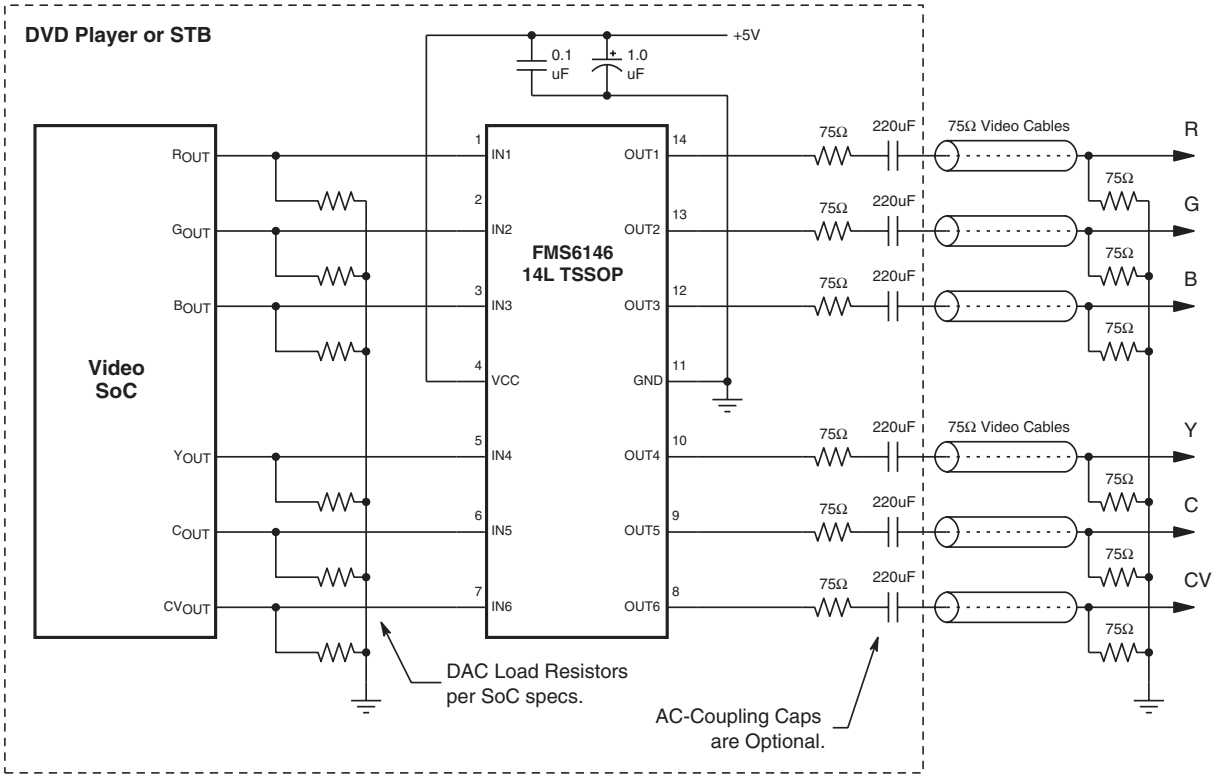
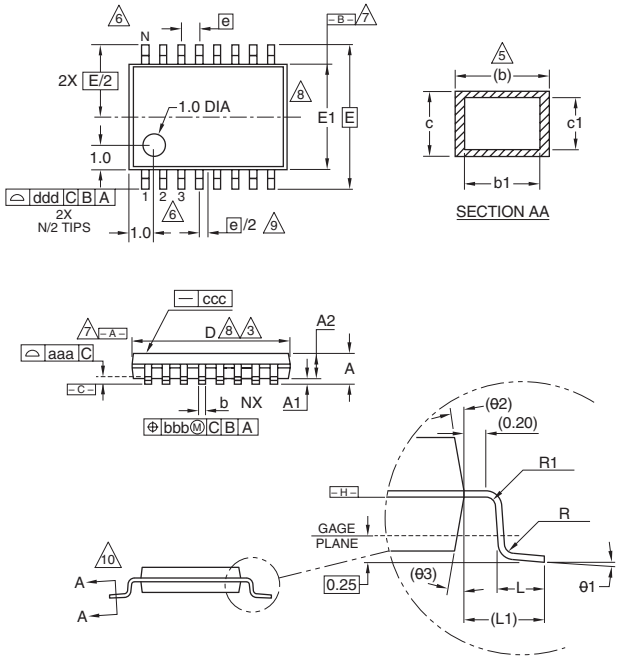


Figure 15. Typical application diagram

Mechanical Dimensions

14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC14



TSSOP-14			
SYMBOL	**MIN**	**NOM**	**MAX**
A	–	–	1.10
A1	0.05	–	0.15
A2	0.85	0.90	0.95
L	0.50	0.60	0.75
R	0.09	–	–
R1	0.09	–	–
b	0.19	–	0.30
b1	0.19	0.22	0.25
c	0.09	–	0.20
c1	0.09	–	0.16
θ1	0°	–	8°
L1	1.0 REF		
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.20		
e	0.65 BSC		
θ2	12° REF		
θ3	12° REF		
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.4 BSC		
e	0.65 BSC		
N	14		

NOTES:

1 All dimensions are in millimeters (angle in degrees).

2 Dimensioning and tolerancing per ASME Y14.5–1994.

3 Dimensions "D" does not include mold flash, protusions or gate burrs. Mold flash protusions or gate burrs shall not exceed 0.15 per side .

4 Dimension "E1" does not include interlead flash or protusion. Interlead flash or protusion shall not exceed 0.25 per side.

5 Dimension "b" does not include dambar protusion. Allowable dambar protusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. Dambar connot be located on the lower radius of the foot. Minimum space between protusion and adjacent lead is 0.07mm for 0.5mm pitch packages.

6 Terminal numbers are shown for reference only.

7 Datums – A – and – B – to be determined at datum plane – H –.

8 Dimensions "D" and "E1" to be determined at datum plane – H –.

9 This dimensions applies only to variations with an even number of leads per side. For variation with an odd number of leads per side, the "center" lead must be coincident with the package centerline, Datum A.

10 Cross sections A – A to be determined at 0.10 to 0.25mm from the leadtip.

Ordering Information

Model	Part Number	Lead Free	Package	Container	Pack Qty.
FMS6146	FMS6146MTC14_NL	Yes	TSSOP-14	Tube	94
FMS6146	FMS6146MTC14X_NL	Yes	TSSOP-14	Tape and Reel	2400

Temperature Range: 0°C to +70°C

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CoolFET™	FRFET™	MICROCOUPLER™	PowerSaver™	SuperSOT™-3
CROSSVOLT™	GlobalOptoisolator™	MicroFET™	PowerTrench®	SuperSOT™-6
DOME™	GTO™	MicroPak™	QFET®	SuperSOT™-8
EcoSPARK™	HiSeC™	MICROWIRE™	QS™	SyncFET™
E²CMOS™	I²C™	MSX™	QT Optoelectronics™	TinyLogic®
EnSigna™	*i-Lo*™	MSXPro™	Quiet Series™	TINYOPTO™
FACT™	ImpliedDisconnect™	OCX™	RapidConfigure™	TruTranslation™
FACT Quiet Series™		OCXPro™	RapidConnect™	UHC™
Across the board. Around the world.™		OPTOLOGIC®	µSerDes™	UltraFET®
The Power Franchise®		OPTOPLANAR™	SILENT SWITCHER®	UniFET™
Programmable Active Droop™		PACMAN™	SMART START™	VCX™

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. I15