32/36-bit Data Bus Dynamic RAM Card

MF14M1-L1XATXX
MF14M1-L2XATXX
MF18M1-L1XATXX
MF18M1-L2XATXX

Connector Type

Two-piece 88-pin

DESCRIPTION

These DRAM CARDs are developed based on JEIDA DRAM CARD GUIDELINE Ver. 2.0.
These cards are made using industry standard 1 M × 4 and 1 M × 1 Dynamic RAM and interface IC's in TSOP.

FEATURES

- All inputs except $\overline{RAS}$ inputs are buffered.
- Standard card size : 54mm (W) × 85.6mm (L) × 3.3mm (T)
- 88pin 2 piece connector type.
- $\overline{RAS}$ only refresh mode, $\overline{CAS}$ before $\overline{RAS}$ refresh mode and Page mode functions are available.
- Extended refresh is available. (128ms/1024cycle)

APPLICATIONS

Main/expansion memory unit for Personal Computer. Laser-Printer, FAX etc.

PRODUCT LIST

Product No. / Item / Type name	Memory capacity	Data Bus width (bits)	Access time (t_{RAC}) (ns)	Connector type	Number of pins	Outline drawing
No. 1 MF14M1-L17ATXX	4 MB	32 (without parity)	70	Two-piece	88	88P-001
No. 2 MF14M1-L18ATXX			80			
No. 3 MF14M1-L27ATXX		36 (with parity)	70			
No. 4 MF14M1-L28ATXX			80			
No. 5 MF18M1-L17ATXX	8 MB	32 (without parity)	70			
No. 6 MF18M1-L18ATXX			80			
No. 7 MF18M1-L27ATXX		36 (with parity)	70			
No. 8 MF18M1-L28ATXX			80			

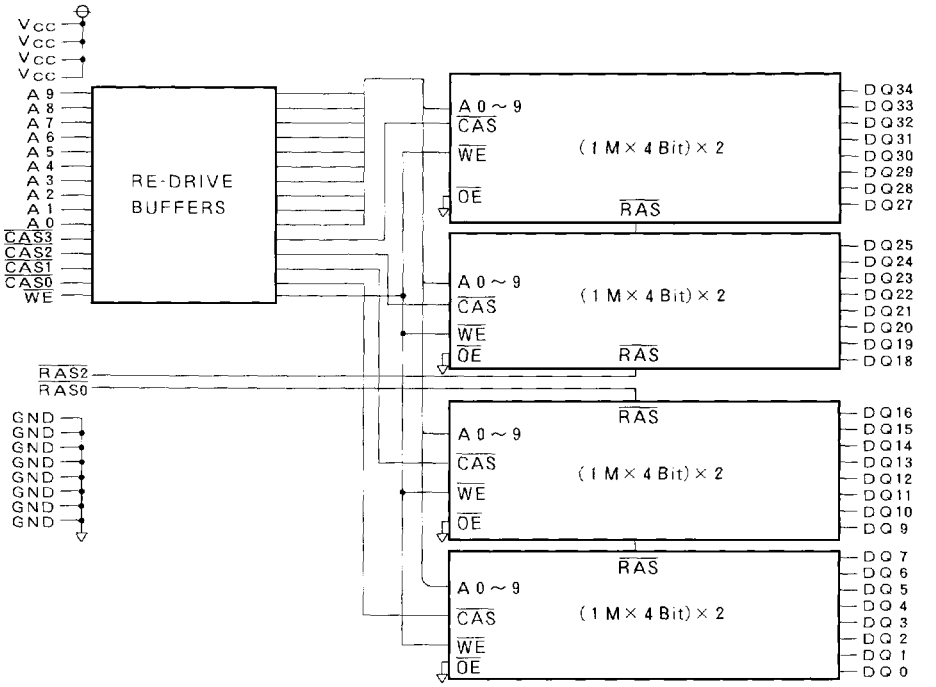
PIN ASSIGNMENT

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	45	GND	Ground
2	DQ 0	Data I/O	46	DQ18	Data I/O
3	DQ 1		47	DQ19	
4	DQ 2		48	DQ20	
5	DQ 3		49	DQ21	
6	DQ 4		50	DQ22	
7	DQ 5		51	DQ23	
8	DQ 6		52	DQ24	
9	Vcc	Power supply voltage	53	DQ25	
10	DQ7	Data I/O	54	DQ26	Data I/O (NC for No. 1, 2, 5, 6)
11	NC	No connection	55	NC	No connection
12	DQ 8	Data I/O (NC for No. 1, 2, 5, 6)	56	GND	Ground
13	A 0	Address input	57	A 1	Address input
14	A 2		58	A 3	
15	Vcc	Power supply voltage	59	A 5	
16	A 4	Address input	60	A 7	
17	NC	No connection	61	A 9	
18	A 6	Address input	62	NC	No connection
19	A 8		63	GND	Ground
20	NC	No connection	64	NC	No connection
21	NC		65	$\overline{RAS1}$	Row address strobe 1 (NC for No. 1, 2, 3, 4)
22	$\overline{RAS0}$	Row address strobe 0	66	$\overline{CAS2}$	Column address strobe 2
23	$\overline{CAS0}$	Column address strobe 0	67	GND	Ground
24	$\overline{CAS1}$	Column address strobe 1	68	$\overline{CAS3}$	Column address strobe 3
25	NC	No connection	69	$\overline{RAS3}$	Row address strobe 3 (NC for No. 1, 2, 3, 4)
26	$\overline{RAS2}$	Row address strobe 2	70	$\overline{WE}$	Write enable
27	Vcc	Power supply voltage	71	PD 1	Presence detect 1
28	PD 2	Presence detect 2	72	PD 3	Presence detect 3
29	PD 4	Presence detect 4	73	GND	Ground
30	PD 6	Presence detect 6	74	PD 5	Presence detect 5
31	NC	No connection	75	PD 7	Presence detect 7
32	NC		76	PD 8	Presence detect 8
33	DQ17	Data I/O (NC for No. 1, 2, 5, 6)	77	NC	No connection
34	DQ 9	Data I/O	78	NC	
35	NC	No connection	79	DQ35	Data I/O (NC for No. 1, 2, 5, 6)
36	DQ10	Data I/O	80	DQ27	Data I/O
37	Vcc	Power supply voltage	81	DQ28	
38	DQ11	Data I/O	82	DQ29	
39	DQ12		83	DQ30	
40	DQ13		84	DQ31	
41	DQ14		85	DQ32	
42	DQ15		86	DQ33	
43	DQ16		87	DQ34	
44	GND	Ground	88	GND	Ground

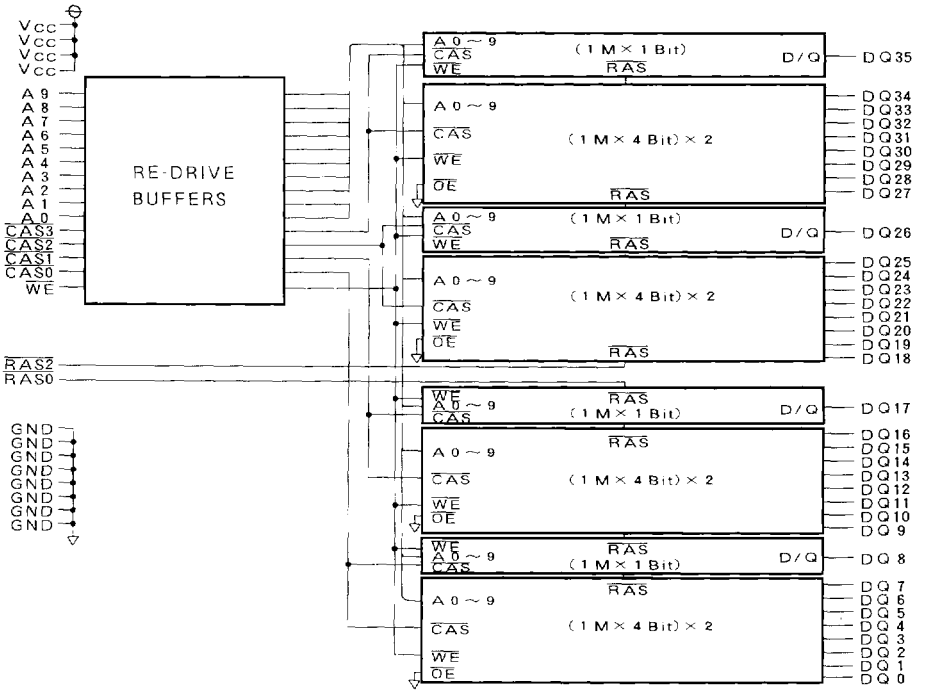
PD Pin Table

Product No.	PD 1	PD 2	PD 3	PD 4	PD 5	PD 6	PD 7	PD 8
No. 1, No. 3	GND	NC	GND	GND	NC	GND	NC	NC
No. 2, No. 4	GND	NC	GND	GND	NC	NC	GND	NC
No. 5, No. 7	GND	NC	GND	GND	GND	GND	NC	NC
No. 6, No. 8	GND	NC	GND	GND	GND	NC	GND	NC

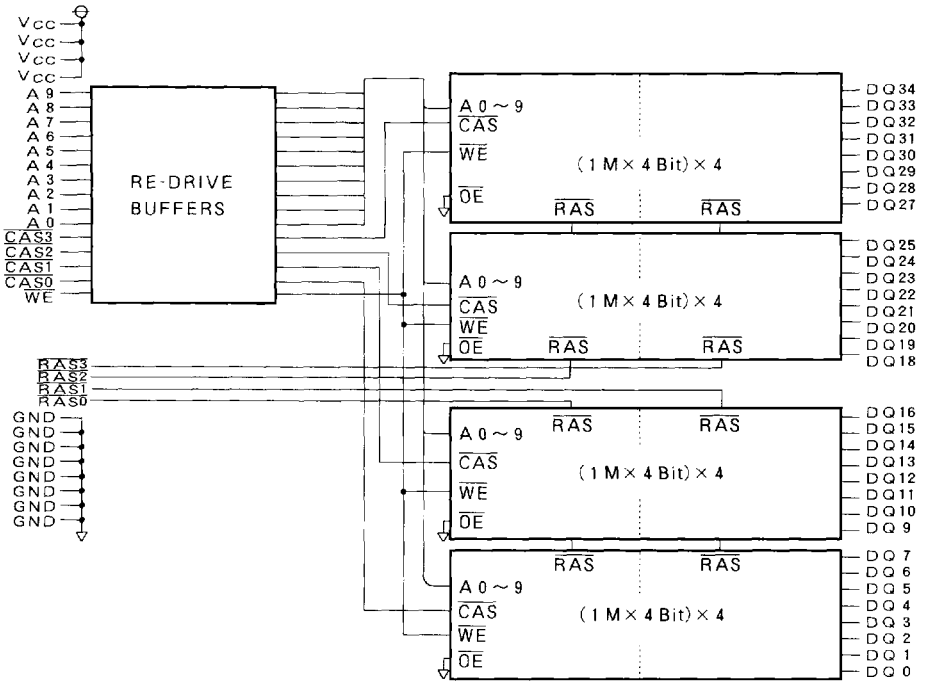
BLOCK DIAGRAM (No.1, 2)



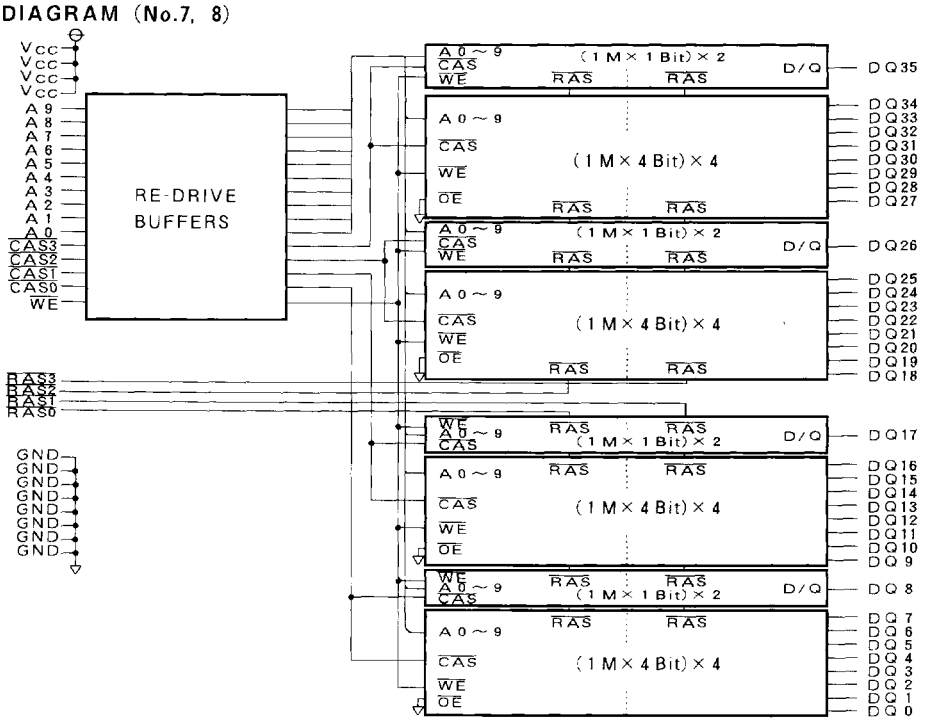
BLOCK DIAGRAM (No.3, 4)



BLOCK DIAGRAM (No.5, 6)



BLOCK DIAGRAM (No.7, 8)



FUNCTION TABLE

Operation	input					input/output		Refresh	Note
	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Row Address	Column Address	input	output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	Page mode indentical
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
$\overline{RAS}$ only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note 1 : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open
Don't be active more than two $\overline{RAS}$s at the same time.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	−0.5～7	V
V_I	Input voltage		−0.5～V_{CC}+0.5 (7V max.)	V
V_O	Output voltage		−0.5～7	V
I_O	Output current		50	mA
P_d	Power dissipation	T_a=25℃	8	W
T_{opr}	Operating temperature		0～55	℃
T_{stg}	Storage temperature		−40～80	℃

RECOMMENDED OPERATING CONDITIONS (T_a= 0～55℃, unless otherwise noted): (Note 2)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.75	5	5.25	V
GND	Supply voltage	0	0	0	V
V_{IL}	Low input voltage	0		0.8	V
V_{IH}	High input voltage	0.7×V_{CC}		V_{CC}	V

Note 2 : With respect to GND

ELECTRICAL CHARACTERISTICS (T_a = 0～55℃, V_{CC} = 5 V ± 5 %, GND = 0 V) : (Note 3)

Symbol	Parameter	Test condition	Limits														Unit
			Min.				Typ.	Max.									
			No. 1, No. 2	No. 3, No. 4	No. 5, No. 6	No. 7, No. 8		No. 1	No. 2	No. 3	No. 4	No. 5	No. 6	No. 7	No. 8	
V_{OH}	High output voltage	I_{OH} = − 5 mA	2.4					V_{CC}								V
V_{OL}	Low output voltage	I_{OL} = 4.2 mA	0					0.4								V
I_{OZ}	Off-stage output current	0 V ≦ V_{OUT} ≦ V_{CC}	−10	−10	−20	−20		10	10	10	10	20	20	20	20	μA
I_I	Input current	0 V ≦ V_{IN} ≦ V_{CC} Other input pins = 0 V	−40	−60	−40	−60		40	40	60	60	40	40	60	60	μA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating (Note 4, 5)	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = t_{WC} = min, output open						800	700	1120	980	820	730	1150	1010	mA
$I_{CC2(AV)}$	Supply current from V_{CC}, standby	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}, output open						20	20	28	28	36	36	52	52	mA
		$\overline{RAS}$ = $\overline{CAS}$ ≧ V_{CC} − 0.2 V, other input pins ≧ V_{CC} − 0.2 V or ≦ 0.2 V, output open						5	5	6	6	9	9	10	10	
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing (Note 4)	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min, output open						800	700	1120	980	820	730	1150	1010	mA
$I_{CC4(AV)}$	Average supply current from V_{CC}, Page-Mode (Note 4, 5)	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{RC} = min, output open						960	900	1240	1140	980	930	1270	1170	mA
$I_{CC6(AV)}$	Average supply current from V_{CC}, $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 4)	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling t_{RC} = min, output open						720	620	1040	900	740	650	1070	930	mA

Note 3 : Current flowing into a CARD is positive, out is negative.

4 : $I_{CC1(AV)}$, $I_{CC3(AV)}$, $I_{CC4(AV)}$ and $I_{CC6(AV)}$ are dependent on cycle rate. Specified values are obtained at the fastest cycle rate.

5 : $I_{CC1(AV)}$ and $I_{CC4(AV)}$ are dependent on output loading. Specified values are obtained with the outputs open.

SWITCHING CHARACTERISTICS (T_a = 0 ~55℃, V_{CC} = 5 V ± 5 %, GND = 0 V): (Note 6)

Symbol	Parameter	Limits				Unit
		No. 2, No. 4, No. 6, No. 8		No. 1, No. 3, No. 5, No. 7		
		Min.	Max.	Min.	Max.	
t_{CAC}	Access time from $\overline{CAS}$ (Note 7, 8)		30		27	ns
t_{RAC}	Access time from $\overline{RAS}$ (Note 7, 9)		80		70	ns
t_{CAA}	Column Address access time (Note 7, 10)		50		45	ns
t_{OFF}	Output disable time after $\overline{CAS}$ high (Note11)	0	30	0	25	ns

Note 6 : An initial pause of 500 μsec is required after power-up followed by any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles before proper device operation is achieved. Note that $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods of $\overline{RAS}$ inactivity before proper device operation is achieved.

7 : Measured with a load circuit equivalent to 2 TTL loads and 100pF.

8 : Assume that $t_{RCD} \geqq t_{RCD(max)}$ and $t_{ASC} \geqq t_{ASC(max)}$.

9 : Assume that $t_{RCD} \leqq t_{RCD(max)}$ and $t_{RAD} \leqq t_{RAD(max)}$.

10 : Assume that $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$.

11 : $t_{OFF(max)}$ define the time at which the output achieves the high impedance state ($|I_{out}| \leqq 10\,\mu A$ or $20\,\mu A$) and are not reference to $V_{OH(min)}$ or $V_{OL(max)}$.

TIMING REQUIREMENTS (T_a = 0 ~55℃, V_{CC} = 5 V ± 5 %, GND = 0 V): (Note 12, 13)

Symbol	Parameter	Limits				Unit
		No. 2, No. 4, No. 6, No. 8		No. 1, No. 3, No. 5, No. 7		
		Min.	Max.	Min.	Max.	
t_{REF}	Refresh cycle time (1024 cycles)		128		128	ms
t_{RP}	$\overline{RAS}$ high pulse width	70		60		ns
t_{RCD}	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (Note14)	20	50	20	43	ns
t_{CRP}	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low (Note15)	20		20		ns
t_{RPC}	Precharge to $\overline{CAS}$ active time	0		0		ns
t_{CPN}	$\overline{CAS}$ high pulse width	10		10		ns
t_{RAD}	Column address delay time from $\overline{RAS}$ low (Note16)	15	30	15	25	ns
t_{ASR}	Row address setup time before $\overline{RAS}$ low	10		10		ns
t_{ASC}	Column address setup time before $\overline{CAS}$ low (Note17)	5	15	5	13	ns
t_{RAH}	Row address hold time after $\overline{RAS}$ low	10		10		ns
t_{CAH}	Column address hold time after $\overline{CAS}$ low	15		15		ns
t_T	Transition time (Note18)	3	50	3	50	ns

Note 12 : The timing requirements are assumed t_T = 5 ns.

13 : $V_{IH(min)}$ and $V_{IL(max)}$ are reference levels for measuring timing of input signals.

14 : $t_{RCD(max)}$ is specified as a reference point only. If t_{RCD} is greater than $t_{RCD(max)}$, access time is defined as t_{CAC} and t_{CAA}.

15 : t_{CRP} requirement is applicable for all $\overline{RAS}/\overline{CAS}$ cycles.

16 : $t_{RAD(max)}$ is specified as reference point only. If $t_{RAD} \geqq t_{RAD(max)}$ and $t_{ASC} \leqq t_{ASC(max)}$, access time is assumed by t_{CAA} for read cycle.

17 : $t_{ASC(max)}$ is specified as a reference point only of address access time.

18 : t_T is measured between $V_{IH(min)}$ and $V_{IL(max)}$.

Read and Refresh Cycles

Symbol	Parameter	Limits				Unit
		No. 2, No. 4, No. 6, No. 8		No. 1, No. 3, No. 5, No. 7		
		Min.	Max.	Min.	Max.	
t_{RC}	Read cycle time	160		140		ns
t_{RAS}	$\overline{RAS}$ low pulse width	80	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	80		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	30		30		ns
t_{RCS}	Read Setup time before $\overline{CAS}$ low	5		5		ns
t_{RCH}	Read hold time after $\overline{CAS}$ high	0		0		ns
t_{RRH}	Read hold time after $\overline{RAS}$ high	10		10		ns

Write Cycle (Early Write)

Symbol	Parameter	Limits				Unit
		No. 2, No. 4, No. 6, No. 8		No. 1, No. 3, No. 5, No. 7		
		Min.	Max.	Min.	Max.	
t_{WC}	Write cycle time	160		140		ns
t_{RAS}	$\overline{RAS}$ low pulse width	80	10000	70	10000	ns
t_{CAS}	$\overline{CAS}$ low pulse width	20	10000	20	10000	ns
t_{CSH}	$\overline{CAS}$ hold time after $\overline{RAS}$ low	80		70		ns
t_{RSH}	$\overline{RAS}$ hold time after $\overline{CAS}$ low	30		30		ns
t_{WCS}	Write Setup time before $\overline{CAS}$ low	5		5		ns
t_{WCH}	Write hold time after $\overline{CAS}$ low	15		15		ns
t_{DS}	Data setup time	10		10		ns
t_{DH}	Data hold time after $\overline{CAS}$ low	25		25		ns

Page Mode Cycle (Read, Early Write)

Symbol	Parameter	Limits				Unit
		No. 2, No. 4, No. 6, No. 8		No. 1, No. 3, No. 5, No. 7		
		Min.	Max.	Min.	Max.	
t_{PC}	Read, Write cycle time	60		55		ns
t_{CP}	$\overline{CAS}$ high pulse width (Note 19)	10	20	10	18	ns
t_{RAS}	$\overline{RAS}$ low pulse width	140	100000	125	100000	ns

Note 19 : $t_{CP(max)}$ is specified as a reference point only.

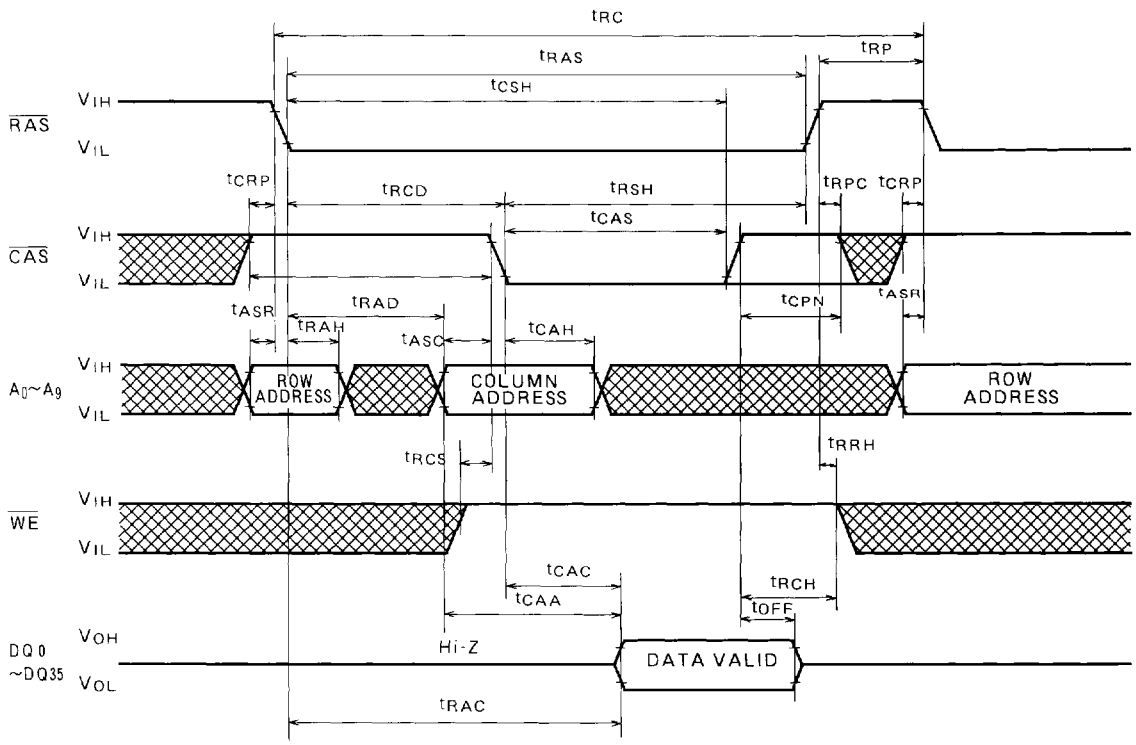
$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 20)

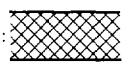
Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_{CSR}	$\overline{CAS}$ setup time for $\overline{CAS}$ before $\overline{RAS}$ refresh	20		ns
t_{CHR}	$\overline{CAS}$ hold time for $\overline{CAS}$ before $\overline{RAS}$ refresh	15		ns

Note 20 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

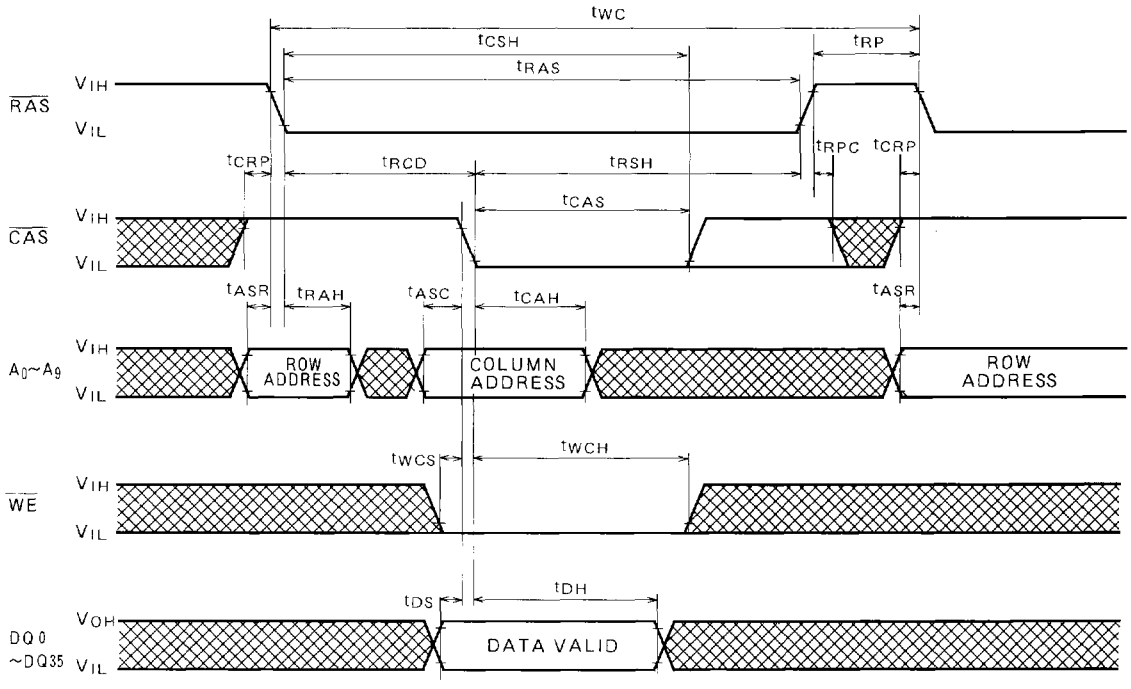
TIMING DIAGRAMS (Note 21)

Read Cycle

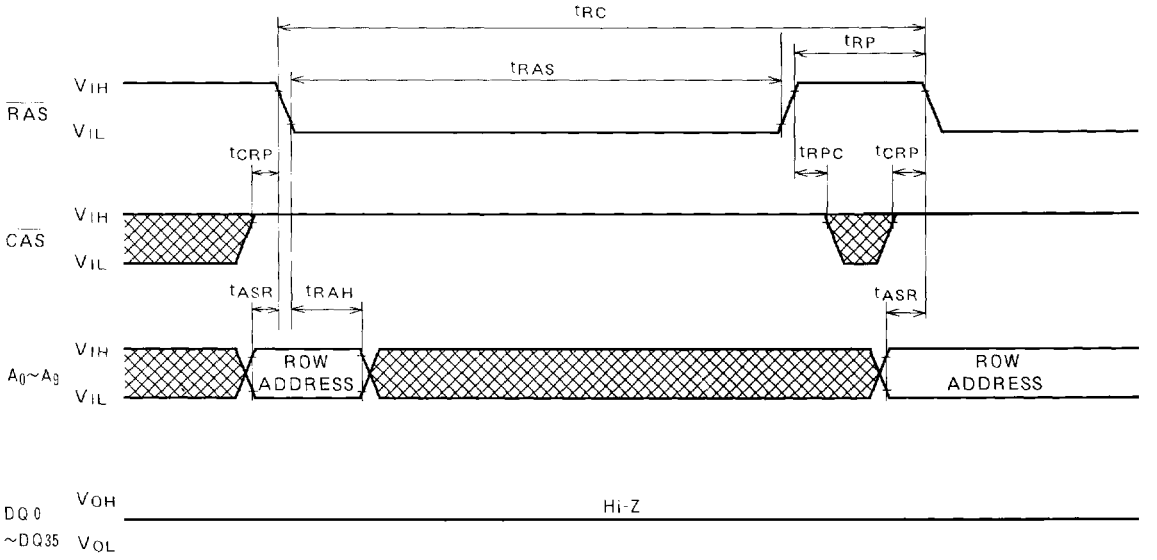


Note 21 :  Indicates the don't care input.

Early Write Cycle

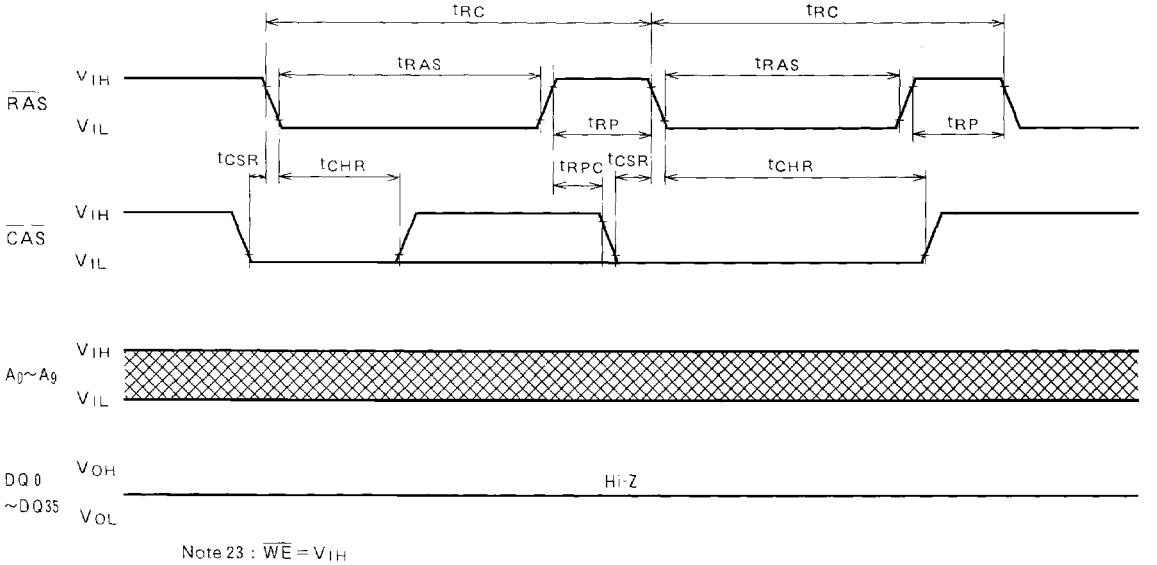


$\overline{RAS}$ only Refresh Cycle (Note 22)



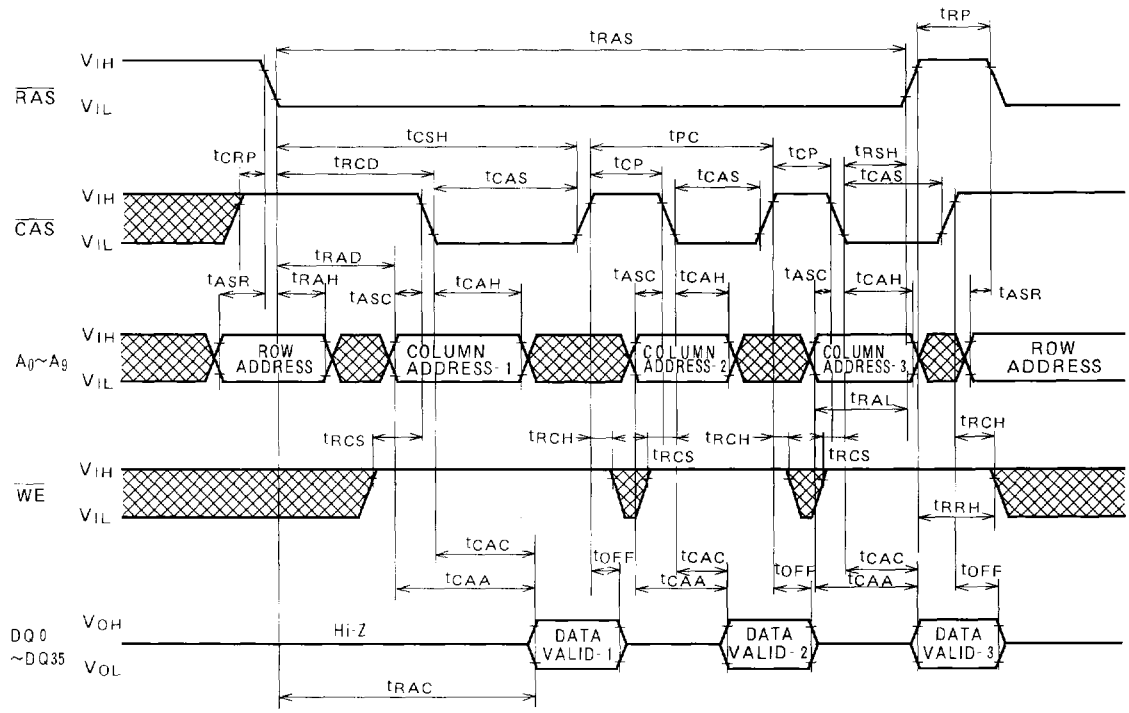
Note 22 : $\overline{WE}$ = don't care.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 23)



Note 23 : $\overline{WE}$ = V_{IH}

Page-Mode Read Cycle



Page-Mode Early Write Cycle