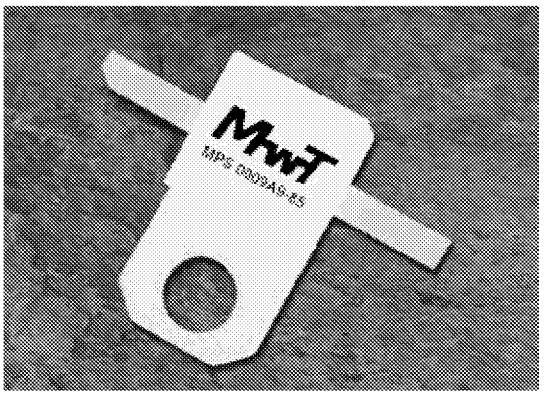
MPS-0909A9-85

925 to 960 MHz Low Noise Receiver Amplifier

Features

- Very Low Noise 1.1 dB Typical
- High +36 dBm Typical IP3
- 16 dB Typical Gain
- 6.0 Volt Bias
- 26% High Power Added Efficiency



Description

The MPS-0909A9-85 is a low noise, high dynamic range amplifier designed for PDC receiver applications. The circuit is matched to 50 Ω and employs a single stage GaAs FET with internal matching to provide exceptional noise figure, 1.1 dB combined with extremly high IP3, +36 dBm. Typical applications are base station receivers, Tower mounted LNA's, smart antenna systems and receiver multi-couplers.

Electrical Specifications at 25°C, V_{dd} = 6.0 V, Zo = 50 Ω

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Freq	Frequency Range	925		960	MHz
SSG	Small Signal Gain	14	16		dB
P1dB	Pout at 1 dB Compression		+22.0		dBm
IP3	Third-order Intercept[1]	+33.0	+36.0		dBm
NF	Noise Figure		1.1	1.5	dB
VSWR	Input/Output VSWR		2.0:1	2.5:1	
ΔGOF	Gain Variation over Frequency		±0.2	±0.5	dB
ΔGOT	Gain Variation over Temperature		-.015		dB/°C
I_{dd}	DC Current		180	250	mA
PAE	Power Added Efficiency		26		%

[1] Two tone tests at +5 dBm per tone output.

Absolute Maximum Ratings

Maximum Bias Voltage	7.0 V
Maximum Continuous RF Input Power	240 mW
Maximum Peak Input Power	360 mW
Maximum Case Operating Temperature	+85°C
Maximum Storage Temperature	-65°C to +150°C

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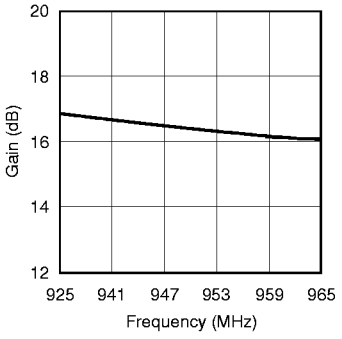
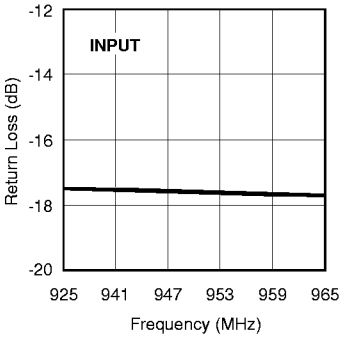
Typical Performance at +25°C

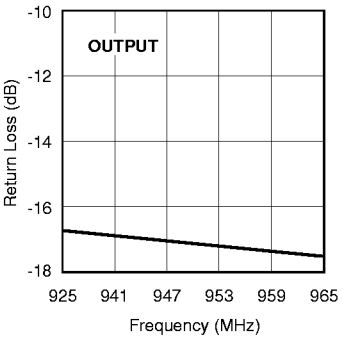
Gain vs. Frequency



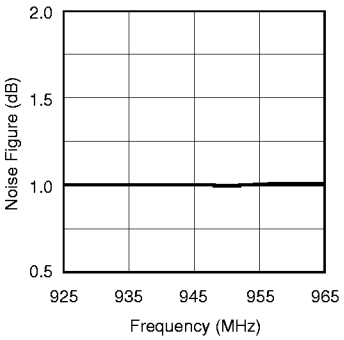
Return Loss vs. Frequency



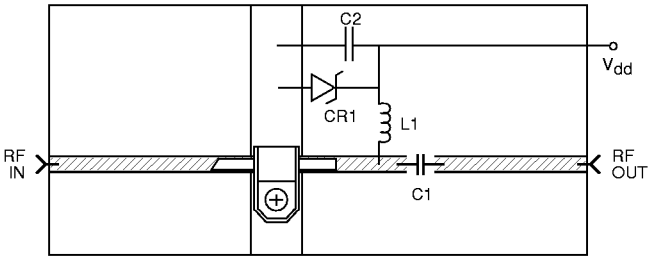
Return Loss vs. Frequency



Noise Figure vs. Frequency



Application Circuit

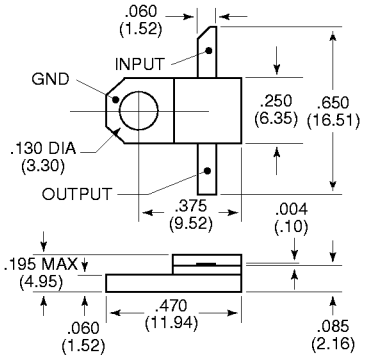


C1	100 pF	Chip Capacitor
C2	.22 µF	Capacitor
L1	160 nH	Printed or Wound Coil
CR1	7.0 V	Zener Diode
		50 Ω Microstrip Line

Board material FR-4 or equivalent.

Outline Diagram

Half Flange Package (-85)



Dimensions in inches and (mm)

Ordering Information

Part Number	Package/Evaluation Board
MPS-0909A9-85	Half Flange Package
MPS-0909A9-85EV	Half Flange Package on Evaluation Board

< Previous Product | Table of Contents | Next Product >

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