



# SYNCHRONOUS DRAM MODULE

## MT9LSDT3272A - 256MB MT18LSDT6472A - 512MB

For the latest data sheet, please refer to the Micron Web site: [www.micron.com/datasheets](http://www.micron.com/datasheets)

### FEATURES

- PC133- and PC100-compliant
- JEDEC-standard 168-pin, dual in-line memory module (DIMM)
- Utilizes 125 MHz and 133 MHz SDRAM components
- Unbuffered
- ECC-optimized pinout
- 256MB (32 Meg x 72) and 512MB (64 Meg x 72)
- Single +3.3V ±0.3V power supply
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal SDRAM banks for hiding row access/ precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Precharge and Auto Refresh Modes
- Self Refresh Mode
- 64ms, 8,192-cycle refresh
- LVTTTL-compatible inputs and outputs
- Serial Presence-Detect (SPD)

### OPTIONS

- Package  
168-pin DIMM (gold)  
Unbuffered
- Frequency/CAS Latency  
133 MHz/CL = 2 -13E  
133 MHz/CL = 3 -133  
100 MHz/CL = 2 -10E

### MARKING

G  
A

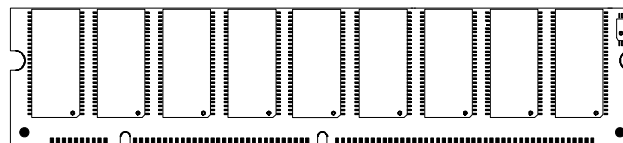
### DEVICE TIMING

Module Markings	PC100 CL - 'RCD - 'RP	PC133 CL - 'RCD - 'RP
-13E	2 - 2 - 2	2 - 2 - 2
-133	2 - 2 - 2	3 - 3 - 3
-10E	2 - 2 - 2	NA

### ADDRESS TABLE

	256MB Module	512MB Module
Refresh Count	8K	8K
Device Banks	4 (BA0, BA1)	4 (BA0, BA1)
Device Configuration	32 Meg x 8	32 Meg x 8
Row Addressing	8K (A0-A12)	8K (A0-A12)
Column Addressing	1K (A0-A9)	1K (A0-A9)
Module Banks	1 (S0,S2)	2 (S0,S2; S1,S3)

### PIN ASSIGNMENT (Front View) 168-Pin DIMM



PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
1	V <sub>SS</sub>	43	V <sub>SS</sub>	85	V <sub>SS</sub>	127	V <sub>SS</sub>
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	S2#	87	DQ33	129	S3#
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V <sub>DD</sub>	48	NC	90	V <sub>DD</sub>	132	NC
7	DQ4	49	V <sub>DD</sub>	91	DQ36	133	V <sub>DD</sub>
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V <sub>SS</sub>	54	V <sub>SS</sub>	96	V <sub>SS</sub>	138	V <sub>SS</sub>
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V <sub>DD</sub>	101	DQ45	143	V <sub>DD</sub>
18	V <sub>DD</sub>	60	DQ20	102	V <sub>DD</sub>	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	CKE1	105	CB4	147	NC
22	CB1	64	V <sub>SS</sub>	106	CB5	148	V <sub>SS</sub>
23	V <sub>SS</sub>	65	DQ21	107	V <sub>SS</sub>	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	V <sub>DD</sub>	68	V <sub>SS</sub>	110	V <sub>DD</sub>	152	V <sub>SS</sub>
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	S0#	72	DQ27	114	S1#	156	DQ59
31	NC	73	V <sub>DD</sub>	115	RAS#	157	V <sub>DD</sub>
32	V <sub>SS</sub>	74	DQ28	116	V <sub>SS</sub>	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V <sub>SS</sub>	120	A7	162	V <sub>SS</sub>
37	A8	79	CK2	121	A9	163	CK3
38	A10	80	NC	122	BA0	164	NC
39	BA1	81	WP	123	A11	165	SA0
40	V <sub>DD</sub>	82	SDA	124	V <sub>DD</sub>	166	SA1
41	V <sub>DD</sub>	83	SCL	125	CK1	167	SA2
42	CK0	84	V <sub>DD</sub>	126	A12	168	V <sub>DD</sub>



## PART NUMBERS

PART NUMBER	CONFIGURATION	SYSTEMBUS SPEED
MT9LSDT3272AG-13E_	32 Meg x 72	133 MHz
MT9LSDT3272AG-133_	32 Meg x 72	133 MHz
MT9LSDT3272AG-10E_	32 Meg x 72	100 MHz
MT18LSDT6472AG-13E_	64 Meg x 72	133 MHz
MT18LSDT6472AG-133_	64 Meg x 72	133 MHz
MT18LSDT6472AG-10E_	64 Meg x 72	100 MHz

**NOTE:** The designators for component and PCB revision are the last two characters of each part number. Consult factory for current revision codes. Example: MT18LSDT6472AG-133B1.

## GENERAL DESCRIPTION

The MT9LSDT3272A and MT18LSDT6472A are high-speed CMOS, dynamic random-access, 256MB and 512MB memories organized in a x72 (ECC) configuration. These modules use internally configured quad-bank SDRAMs with a synchronous interface (all signals are registered on the positive edge of the clock signals CK0-CK3).

Read and write accesses to the SDRAM modules are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed (BA0, BA1 select the device bank, A0-A12 select the device row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The modules provide for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

The modules use an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the  $2n$  rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one device bank while accessing one of the other three device banks will hide the precharge cycles and provide seamless, high-speed, random-access operation.

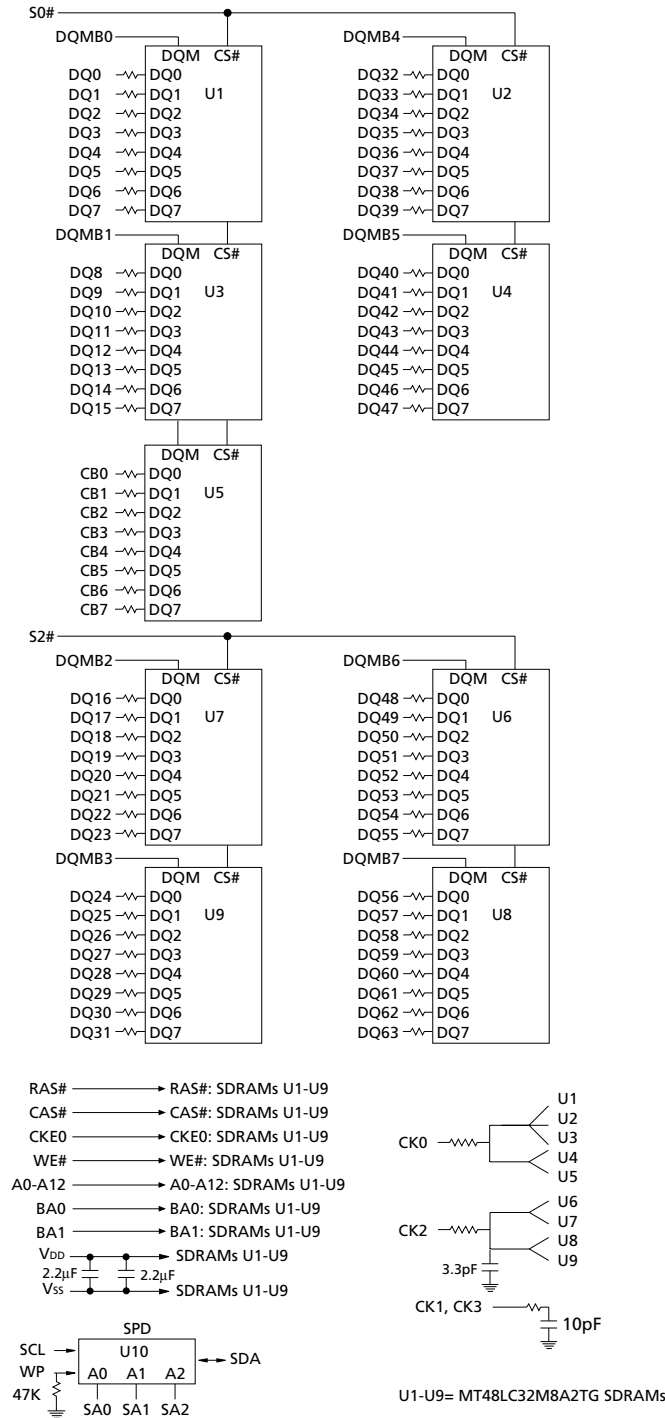
The modules are designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to syn-chronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal device banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding SDRAM operation, refer to the 256Mb SDRAM data sheet.

## SERIAL PRESENCE-DETECT OPERATION

These modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

### FUNCTIONAL BLOCK DIAGRAM MT9LSDT3272A (256MB)

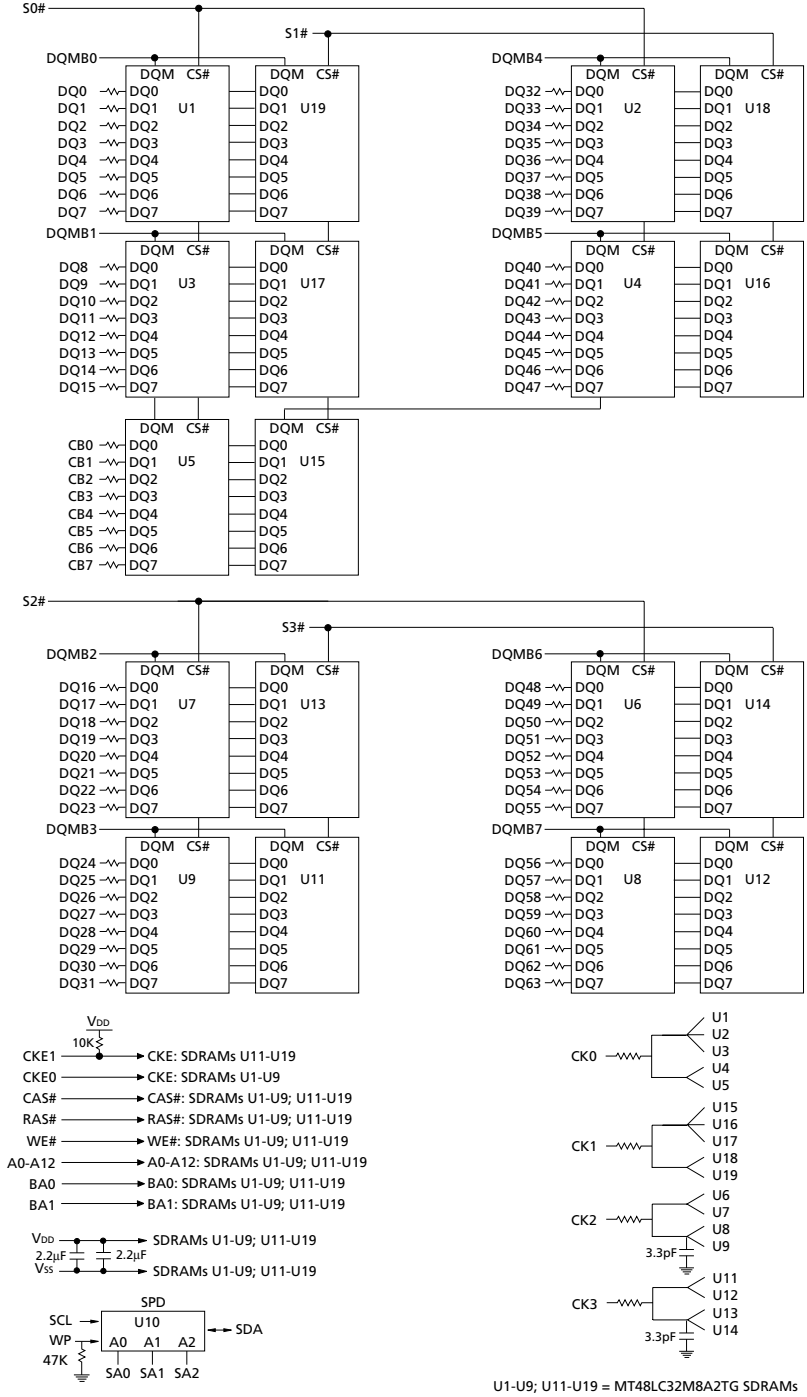


- NOTE:**
1. All resistor values are 10 ohms unless otherwise specified.
  2. Reference designators in this diagram do not necessarily match the actual module.



256MB / 512MB (x72, ECC) 168-PIN SDRAM DIMMs

FUNCTIONAL BLOCK DIAGRAM MT18LSDT3272A (512MB)



**NOTE:** 1. All resistor values are 10 ohms unless otherwise specified.  
 2. Reference designators in this diagram do not necessarily match the actual module.


**PIN DESCRIPTIONS**

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
27, 111, 115	RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS#, and WE# (along with S0#-S3#) define the command being entered.
42, 79, 125, 163	CK0-CK3	Input	Clock: CK0-CK3 are driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
63, 128	CKE1, CKE0	Input	Clock Enable: CKE0-CKE1 activate (HIGH) and deactivate (LOW) the CK0-CK3 signals. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all device banks idle), ACTIVE POWER-DOWN (row ACTIVE in any device bank) or CLOCK SUSPEND operation (burst access in progress). CKE0-CKE1 are synchronous except after the device enters power-down and self refresh modes, where CKE0-CKE1 become asynchronous until after exiting the same mode. The input buffers, including CK0-CK3, are disabled during power-down and self refresh modes, providing low standby power.
30, 45, 114, 129	S0#-S3#	Input	Chip Select: S0#-S3# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0#-S3# are registered HIGH. S0#-S3# are considered part of the command code.
28-29, 46-47, 112-113, 130-131	DQMB0-DQMB7	Input	Input/Output Mask: DQMB is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQMB is sampled HIGH during a READ cycle.
39, 122	BA0, BA1	Input	Bank Address: BA0 and BA1 define to which device bank the ACTIVE, READ, WRITE, or PRECHARGE command is being applied.
33, 34, 35, 36, 37, 38, 117, 118, 119, 120, 121, 123, 126	A0-A12	Input	Address Inputs: A0-A12 are sampled during the ACTIVE command (row-address A0-A12) and READ/WRITE command (column-address A0-A9, with A10 defining auto precharge) to select one location out of the memory array in the respective device bank. A10 is sampled during a PRECHARGE command to determine if all device banks are to be precharged (A10 HIGH) or device bank selected by BA0, BA1 (LOW). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
81	WP	Input	Write Protect: Serial presence-detect hardware write protect.
83	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.


**PIN DESCRIPTIONS (continued)**

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
165-167	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
2-5, 7-11, 13-17, 19-20, 55-58, 60, 65-67, 69-72, 74-77, 86-89, 91-95, 97-101, 103-104, 139-142, 144, 149-151, 153-156, 158-161	DQ0-DQ63	Input/ Output	Data I/O: Data bus.
21, 22, 52, 53, 105, 106, 136, 137	CB0-CB7	Input/ Output	Check Bits.
82	SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
1, 12, 23, 32, 43, 54, 64, 68, 78, 85, 96, 107, 116, 127, 138, 148, 152, 162	V <sub>SS</sub>	Supply	Ground.
6, 18, 26, 40, 41, 49, 59, 73, 84, 90, 102, 110, 124, 133, 143, 157, 168	V <sub>DD</sub>	Supply	Power Supply: +3.3V ±0.3V.
24, 25 31, 44, 48 61, 62, 80, 108, 109, 134, 135, 145-147, 164	NC	–	Not Connected: These pins are not connected on this module.



## SDRAM FUNCTIONAL DESCRIPTION

In general, the 256Mb SDRAMs are quad-bank DRAMs that operate at 3.3V and include a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). The four banks of the x8 configured devices used for these modules are configured as 8,192 bit-rows by 1,024 bit-columns, by 8 input/output bits.

Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the device bank and row to be accessed; BA0 and BA1 select the device bank, A0–A12 select the device row. The address bits A0–A9 registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

Prior to normal operation, the SDRAM must be initialized. The following sections provide detailed information covering device initialization, register definition, command descriptions and device operation.

### Initialization

SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Once power is applied to V<sub>DD</sub> and V<sub>DDQ</sub> (simultaneously) and the clock is stable (stable clock is defined as a signal cycling within timing constraints specified for the clock pin), the SDRAM requires a 100µs delay prior to issuing any command other than a COMMAND INHIBIT or NOP. Starting at some point during this 100µs period and continuing at least through the end of this period, COMMAND INHIBIT or NOP commands should be applied.

Once the 100µs delay has been satisfied with at least one COMMAND INHIBIT or NOP command having been applied, a PRECHARGE command should be applied. All device banks must then be precharged, thereby placing the device in the all banks idle state.

Once in the idle state, two AUTO REFRESH cycles must be performed. After the AUTO REFRESH cycles are complete, the SDRAM is ready for mode register programming. Because the mode register will power up in an unknown state, it should be loaded prior to applying any operational command.

## Register Definition

### MODE REGISTER

The mode register is used to define the specific mode of operation of the SDRAM. This definition includes the selection of a burst length, a burst type, a CAS latency, an operating mode and a write burst mode, as shown in the Mode Register Definition Diagram (Pg. 8). The mode register is programmed via the LOAD MODE REGISTER command and will retain the stored information until it is programmed again or the device loses power.

Mode register bits M0–M2 specify the burst length, M3 specifies the type of burst (sequential or interleaved), M4–M6 specify the CAS latency, M7 and M8 specify the operating mode, M9 specifies the write burst mode, and M10 and M11 are reserved for future use. Address A12 (M12) is undefined but should be driven LOW during loading of the mode register.

The mode register must be loaded when all device banks are idle, and the controller must wait the specified time before initiating the subsequent operation. Violating either of these requirements will result in unspecified operation.

### Burst Length

Read and write accesses to the SDRAM are burst oriented, with the burst length being programmable, as shown in the Mode Register Definition Diagram (Pg. 8). The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 1, 2, 4, or 8 locations are available for both the sequential and the interleaved burst types, and a full-page burst is available for the sequential type. The full-page burst is used in conjunction with the BURST TERMINATE command to generate arbitrary burst lengths.

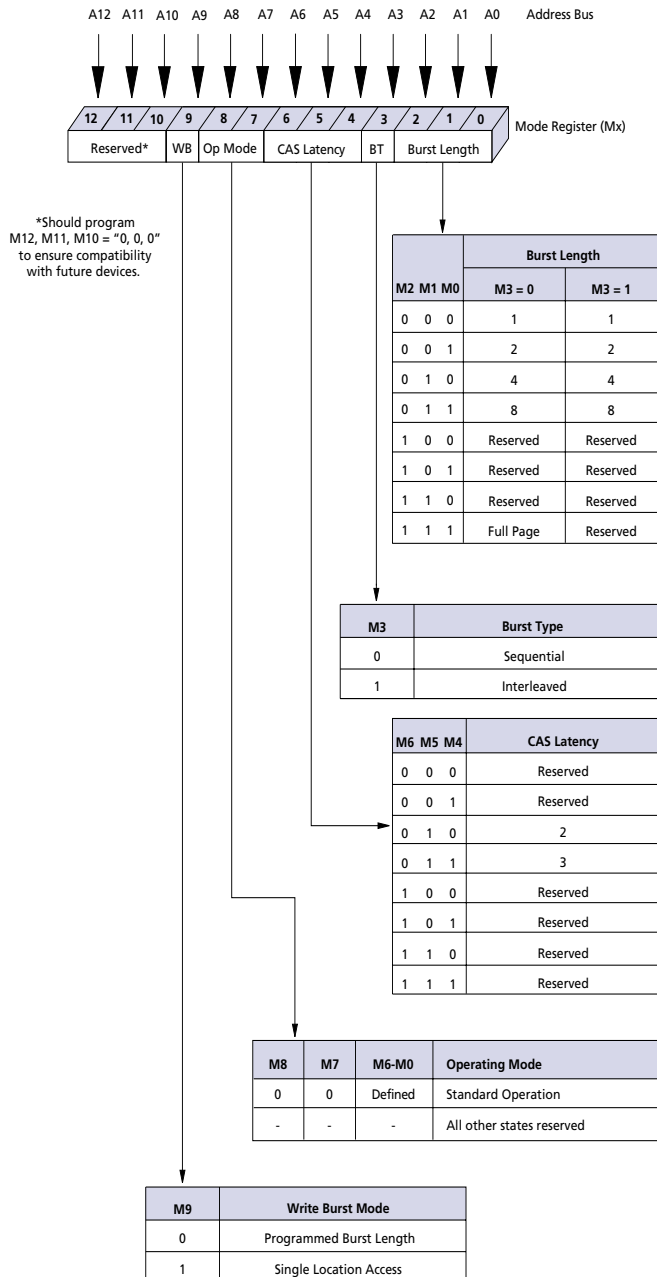
Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached, as shown in the Burst Definition Table (Pg. 8). The block is uniquely selected by A1–A9 when the burst length is set to two; by A2–A9 when the burst length is set to four; and by A3–A9 when the burst length is set to eight. The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. Full-page bursts wrap within the page if the boundary is reached, as shown in the Burst Definition Table (Pg. 8).

### Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit M3.

The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in the Burst Definition Table.



### Mode Register Definition Diagram

### Burst Definition Table

Burst Length	Starting Column Address:	Order of Accesses Within a Burst	
		Type = Sequential	Type = Interleaved
2	<b>A0</b>		
	0	0-1	0-1
	1	1-0	1-0
4	<b>A1 A0</b>		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	<b>A2 A1 A0</b>		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1	
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (y)	n = A0-A11/9/8 (location 0-y)	Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... ...Cn - 1, Cn...	Not supported

- NOTE:**
- For full-page accesses:  $y = 1,024$ .
  - For a burst length of two, A1-A9 select the block-of-two burst; A0 selects the starting column within the block.
  - For a burst length of four, A2-A9 select the block-of-four burst; A0-A1 select the starting column within the block.
  - For a burst length of eight, A3-A9 select the block-of-eight burst; A0-A2 select the starting column within the block.
  - For a full-page burst, the full row is selected and A0-A9 select the starting column.
  - Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
  - For a burst length of one, A0-A9 select the unique column to be accessed, and mode register bit M3 is ignored.





**CAS Latency**

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first piece of output data. The latency can be set to two or three clocks.

If a READ command is registered at clock edge  $n$ , and the latency is  $m$  clocks, the data will be available by clock edge  $n + m$ . The DQs will start driving as a result of the clock edge one cycle earlier ( $n + m - 1$ ), and provided that the relevant access times are met, the data will be valid by clock edge  $n + m$ . For example, assuming that the clock cycle time is such that all relevant access times are met, if a READ command is registered at  $T_0$  and the latency is programmed to two clocks, the DQs will start driving after  $T_1$  and the data will be valid by  $T_2$ , as shown in the CAS Latency Diagram. The CAS Latency Table indicates the operating frequencies at which each CAS latency setting can be used.

Reserved states should not be used as unknown operation or incompatibility with future versions may result.

**Operating Mode**

The normal operating mode is selected by setting M7 and M8 to zero; the other combinations of values for M7 and M8 are reserved for future use and/or test modes. The programmed burst length applies to both READ and WRITE bursts.

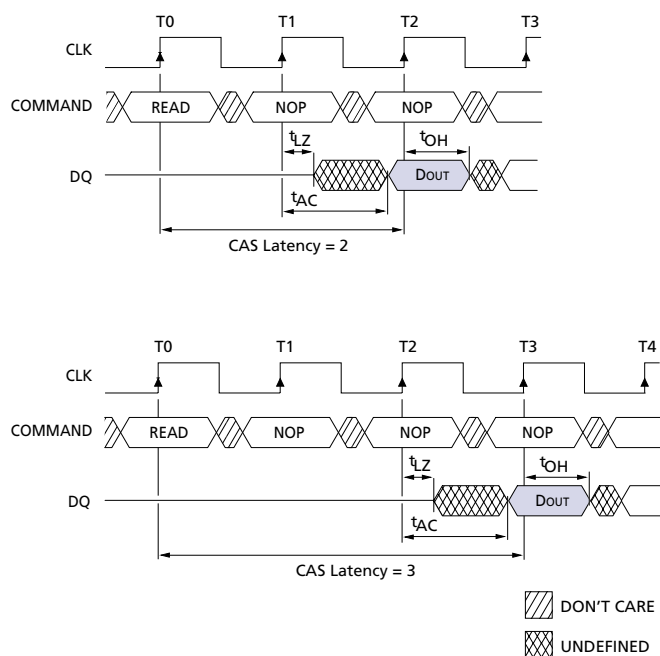
Test modes and reserved states should not be used because unknown operation or incompatibility with future versions may result.

**Write Burst Mode**

When M9 = 0, the burst length programmed via M0-M2 applies to both READ and WRITE bursts; when M9 = 1, the programmed burst length applies to READ bursts, but write accesses are single-location (nonburst) accesses.

**CAS Latency Table**

SPEED	ALLOWABLE OPERATING FREQUENCY (MHz)	
	CAS LATENCY = 2	CAS LATENCY = 3
-13E	≤ 133	≤ 143
-133	≤ 100	≤ 133
-10E	≤ 100	≤ 125



**CAS Latency Diagram**



## COMMANDS

The Truth Table provides a quick reference of available commands. This is followed by written description of each command. For a more detailed description

of commands and operations, refer to the 256Mb SDRAM component data sheet.

## TRUTH TABLE – SDRAM Commands and DQMB Operation

(Note: 1, notes appear below table)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	L/H <sup>8</sup>	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	L/H <sup>8</sup>	Bank/Col	Valid	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (Enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	2
Write Enable/Output Enable	–	–	–	–	L	–	Active	8
Write Inhibit/Output High-Z	–	–	–	–	H	–	High-Z	8

- NOTE:**
1. CKE is HIGH for all commands shown except SELF REFRESH.
  2. A0-A11 define the op-code written to the mode register, and A12 should be driven LOW
  3. A0-A12 provide row address, and BA0, BA1 determine which device bank is made active.
  4. A0-A9 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent), while A10 LOW disables the auto precharge feature; BA0, BA1 determine which device bank is being read from or written to.
  5. A10 LOW: BA0, BA1 determine which device bank is being precharged. A10 HIGH: all device banks are precharged and BA0, BA1 are "Don't Care."
  6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
  7. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care" except for CKE.
  8. Activates or deactivates the DQs during WRITES (zero-clock delay) and READs (two-clock delay).



## 256MB / 512MB (x72, ECC) 168-PIN SDRAM DIMMs

### ABSOLUTE MAXIMUM RATINGS\*

Voltage on V <sub>DD</sub> , V <sub>DDQ</sub> Supply	
Relative to V <sub>SS</sub> .....	-1V to +4.6V
Voltage on Inputs, NC or I/O Pins	
Relative to V <sub>SS</sub> .....	-1V to +4.6V
Operating Temperature,	
T <sub>A</sub> .....	0°C to +70°C
Storage Temperature (plastic) .....	-55°C to +150°C
Power Dissipation, 256MB .....	9W
Power Dissipation, 512MB .....	18W

\*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS - 256MB Module

(Notes: 1, 5, 6; notes appear following parameter tables); (V<sub>DD</sub>, V<sub>DDQ</sub> = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V <sub>DD</sub> , V <sub>DDQ</sub>	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V <sub>IH</sub>	2	V <sub>DD</sub> + 0.3	V	22
INPUT LOW VOLTAGE: Logic 0; All inputs	V <sub>IL</sub>	-0.3	0.8	V	22
INPUT LEAKAGE CURRENT: Any input 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> (All other pins not under test = 0V)	I <sub>I</sub>	-45	45	μA	
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub>	I <sub>OZ</sub>	-5	5	μA	
OUTPUT LEVELS: Output High Voltage (I <sub>OUT</sub> = -4mA)	V <sub>OH</sub>	2.4	-	V	
Output Low Voltage (I <sub>OUT</sub> = 4mA)	V <sub>OL</sub>	-	0.4	V	

### DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS - 512MB Module

(Notes: 1, 5, 6; notes appear following parameter tables); (V<sub>DD</sub>, V<sub>DDQ</sub> = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SUPPLY VOLTAGE	V <sub>DD</sub> , V <sub>DDQ</sub>	3	3.6	V	
INPUT HIGH VOLTAGE: Logic 1; All inputs	V <sub>IH</sub>	2	V <sub>DD</sub> + 0.3	V	22
INPUT LOW VOLTAGE: Logic 0; All inputs	V <sub>IL</sub>	-0.3	0.8	V	22
INPUT LEAKAGE CURRENT: Any input 0V ≤ V <sub>IN</sub> ≤ V <sub>DD</sub> (All other pins not under test = 0V)	I <sub>I</sub>	-90	90	μA	
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V <sub>OUT</sub> ≤ V <sub>DDQ</sub>	I <sub>OZ</sub>	-10	10	μA	
OUTPUT LEVELS: Output High Voltage (I <sub>OUT</sub> = -4mA)	V <sub>OH</sub>	2.4	-	V	
Output Low Voltage (I <sub>OUT</sub> = 4mA)	V <sub>OL</sub>	-	0.4	V	


**I<sub>DD</sub> SPECIFICATIONS AND CONDITIONS\*: 256MB Module**

(Notes: 1, 5, 6, 11, 13; notes appear following the parameter tables);

 (V<sub>DD</sub>, V<sub>DDQ</sub> = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES	
		-13E	-133	-10E			
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; t <sub>RC</sub> = t <sub>RC</sub> (MIN)	I <sub>DD1</sub>	1,188	1,143	1,143	mA	3, 18, 19, 30	
STANDBY CURRENT: Power-Down Mode; All banks idle; CKE = LOW	I <sub>DD2</sub>	18	18	18	mA	30	
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All banks active after t <sub>RCD</sub> met; No accesses in progress	I <sub>DD3</sub>	423	423	423	mA	3, 12, 19, 30	
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active	I <sub>DD4</sub>	1,233	1,233	1,233	mA	3, 18, 19, 30	
AUTO REFRESH CURRENT CKE = HIGH; CS# = HIGH	t <sub>RFC</sub> = t <sub>RFC</sub> (MIN)	I <sub>DD5</sub>	2,565	2,430	2,430	mA	3, 12, 18, 19, 30, 31
	t <sub>RFC</sub> = 7.81μs	I <sub>DD6</sub>	36	36	36	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V	STANDARD	I <sub>DD7</sub>	23	23	23	mA	4

\*DRAM Components only.

**I<sub>DD</sub> SPECIFICATIONS AND CONDITIONS\*: 512MB Module**

(Notes: 1, 6, 11, 13; notes appear following parameter tables)

 (V<sub>DD</sub>, V<sub>DDQ</sub> = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES	
		-13E	-133	-10E			
OPERATING CURRENT: Active Mode; Burst = 2; READ or WRITE; t <sub>RC</sub> = t <sub>RC</sub> (MIN)	I <sub>DD1</sub> <sup>†</sup>	1,188	1,143	1,143	mA	3, 18, 19, 30	
STANDBY CURRENT: Power-Down Mode; All banks idle; CKE = LOW	I <sub>DD2</sub> <sup>‡</sup>	36	36	36	mA	30	
STANDBY CURRENT: Active Mode; CKE = HIGH; CS# = HIGH; All banks active after t <sub>RCD</sub> met; No accesses in progress	I <sub>DD3</sub> <sup>†</sup>	423	423	423	mA	3, 12, 19, 30	
OPERATING CURRENT: Burst Mode; Continuous burst; READ or WRITE; All banks active	I <sub>DD4</sub> <sup>†</sup>	1,233	1,233	1,233	mA	3, 18, 19, 30	
AUTO REFRESH CURRENT CS# = HIGH; CKE = HIGH	t <sub>RFC</sub> = t <sub>RFC</sub> (MIN)	I <sub>DD5</sub> <sup>‡</sup>	5,130	4,860	4,860	mA	3, 12, 18, 19, 30, 31
	t <sub>RFC</sub> = 7.81 μs	I <sub>DD6</sub> <sup>‡</sup>	72	72	72	mA	
SELF REFRESH CURRENT: CKE ≤ 0.2V	STANDARD	I <sub>DD7</sub> <sup>‡</sup>	45	45	45	mA	4

\*DRAM components only.

†Value calculated as one module bank in this operating condition, and all other module banks in Power-Down Mode.

‡Value calculated reflects all module banks in this operating condition.



## CAPACITANCE

(Note 2; notes appear following parameter tables)

PARAMETER	SYMBOL	256MB		512MB		UNITS
		MIN	MAX	MIN	MAX	
Input Capacitance: A0-A12, BA0, BA1, RAS#, CAS#, WE#	C <sub>11</sub>	22.5	34.2	45	68.4	pF
Input Capacitance: CK0-CK1	C <sub>12<sub>a</sub></sub>	12.5	17.5	12.5	17.5	pF
Input Capacitance: CK2-CK3	C <sub>12<sub>b</sub></sub>	13.3	17.3	13.3	17.3	pF
Input Capacitance: S0#-S1#	C <sub>13<sub>a</sub></sub>	12.5	19	12.5	19	pF
Input Capacitance: S2#-S3#	C <sub>13<sub>b</sub></sub>	10	15.2	10	15.2	pF
Input Capacitance: CKE0, CKE1	C <sub>14</sub>	22.5	34.2	22.5	34.2	pF
Input Capacitance: DQMB0, 2-4, 6, 7	C <sub>15<sub>a</sub></sub>	2.5	3.8	5	7.6	pF
Input Capacitance: DQMB1, DQMB5	C <sub>15<sub>b</sub></sub>	5	7.6	7.5	11.4	pF
Input/Output Capacitance: SCL, SA0-SA2, SDA	C <sub>16</sub>	–	10	–	10	pF
Input/Output Capacitance: DQ0-DQ63, CB0-CB7	C <sub>10</sub>	4	6	8	12	pF


**ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

(Notes: 5, 6, 8, 9, 11; notes appear following parameter tables)

AC CHARACTERISTICS			-13E		-133		-10E		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX			
Access time from CLK (pos. edge)	CL = 3 CL = 2	$t_{AC(3)}$ $t_{AC(2)}$		5.4 5.4		5.4 6		6 6	ns	27
Address hold time		$t_{AH}$	0.8		0.8		1		ns	
Address setup time		$t_{AS}$	1.5		1.5		2		ns	
CLK high-level width		$t_{CH}$	2.5		2.5		3		ns	
CLK low-level width		$t_{CL}$	2.5		2.5		3		ns	
Clock cycle time	CL = 3 CL = 2	$t_{CK(3)}$ $t_{CK(2)}$	7 7.5		7.5 10		8 10		ns	23 23
CKE hold time		$t_{CKH}$	0.8		0.8		1		ns	
CKE setup time		$t_{CKS}$	1.5		1.5		2		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		$t_{CMH}$	0.8		0.8		1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		$t_{CMS}$	1.5		1.5		2		ns	
Data-in hold time		$t_{DH}$	0.8		0.8		1		ns	
Data-in setup time		$t_{DS}$	1.5		1.5		2		ns	
Data-out high-impedance time	CL = 3 CL = 2	$t_{HZ(3)}$ $t_{HZ(2)}$		5.4 5.4		5.4 6		6 6	ns	10 10
Data-out low-impedance time		$t_{LZ}$	1		1		1		ns	
Data-out hold time (load)		$t_{OH}$	3		3		3		ns	
Data-out hold time (no load)		$t_{OH_N}$	1.8		1.8		1.8		ns	28
ACTIVE to PRECHARGE command		$t_{RAS}$	37	120,000	44	120,000	50	120,000	ns	29
ACTIVE to ACTIVE command period		$t_{RC}$	60		66		70		ns	
ACTIVE to READ or WRITE delay		$t_{RCD}$	15		20		20		ns	
Refresh period (8,192 rows)		$t_{REF}$		64		64		64	ms	
AUTOREFRESH period		$t_{RFC}$	66		66		70		ns	
PRECHARGE command period		$t_{RP}$	15		20		20		ns	
ACTIVE bank a to ACTIVE bank b command		$t_{RRD}$	14		15		20		ns	
Transition time		$t_T$	0.3	1.2	0.3	1.2	0.3	1.2	ns	7
WRITE recovery time		$t_{WR}$	1 CLK + 7ns		1 CLK + 7.5ns		1 CLK + 7ns		ns	24
			14		15		15		ns	25
Exit SELF REFRESH to ACTIVE command		$t_{XSR}$	67		75		80		ns	20

\*Module AC timing parameters comply with PC133 Design Specs, based on component parameters.



## AC FUNCTIONAL CHARACTERISTICS

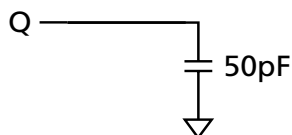
(Notes: 5, 6, 7, 8, 9, 11; notes appear following parameter tables)

PARAMETER	SYMBOL	-13E	-133	-10E	UNITS	NOTES	
READ/WRITE command to READ/WRITE command	$t_{CCD}$	1	1	1	$t_{CK}$	17	
CKE to clock disable or power-down entry mode	$t_{CKED}$	1	1	1	$t_{CK}$	14	
CKE to clock enable or power-down exit setup mode	$t_{PED}$	1	1	1	$t_{CK}$	14	
DQM to input data delay	$t_{DQD}$	0	0	0	$t_{CK}$	17	
DQM to data mask during WRITES	$t_{DQM}$	0	0	0	$t_{CK}$	17	
DQM to data high-impedance during READs	$t_{DQZ}$	2	2	2	$t_{CK}$	17	
WRITE command to input data delay	$t_{DWD}$	0	0	0	$t_{CK}$	17	
Data-in to ACTIVE command	$t_{DAL}$	4	5	4	$t_{CK}$	15, 21	
Data-in to PRECHARGE command	$t_{DPL}$	2	2	2	$t_{CK}$	16, 21	
Last data-in to burst STOP command	$t_{BDL}$	1	1	1	$t_{CK}$	17	
Last data-in to new READ/WRITE command	$t_{CDL}$	1	1	1	$t_{CK}$	17	
Last data-in to PRECHARGE command	$t_{RD L}$	2	2	2	$t_{CK}$	16, 21	
LOAD MODE REGISTER command to ACTIVE or REFRESH command	$t_{MRD}$	2	2	2	$t_{CK}$	26	
Data-out to high-impedance from PRECHARGE command	CL = 3	$t_{ROH(3)}$	3	3	3	$t_{CK}$	17
	CL = 2	$t_{ROH(2)}$	2	2	2	$t_{CK}$	17



## NOTES

- All voltages referenced to  $V_{SS}$ .
- This parameter is sampled.  $V_{DD}$ ,  $V_{DDQ} = +3.3V$ ;  $f = 1\text{ MHz}$ ,  $T_A = 25^\circ\text{C}$ ; pin under test biased at 1.4V.
- $I_{DD}$  is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
- Enables on-chip refresh and address counters.
- The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured ( $0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$ ).
- An initial pause of 100 $\mu\text{s}$  is required after power-up, followed by two AUTO REFRESH commands, before proper device operation is ensured. ( $V_{DD}$  and  $V_{DDQ}$  must be powered up simultaneously.  $V_{SS}$  and  $V_{SSQ}$  must be at same potential.) The two AUTO REFRESH command wake-ups should be repeated any time the  $t_{REF}$  refresh requirement is exceeded.
- AC characteristics assume  $t_T = 1\text{ ns}$ .
- In addition to meeting the transition rate specification, the clock and CKE must transit between  $V_{IH}$  and  $V_{IL}$  (or between  $V_{IL}$  and  $V_{IH}$ ) in a monotonic manner.
- Outputs measured at 1.5V with equivalent load:



- $t_{HZ}$  defines the time at which the output achieves the open circuit condition; it is not a reference to  $V_{OH}$  or  $V_{OL}$ . The last valid data element will meet  $t_{OH}$  before going High-Z.
- AC timing and  $I_{DD}$  tests have  $V_{IL} = 0V$  and  $V_{IH} = 3V$ , with timing referenced to 1.5V crossover point. If the input transition time is longer than 1 ns, then the timing is referenced at  $V_{IL}(\text{MAX})$  and  $V_{IH}(\text{MIN})$  and no longer at the 1.5V crossover point.
- Other input signals are allowed to transition no more than once every two clocks and are otherwise at valid  $V_{IH}$  or  $V_{IL}$  levels.
- $I_{DD}$  specifications are tested after the device is properly initialized.

- Timing actually specified by  $t_{CKS}$ ; clock(s) specified as a reference only at minimum cycle rate.
- Timing actually specified by  $t_{WR}$  plus  $t_{RP}$ ; clock(s) specified as a reference only at minimum cycle rate.
- Timing actually specified by  $t_{WR}$ .
- Required clocks are specified by JEDEC functionality and are not dependent on any timing parameter.
- The  $I_{DD}$  current will increase or decrease proportionally according to the amount of frequency alteration for the test condition.
- Address transitions average one transition every two clocks.
- CLK must be toggled a minimum of two times during this period.
- Based on  $t_{CK} = 10\text{ ns}$  for -10E, and  $t_{CK} = 7.5\text{ ns}$  for -133 and -13E.
- $V_{IH}$  overshoot:  $V_{IH}(\text{MAX}) = V_{DDQ} + 2V$  for a pulse width  $\leq 3\text{ ns}$ , and the pulse width cannot be greater than one third of the cycle rate.  $V_{IL}$  undershoot:  $V_{IL}(\text{MIN}) = -2V$  for a pulse width  $\leq 3\text{ ns}$ .
- The clock frequency must remain constant (stable clock is defined as a signal cycling within timing constraints specified for the clock pin) during access or precharge states (READ, WRITE, including  $t_{WR}$ , and PRECHARGE commands). CKE may be used to reduce the data rate.
- Auto precharge mode only. The precharge timing budget ( $t_{RP}$ ) begins 7ns for -13E; 7.5ns for -133 and 7ns for -10E after the first clock delay, after the last WRITE is executed. May not exceed limit set for precharge mode.
- Precharge mode only.
- JEDEC and PC100 specify three clocks.
- $t_{AC}$  for -133/-13E at  $CL = 3$  with no load is 4.6ns and is guaranteed by design.
- Parameter guaranteed by design.
- The value of  $t_{RAS}$ . use in -13E speed grade module SPDs is calculated from  $t_{RC} - t_{RP} = 45\text{ ns}$ .
- For -10E,  $CL = 2$  and  $t_{CK} = 10\text{ ns}$ ; for -133,  $CL = 3$  and  $t_{CK} = 7.5\text{ ns}$ ; for -13E,  $CL = 2$  and  $t_{CK} = 7.5\text{ ns}$ .
- CKE is HIGH during refresh command period  $t_{RFC}(\text{MIN})$  else CKE is LOW. The  $I_{DD6}$  limit is actually a nominal value and does not result in a fail value.





**SPD CLOCK AND DATA CONVENTIONS**

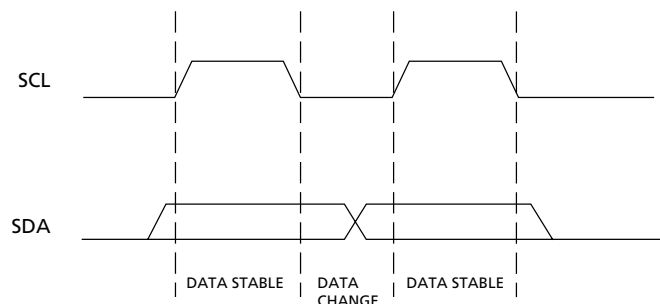
Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

**SPD START CONDITION**

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

**SPD STOP CONDITION**

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

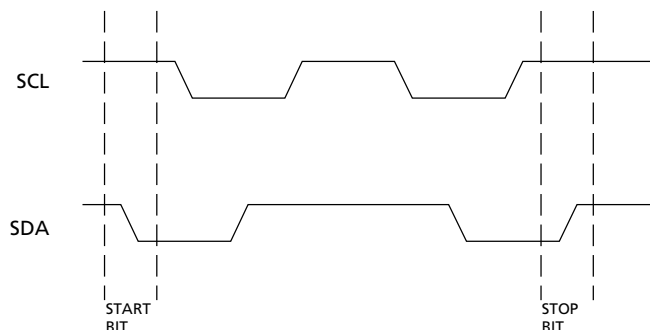


**Figure 1**  
**Data Validity**

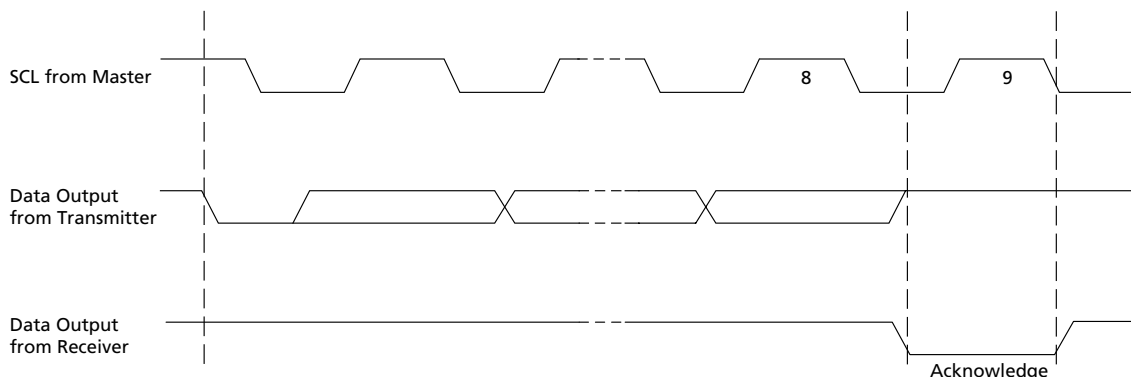
**SPD ACKNOWLEDGE**

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.



**Figure 2**  
**Definition of Start and Stop**



**Figure 3**  
**Acknowledge Response From Receiver**



### EEPROM DEVICE SELECT CODE

(The most significant bit (b7) is sent first)

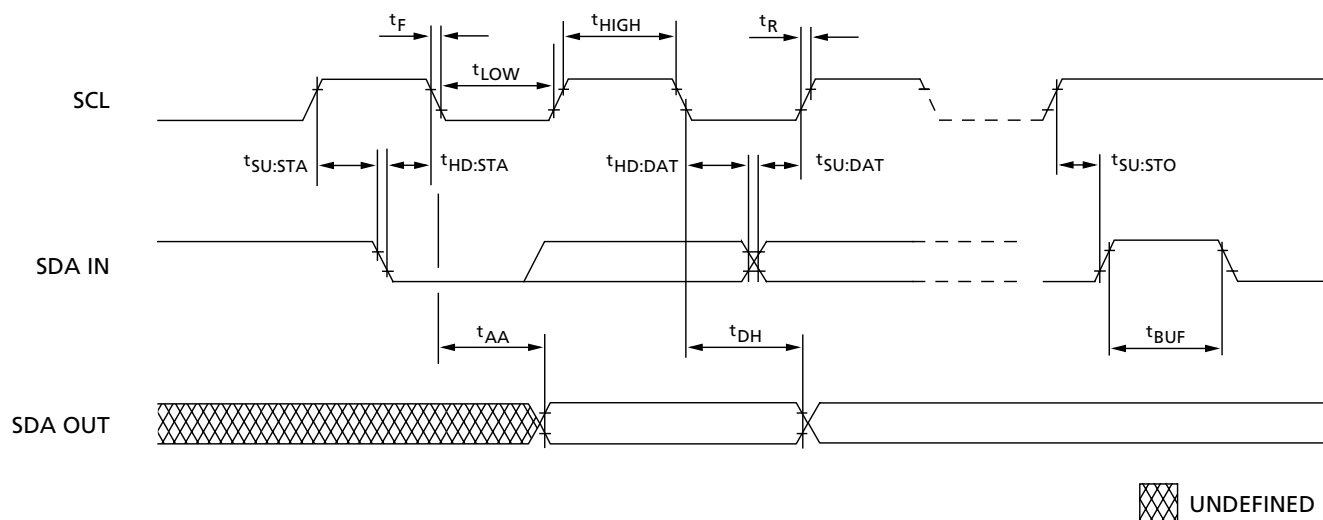
	Device Type Identifier				Chip Enable			RW
	b7	b6	b5	b4	b3	b2	b1	b0
Memory Area Select Code (two arrays)	1	0	1	0	E2	E1	E0	RW
Protection Register Select Code	0	1	1	0	E2	E1	E0	RW

### EEPROM OPERATING MODES

(X = V<sub>IH</sub> or V<sub>IL</sub>)

MODE	RW Bit	WC <sup>1</sup>	BYTES	Initial Sequence
Current Address Read	1	X	1	Start, Device Select, RW = 1
Random Address Read	0	X	1	Start, Device Select, RW = 0, Address
	1	X		reSTART, Device Select, RW = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V <sub>IL</sub>	1	START, Device Select, RW = 0
Page Write	0	V <sub>IL</sub>	≤ 16	START, Device Select, RW = 0

### SPD EEPROM TIMING DIAGRAM



### SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

SYMBOL	MIN	MAX	UNITS
t <sub>AA</sub>	0.3	3.5	μs
t <sub>BUF</sub>	4.7		μs
t <sub>DH</sub>	300		ns
t <sub>F</sub>		300	ns
t <sub>HD:DAT</sub>	0		μs
t <sub>HD:STA</sub>	4		μs

SYMBOL	MIN	MAX	UNITS
t <sub>HIGH</sub>	4		μs
t <sub>LOW</sub>	4.7		μs
t <sub>R</sub>		1	μs
t <sub>SU:DAT</sub>	250		ns
t <sub>SU:STA</sub>	4.7		μs
t <sub>SU:STO</sub>	4.7		μs


**SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS**

 (Note: 1) ( $V_{DD} = +3.3V \pm 0.3V$ )

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS
SUPPLY VOLTAGE	$V_{DD}$	3	3.6	V
INPUT HIGH VOLTAGE: Logic 1; All inputs	$V_{IH}$	$V_{DD} \times 0.7$	$V_{DD} + 0.5$	V
INPUT LOW VOLTAGE: Logic 0; All inputs	$V_{IL}$	-1	$V_{DD} \times 0.3$	V
OUTPUT LOW VOLTAGE: $I_{OUT} = 3mA$	$V_{OL}$	-	0.4	V
INPUT LEAKAGE CURRENT: $V_{IN} = GND$ to $V_{DD}$	$I_{LI}$	-	10	$\mu A$
OUTPUT LEAKAGE CURRENT: $V_{OUT} = GND$ to $V_{DD}$	$I_{LO}$	-	10	$\mu A$
STANDBY CURRENT: SCL = SDA = $V_{DD} - 0.3V$ ; All other inputs = GND or $3.3V + 10\%$	$I_{SB}$	-	30	$\mu A$
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	$I_{CC}$	-	2	mA

**SERIAL PRESENCE-DETECT EEPROM AC OPERATING CONDITIONS**

 (Note: 1) ( $V_{DD} = +3.3V \pm 0.3V$ )

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	$t_{AA}$	0.3	3.5	$\mu s$	
Time the bus must be free before a new transition can start	$t_{BUF}$	4.7		$\mu s$	
Data-out hold time	$t_{DH}$	300		ns	
SDA and SCL fall time	$t_F$		300	ns	
Data-in hold time	$t_{HD:DAT}$	0		$\mu s$	
Start condition hold time	$t_{HD:STA}$	4		$\mu s$	
Clock HIGH period	$t_{HIGH}$	4		$\mu s$	
Noise suppression time constant at SCL, SDA inputs	$t_I$		100	ns	
Clock LOW period	$t_{LOW}$	4.7		$\mu s$	
SDA and SCL rise time	$t_R$		1	$\mu s$	
SCL clock frequency	$t_{SCL}$		100	KHz	
Data-in setup time	$t_{SU:DAT}$	250		ns	
Start condition setup time	$t_{SU:STA}$	4.7		$\mu s$	
Stop condition setup time	$t_{SU:STO}$	4.7		$\mu s$	
WRITE cycle time	$t_{WRC}$		10	ms	2

- NOTE:**
- All voltages referenced to  $V_{SS}$ .
  - The SPD EEPROM WRITE cycle time ( $t_{WRC}$ ) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.


**SERIAL PRESENCE-DETECT MATRIX**

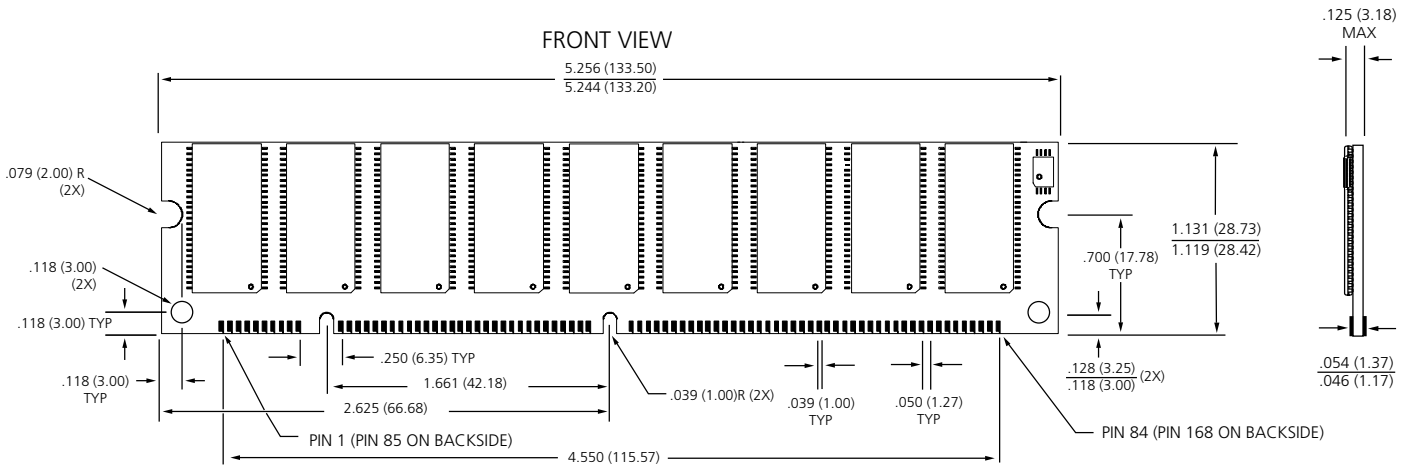
BYTE	DESCRIPTION	ENTRY (VERSION)	MT9LSDT3272AG	MT18LSDT6472A
0	NUMBER OF BYTES USED BY MICRON	128	80	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256	08	08
2	MEMORY TYPE	SDRAM	04	04
3	NUMBER OF ROW ADDRESSES	13	0D	0D
4	NUMBER OF COLUMN ADDRESSES	10	0A	0A
5	NUMBER OF BANKS	1 or 2	01	02
6	MODULE DATA WIDTH	72	48	48
7	MODULE DATA WIDTH (continued)	0	00	00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTTL	01	01
9	SDRAM CYCLE TIME, $t_{CK}$ (CAS LATENCY = 3)	7.5 (-13E)	70	75
		7.5 (-133)	75	75
		8 (-10E)	80	80
10	SDRAM ACCESS FROM CLK, $t_{AC}$ (CAS LATENCY = 3)	5.4 (-13E/-133)	54	54
		6 (-10E)	60	60
11	MODULE CONFIGURATION TYPE	ECC	02	02
12	REFRESH RATE/TYPE	7.81 $\mu$ s/SELF	82	82
13	SDRAM WIDTH (PRIMARY SDRAM)	8	08	08
14	ERROR-CHECKING SDRAM DATA WIDTH	8	08	08
15	MINIMUM CLOCK DELAY FROM BACK-TO-BACK RANDOM COLUMN ADDRESSES, $t_{CCD}$	1	01	01
16	BURST LENGTHS SUPPORTED	1, 2, 4, 8, PAGE	8F	8F
17	NUMBER OF BANKS ON SDRAM DEVICE	4	04	04
18	CAS LATENCIES SUPPORTED	2, 3	06	06
19	CS LATENCY	0	01	01
20	WE LATENCY	0	01	01
21	SDRAM MODULE ATTRIBUTES	UNBUFFERED	00	00
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0E	0E	0E
23	SDRAM CYCLE TIME, $t_{CK}$ (CAS LATENCY = 2)	7.5 (-13E)	75	75
		10 (-133/-10E)	A0	A0
24	SDRAM ACCESS FROM CLK, $t_{AC}$ (CAS LATENCY = 2)	5.4 (-13E)	54	54
		6 (-133/-10E)	60	60
25	SDRAM CYCLE TIME, $t_{CK}$ (CAS LATENCY = 1)	-	00	00
26	SDRAM ACCESS FROM CLK, $t_{AC}$ (CAS LATENCY = 1)	-	00	00
27	MINIMUM ROW PRECHARGE TIME, $t_{RP}$	15 (-13E)	0F	0F
		20 (-133/-10E)	14	14
28	MINIMUM ROW ACTIVE TO ROW ACTIVE, $t_{RRD}$	14 (-13E)	0E	0E
		15 (-133)	0F	0F
		20 (-10E)	14	14
29	MINIMUM RAS# TO CAS# DELAY, $t_{RCD}$	15 (-13E)	0F	0F
		20 (-133/-10E)	14	14
30	MINIMUM RAS# PULSE WIDTH, $t_{RAS}$ ( $t_{RAS}$ MODULE = $t_{RC}$ - $t_{RP}$ ) note 2	45 (-13E)	2D	2D
		44 (-133)	2C	2C
		50 (-10E)	32	32
31	MODULE BANK DENSITY	256MB	40	40
32	COMMAND AND ADDRESS SETUP TIME, $t_{AS}$ , $t_{CMS}$	1.5 (-13E/-133)	15	15
		2 (-10E)	20	20

- NOTE:** 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."  
2. The value of  $t_{RAS}$  used for -13E modules is calculated from  $t_{RC}$  -  $t_{RP}$ . Actual device spec. value is 37ns.

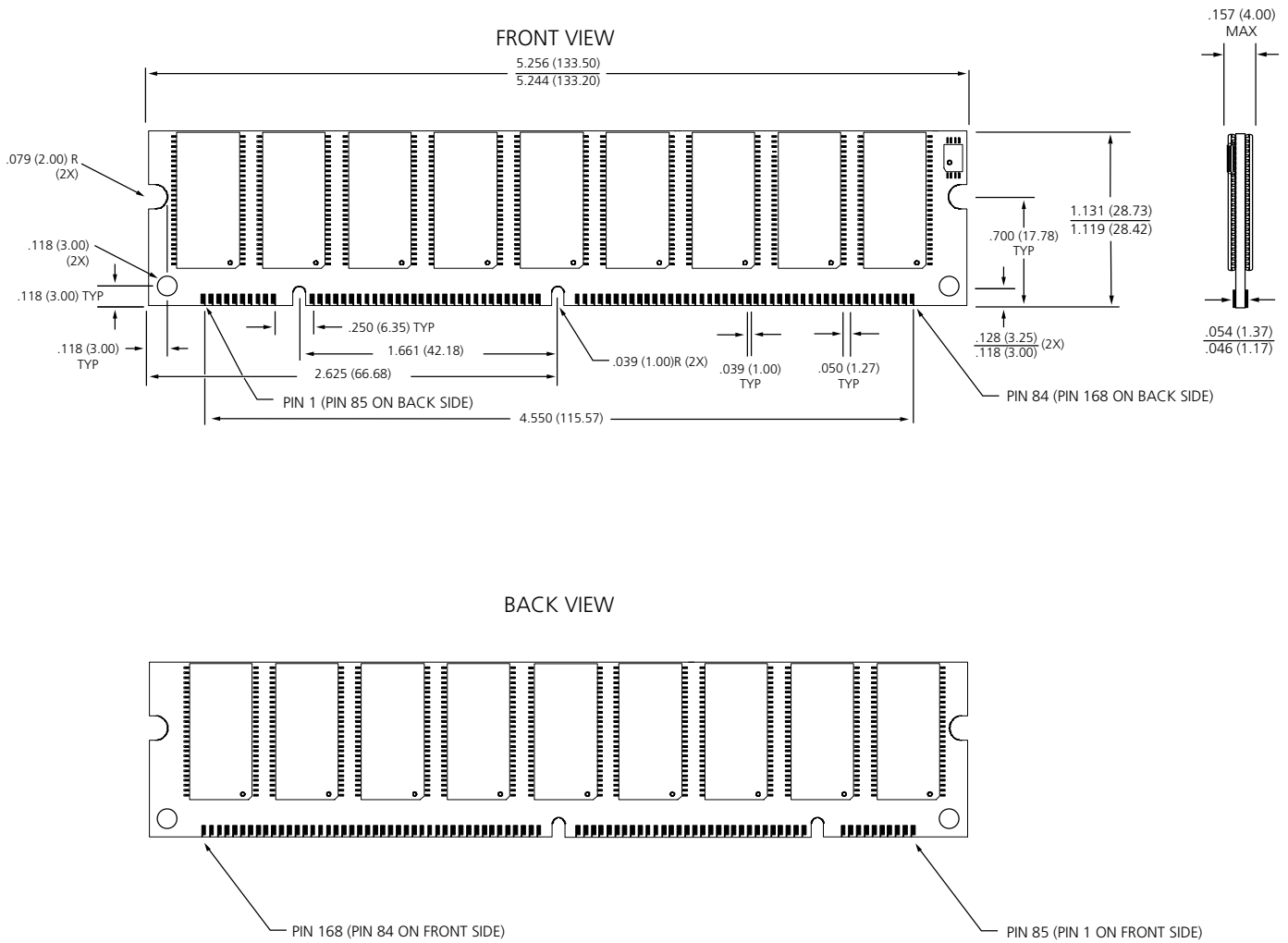

**SERIAL PRESENCE-DETECT MATRIX (continued)**

BYTE	DESCRIPTION	ENTRY (VERSION)	MT9LSDT3272AG	MT18LSDT6472A
33	COMMAND AND ADDRESS HOLD TIME, <sup>t</sup> AH, <sup>t</sup> CMH	0.8 (-13E)	08	08
		0.8 (-133)	08	08
		1 (10E)	10	10
34	DATA SIGNAL INPUT SETUP TIME, <sup>t</sup> DS	1.5 (-13E)	15	15
		1.5 (-133)	15	15
		2 (-10E)	20	20
35	DATA SIGNAL INPUT HOLD TIME, <sup>t</sup> DH	0.8 (-13E)	08	08
		0.8 (-133)	08	08
		1 (-10E)	10	10
36-61	RESERVED		00	00
62	SPD REVISION	REV. 1.2	12	12
63	CHECKSUM FOR BYTES 0-62	(-13E)	9D	9E
		(-133)	E3	E4
		(-10E)	2B	2C
64	MANUFACTURER'S JEDEC ID CODE	MICRON	2C	2C
65-71	MANUFACTURER'S JEDEC ID CODE (CONT.)		FF	FF
72	MANUFACTURING LOCATION		01	01
			02	02
			03	03
			04	04
			05	05
			06	06
			07	07
			08	08
73-90	MODULE PART NUMBER (ASCII)		xx	xx
91	PCB IDENTIFICATION CODE	1	01	01
		2	02	02
		3	03	03
		4	04	04
		5	05	05
		6	06	06
		7	07	07
		8	08	08
		9	09	09
92	IDENTIFICATION CODE (CONT.)	0	00	00
93	YEAR OF MANUFACTURE IN BCD		xx	xx
94	WEEK OF MANUFACTURE IN BCD		xx	xx
95-98	MODULE SERIAL NUMBER		xx	xx
99-125	MANUFACTURER-SPECIFIC DATA (RSVD)		-	-
126	SYSTEM FREQUENCY 100 MHz	(-13E/-133/-10E)	64	64
127	SDRAM COMPONENT & CLOCK DETAIL		AF	FF

**NOTE:** 1. "1"/"0": Serial Data, "driven to HIGH"/"driven to LOW."  
2. x = Variable Data.

**256MB MODULE**


**NOTE:** 1. All dimensions in inches (millimeters)  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.

**512MB MODULE**


**NOTE:** 1. All dimensions in inches (millimeters)  $\frac{\text{MAX}}{\text{MIN}}$  or typical where noted.



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