**AT&T** Microelectronics

# ATTM6088

# 5.5 Mbit (128K x 44) Secondary Cache Module for R4000

## Features

- 25 ns access time

- Support for 50 MHz R4000 MIPS architecture with zero wait-state

- High-speed CMOS SRAMs for cache data and tag functions

- Support for 16-, 32-, 64-, and 128-byte cache blocks

- Pin-compatible with IDT7MP6084 and IDT7MP6094 secondary cache modules

- Single 5 V (±10%) power supply

- Gold-plated contacts on each side for minimum socket resistance

- Package styles available:
  — 80-lead SIMM module with surface-mount plastic components on epoxy (FR-4) substrate TTL compatible I/Os
  — ZIP module

## Description

The ATTM6088 is a 5.5 Mbit secondary cache module that supports the R4000 MIPS CPU. Four ATTM6088 modules are required to complete a full 2 Mbyte secondary cache for the R4000.

The module is constructed using six 128K x 8 bit high-speed CMOS SRAMs and two 10-bit buffer/drivers. The ICs are surface-mounted to an epoxy-glass laminate (FR-4) substrate. The 10-bit buffers incorporate on-chip 25 Ω series resistors that minimize overshoot and ringing during fast cycle times.

The ATTM6088 module is partitioned to provide both cache data and tag functions. Five 128K x 8 bit SRAMs comprise the cache data while one 128K x 8 bit SRAM is used for the tag and state. The ATTM6088 supports an R4000-based system at speeds to 50 MHz with zero wait-state operation. All inputs are TTL compatible and operate from a single 5 V supply.

The ATTM6088 module supports 16-, 32-, 64-, and 128-byte cache blocks via a jumper arrangement on addresses A0—A2 of the 128K x 8 tag and state SRAM. The user can reconfigure the module by changing the jumpers as shown in Tables 2.
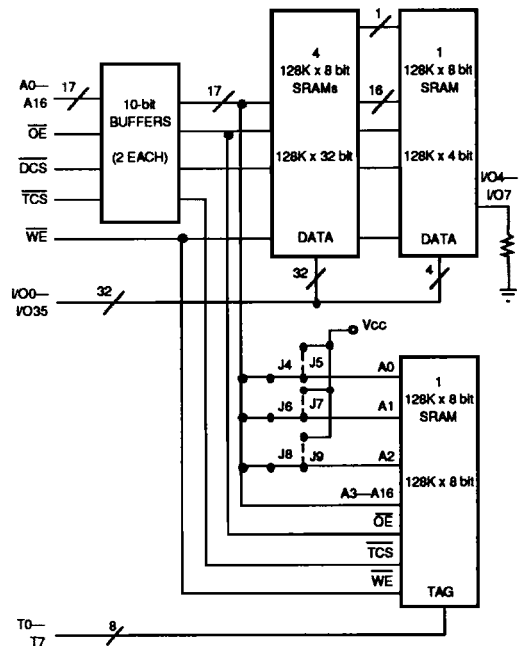


**Figure 1. Block Diagram**

# Pin Information

### Table 1. Pin Descriptions

| Pin | Name/Function |
|---|---|
| I/O0—I/O35 | Data Inputs/Outputs |
| T0—T7 | Tag Inputs/Outputs |
| A0—A16 | Address Inputs |
| $\overline{DCS}$ | Data Chip Select |
| $\overline{TCS}$ | Tag Chip Select |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| Vcc | Power Supply |
| GND | Ground |
| NC | No Connect |

### Table 2. Jumper Combinations (J4—J9)

| Jumper | Second-Level Cache Block Size (Bytes) | | | |
|---|---|---|---|---|
| | 16 | 32 | 64 | 128 |
| J4 | In | Out | Out | Out |
| J5 | Out | In | In | In |
| J6 | In | In | Out | Out |
| J7 | Out | Out | In | In |
| J8 | In | In | In | Out |
| J9 | Out | Out | Out | In |

Note: Jumpers J1—J3 (not shown) are factory set. These are not user configurable.

| | | | | |
|---|---|---|---|---|
| GND | 1 | 2 | Vcc | |
| I/O0 | 3 | 4 | I/O1 | |
| I/O2 | 5 | 6 | I/O3 | |
| I/O4 | 7 | 8 | I/O5 | |
| I/O6 | 9 | 10 | GND | |
| I/O7 | 11 | 12 | I/O8 | |
| I/O9 | 13 | 14 | I/O10 | |
| I/O11 | 15 | 16 | I/O12 | |
| I/O13 | 17 | 18 | I/O14 | |
| GND | 19 | 20 | I/O15 | |
| I/O16 | 21 | 22 | I/O17 | |
| I/O18 | 23 | 24 | I/O19 | |
| I/O20 | 25 | 26 | I/O21 | |
| I/O22 | 27 | 28 | GND | |
| Vcc | 29 | 30 | I/O23 | |
| I/O24 | 31 | 32 | I/O25 | |
| I/O26 | 33 | 34 | I/O27 | |
| I/O28 | 35 | 36 | I/O29 | |
| GND | 37 | 38 | I/O30 | |
| I/O31 | 39 | 40 | I/O32 | |
| I/O33 | 41 | 42 | I/O34 | |
| I/O35 | 43 | 44 | GND | |
| $\overline{WE}$ | 45 | 46 | A0 | |
| A1 | 47 | 48 | A2 | |
| A3 | 49 | 50 | A4 | |
| A5 | 51 | 52 | A6 | |
| GND | 53 | 54 | Vcc | |
| $\overline{DCS}$ | 55 | 56 | $\overline{OE}$ | |
| A7 | 57 | 58 | A8 | |
| A9 | 59 | 60 | A10 | |
| A11 | 61 | 62 | GND | |
| A12 | 63 | 64 | A13 | |
| A14 | 65 | 66 | A15 | |
| A16 | 67 | 68 | NC | |
| $\overline{TCS}$ | 69 | 70 | T0 | |
| GND | 71 | 72 | T1 | |
| T2 | 73 | 74 | T3 | |
| T4 | 75 | 76 | T5 | |
| T8 | 77 | 78 | T7 | |
| Vcc | 79 | 80 | GND | |

Note: Pins alternate side-to-side on the ZIP module (as shown). All 80 pins on the SIMM module appear on both sides.

### Figure 2. Pin Diagram (Top View)

## Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operations sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Terminal Voltage with Respect to GND | $V_{TERM}$ | −0.5 | 7.0 | V |
| Operating Temperature | $T_A$ | 0 | 70 | °C |
| Storage Temperature | $T_{stg}$ | −55 | 125 | °C |
| dc Output Current (Short Circuit) | $I_{OUT}$ | — | 25 | mA |

## Recommended Operating Conditions

| Mode | Temperature Range (Ambient) | Supply Voltage |
|---|---|---|
| Commercial | 0 °C to 70 °C | 5 V ± 10% |

# Electrical Characteristics

### Table 3. General Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage: | | | | | | |
| High | $V_{IH}$ | — | 2.2 | — | Vcc + 0.3 | V |
| Low | $V_{IL}$ | — | –0.5 | — | 0.8 | V |
| Output Voltage: | | | | | | |
| High | $V_{OH}$ | Vcc = Min, $I_{OH}$ = –4 mA | 2.4 | — | — | V |
| Low | $V_{OL}$ | Vcc = Min, $I_{OL}$ = 8 mA | — | — | 0.4 | V |
| Supply Voltage | Vcc | — | 4.5 | 5 | 5.5 | V |
| Ground | GND | — | 0 | 0 | 0 | V |
| Input Leakage Current: | | | | | | |
| Except A0, $\overline{WE}$ | $I_{LI1}$ | Vcc = Max, $V_{IN}$ = GND to Vcc | — | — | 10 | μA |
| A0, $\overline{WE}$ | $I_{LI2}$ | Vcc = Max, $V_{IN}$ = GND to Vcc | — | — | 110 | μA |
| Output Leakage Current | $I_{LO}$ | Vcc = Max, $\overline{CS}$ = $V_{IH}$, $V_{OUT}$ = GND to Vcc | — | — | 10 | μA |
| Operating Current[1,2] (typical R4000 application) | $I_{CC}$ | — | — | — | 400 | mA |
| Standby Current[3] | $I_{SB}$ | — | — | — | 250 | mA |
| Active Current (100% duty cycle) | $I_{MAX}$ | Inputs changing 0 V—3 V; Outputs open; $\overline{DCS}$ = $\overline{TCS}$ = $\overline{WE}$ = low; Write cycle = 50 ns | — | — | 1000 | mA |
| Capacitance:[1] | | | | | | |
| Input/Output (data) | $C_{I/O}(D)$ | $V_{IN}$ = 0 V | — | — | 10 | pF |
| Input (A1—A15, $\overline{OE}$, $\overline{TCS}$, $\overline{DCS}$) | $C_{IN}(A)$ | $V_{IN}$ = 0 V | — | — | 10 | pF |
| Input (A0, $\overline{WE}$) | $C_{IN}(B)$ | $V_{IN}$ = 0 V | — | — | 100 | pF |

1. This parameter is guaranteed by design, but not tested.
2. The conditions for determining operating current (Icc) for a typical R4000 system are as follows:
   - 50 MHz master clock.
   - 100 MHz (internal) Pclock.
   - Assume 5 Pclock cycles required for a secondary cache read or write; therefore, min. read/write cycle = 50 ns and min. access time (module) = 25 ns.
   - Assume hit rate of primary cache is 85%; therefore, secondary cache has 15% duty cycle for read/write instruction from the R4000 processor.
   - Allow an additional 5% module duty cycle for secondary cache fill and copyback operations; therefore, total secondary cache duty cycle is 20%.

   Under the conditions outlined above, the maximum operating current for the module is 400 mA:

   Icc = (%active)($I_{MAX}$) + (%standby)($I_{SB}$)
   Icc = (0.20 x 1000 mA) + (0.80 x 250 mA)
   Icc = 400 mA
3. Tested with outputs open and all address and data inputs stable. The module is continuously disabled ($\overline{TCS}$ = $\overline{DCS}$ = Vcc). Input levels are within 0.2 V of Vcc or ground.
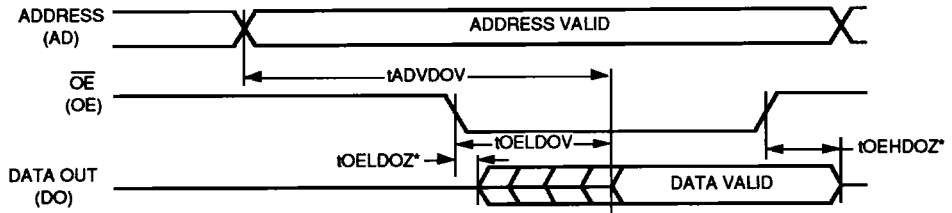
# Timing Characteristics

## Table 4. Read Cycle

Vcc = 5 V ± 10%, TA = 0 °C to 70 °C

| Symbol | Parameter | Min | Max | Unit |
|--------|-----------|-----|-----|------|
| tADVDOV | Address Access Time | — | 25 | ns |
| tOELDOV | Output Enable to Output Valid | — | 25 | ns |
| tOEHDOZ* | Output Enable High to Output in High Z | — | 20 | ns |
| tOELDOZ* | Output Enable to Output in Low Z | 0 | — | ns |

* This parameter is guaranteed by design, but not tested.
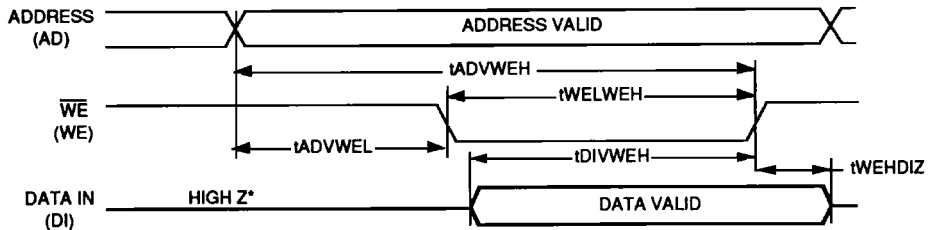


* This parameter is guaranteed by design, but not tested.

**Figure 3. Read Cycle**

## Table 5. Write Cycle

Vcc = 5 V ± 10%, TA = 0 °C to 70 °C

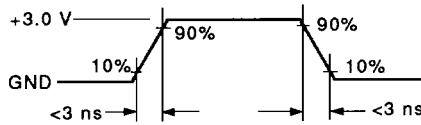| Symbol | Parameter | Min | Max | Unit |
|--------|-----------|-----|-----|------|
| tADVWEH | Address Valid to End of Write | 25 | — | ns |
| tWELWEH | Write Pulse Width | 15 | — | ns |
| tDIVWEH | Data Valid to End of Write | 10 | — | ns |
| tWEHDIZ | Data Hold Time | 0 | — | ns |
| tADVWEL | Address Valid to Write Enable Low | 7 | — | ns |



* Common I/O lines must be in 3-state prior to a write cycle.

**Figure 4. Write Cycle**
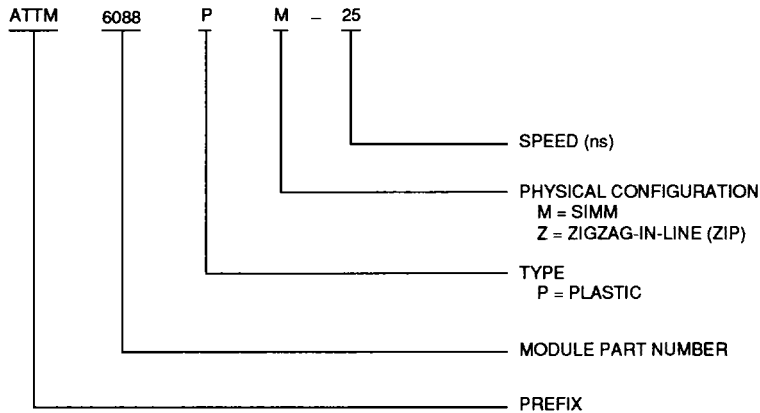
## Timing Characteristics (continued)



**A.**    **B.**
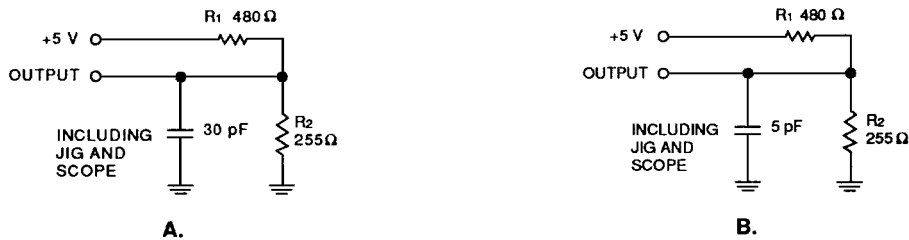
**Figure 5.  Test Loads**



**Figure 6.  Transition Times**

## Ordering Information



ATTM    6088    P    M  –  25

SPEED (ns)

PHYSICAL CONFIGURATION
M = SIMM
Z = ZIGZAG-IN-LINE (ZIP)

TYPE
P = PLASTIC

MODULE PART NUMBER

PREFIX

Operating Range 0 °C to 70 °C on all devices.

| Device # | Package Style | Performance Speed |
|----------|---------------|-------------------|
|          |               | 25 ns |
| ATTM6088 | 80-Lead SIMM Module | ATTM6088PM-25 |
|          | 80-Lead ZIP Module | ATTM6088PZ-25 |