SONY

CXA1845Q

I²C Bus-Compatible Audio/Video Switch

Description

The CXA1845Q is a 7-input, 3-output audio/video switch featuring I²C bus compatibility for TVs.

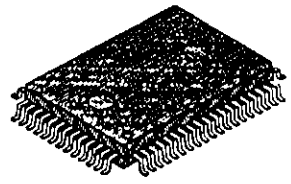
Features

- Serial control via I²C bus
- 7 inputs, 3 outputs
- 3 outputs can each be independently selected
- Separate control of video and audio switches
- 6dB amplifiers for both video and audio outputs
- Wideband video amplifier (20MHz, –3dB)
- Y/C mixer circuit
- Slave address can be changed (90H/92H)
- Audio muting from external pin
- I²C bus line (SDA, SCL) is left in high impedance state when power is OFF
- Wide audio dynamic range (3Vrms typ.)

Applications

Audio/video switch featuring I²C bus compatibility for TVs

64 pin QFP (Plastic)



Absolute Maximum Ratings

• Supply voltage	Vcc	12	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	PD	1000	mW

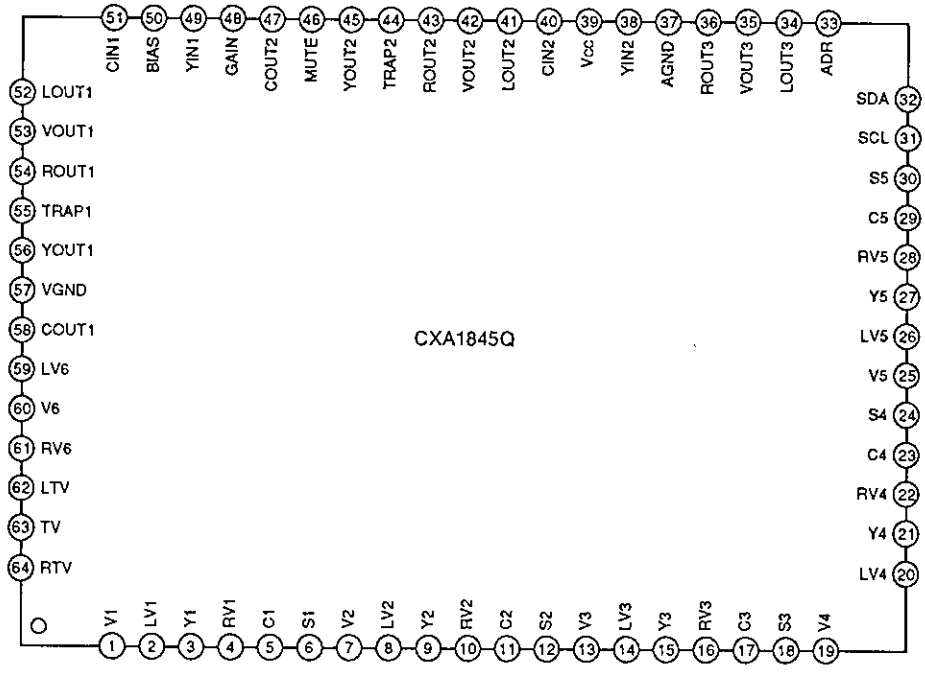
Operating Conditions

Supply voltage	Vcc	9±0.5	V

Structure

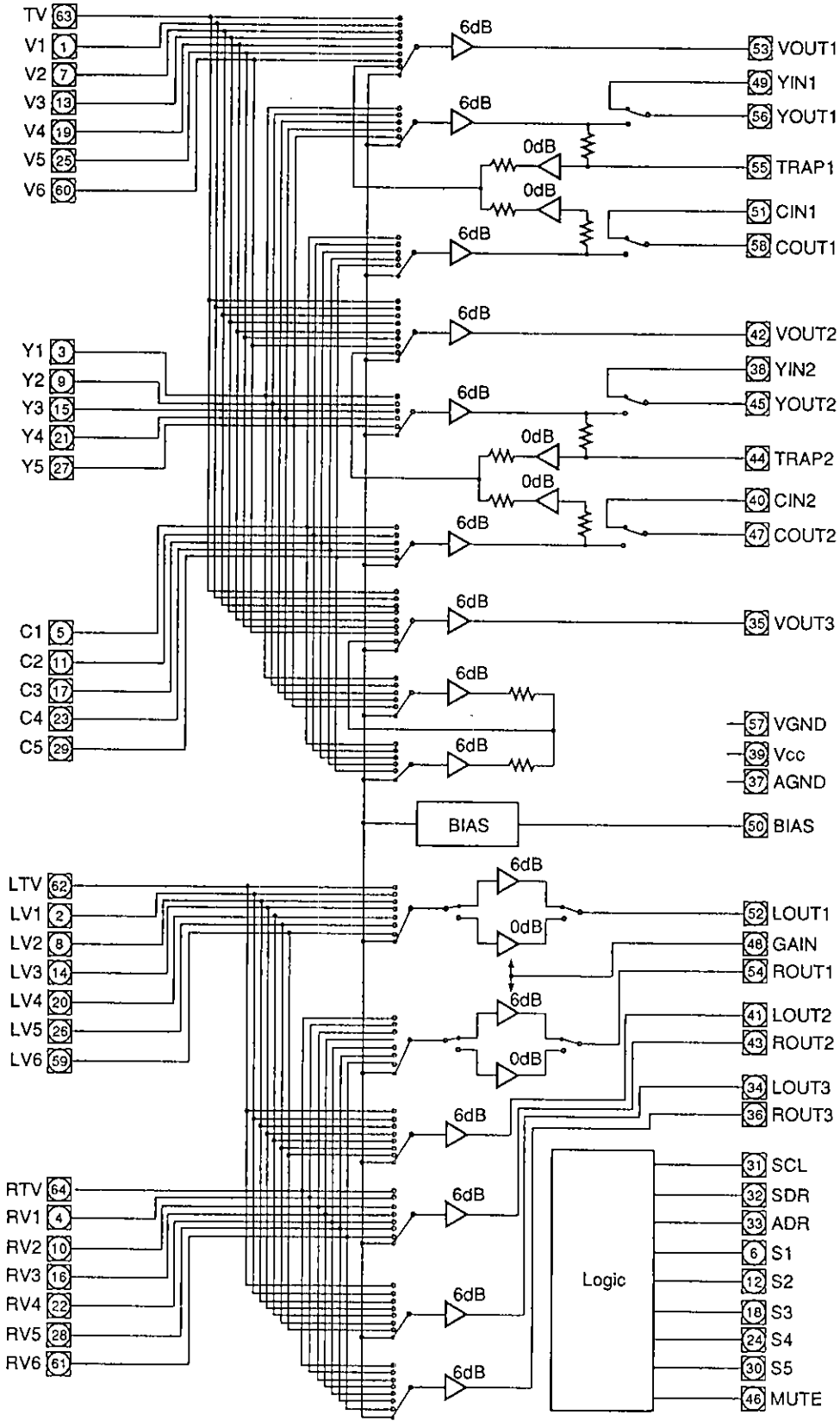
Bipolar silicon monolithic IC

Pin Configuration (Top View)



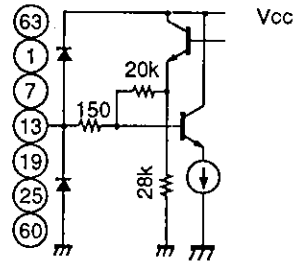
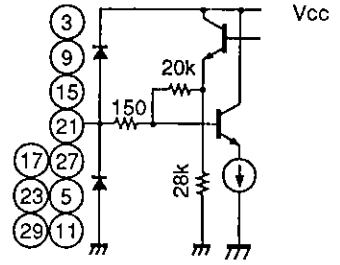
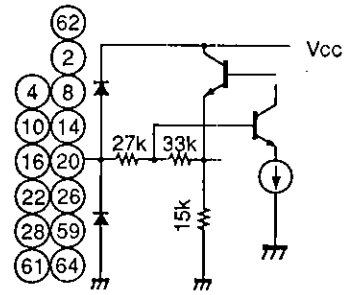
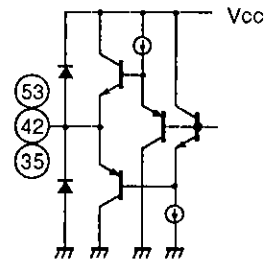
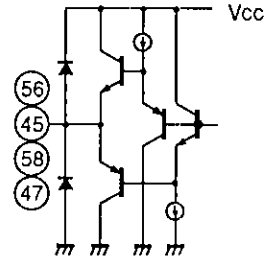
E93408B58—ST

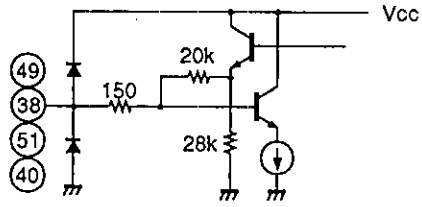
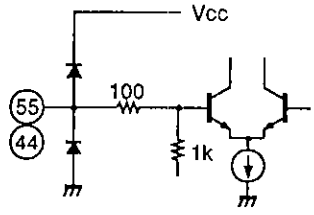
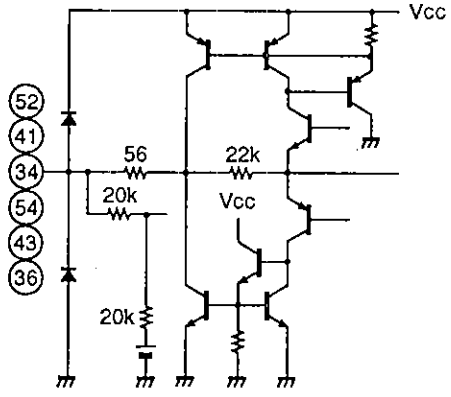
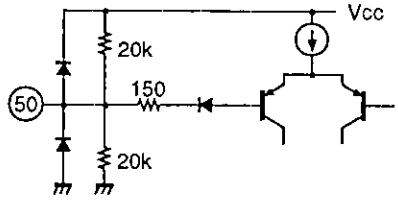
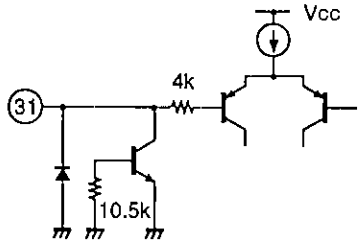
Block Diagram

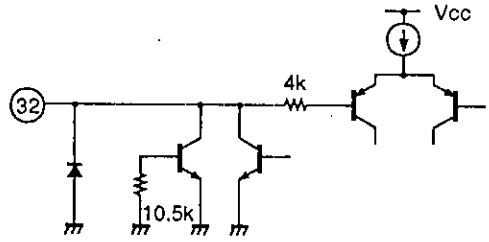
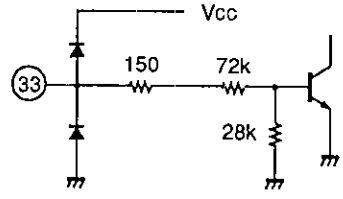
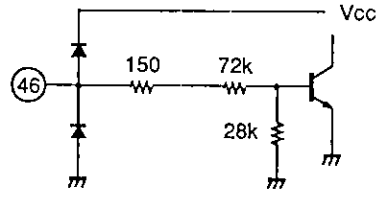
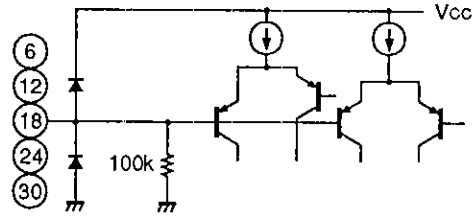
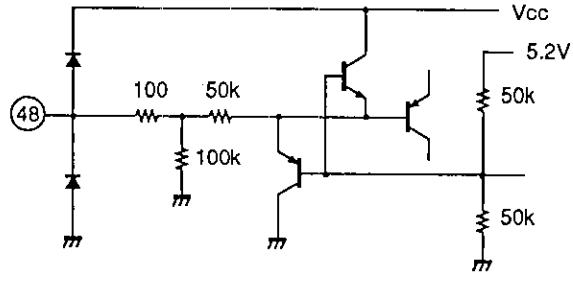


Note) A total gain of 0dB is achieved by connecting a 6kΩ resistor to the each audio input.

Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
63 1 7 13 19 25 60	TV V1 V2 V3 V4 V5 V6	4.5V		Video signal inputs. Input composite video signals.
3 9 15 21 27 5 11 17 23 29	Y1 Y2 Y3 Y4 Y5 C1 C2 C3 C4 C5	4.5V		Y/C separation signal inputs Y1 to Y5 pins: Luminance signals input C1 to C5 pins: Chrominance signals input
62 2 8 14 20 26 59 64 4 10 16 22 28 61	LTV LV1 LV2 LV3 LV4 LV5 LV6 RTV RV1 RV2 RV3 RV4 RV5 RV6	4.6V		Audio signal inputs.
53 42 35	VOUT1 VOUT2 VOUT3	4.5V		Video signal outputs. Output composite video signals.
56 45 58 47	YOUT1 YOUT2 COUT1 COUT2	4.5V		Y/C signal outputs. YOUT1, YOUT2 pins: Luminance signal output COUT1, COUT2 pins: Chrominance signal output

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
49 38 51 40	YIN1 YIN2 CIN1 CIN2	4.5V		YIN1, CIN1 pins: Input the Y/C separated signal of VOUT1 output. YIN2, CIN2 pins: Input the Y/C separated signal of VOUT2 output.
55 44	TRAP1 TRAP2	4.5V		Connect the subcarrier trap circuits.
52 41 34 54 43 36	LOUT1 LOUT2 LOUT3 ROUT1 ROUT2 ROUT3	4.6V		Audio signal outputs. Z_{OUT} =50Ω (Within DC ±2mA)
50	BIAS	4.6V		Internal reference bias (Vcc/2). A capacitor is connected between this pin and GND.
31	SCL	—		I^2C bus signal input. V_{IL} =1.5V (max.) V_{IH} =3.0V (min.)

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
32	SDA	—		I²C bus signal input/output. VIL =1.5V (max.) VIH =3.0V (min.) VOL=0.4V (max.)
33	ADR	—		Selects the slave address for the I²C bus. 90H at 1.5V or less 92H at 2.5V or more 90H when open
46	MUTE	—		Audio output mute. Mute OFF at 1.5V or less Mute ON at 2.5V or more Mute OFF when open
6 12 18 24 30	S1 S2 S3 S4 S5	—		Video/S signal selection. S signal output at 0.8V or less Video signal output at 1.4V or more S signal output when open
48	GAIN	—		Audio output gain control. 0dB output at 2.0V or less –6dB output at 3.0V or more 0dB output when open

Electrical Characteristics

(Ta=25°C, Vcc=9V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Current consumption	ICC	Vcc=9V, no signal, no load	48	60	78	mA

(Video system)

Gain	GVv	f=100kHz, 0.3Vp-p input (Fig. 1)	5.5	6.0	6.5	dB
Frequency response characteristics	FBWV1	0.3Vp-p input, input frequency where output amplitude is –3dB with 100kHz output serving as 0dB (Fig. 1)	15	20	—	MHz
Frequency response characteristics (Y/C mix)	FBWV2	0.3Vp-p input, input frequency where output amplitude is -3dB with 100kHz output serving as 0dB (Fig. 1)	10	15	—	MHz
Input dynamic range	Vdv	f=100kHz, maximum with distortion<1.0% (Fig. 1)	2.0	—	—	Vp-p
Cross talk	Vctv	f=4.43MHz, 1Vp-p input (Fig. 2)	—	—	–50	dB

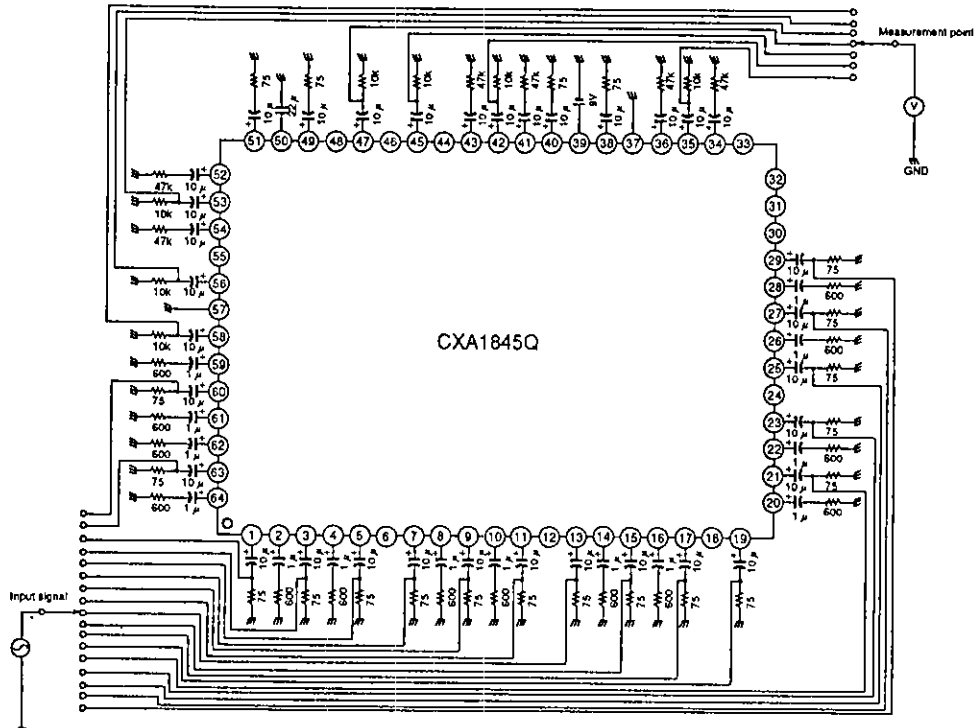
(Audio system)

Gain	GVA	f=1kHz, 1Vp-p input, 6kΩ resistor inserted to input (Fig. 3)	–1	0	1	dB
Frequency response characteristics	FBWA	1Vp-p input, input frequency where output amplitude is –3dB with 100kHz output serving as 0dB (Fig. 3)	50	—	—	kHz
Total harmonic distortion	THD	f=1kHz, 2.2Vp-p input, when 400Hz HPF + 80kHz LPF are inserted (Fig. 3)	—	0.03	0.05	%
Input dynamic range	VdA	f=1kHz, maximum with distortion<0.3% (Fig. 3)	2.8	3.0	—	Vrms
Cross talk	VctA	f=1kHz, 1Vp-p input (Fig. 4)	—	–90	–80	dB
Ripple rejection ratio		f=100Hz, 0.3Vp-p applied to Vcc (Fig. 5)	—	–50	–40	dB
Output DC offset	VOFF	Offset voltage between input and output (Fig. 6)	–30	—	30	mV
Residual noise	VNA	fCL=300Hz, fCH=19kHz, 40dB amplifier connected (Fig. 7)	0	—	6.0	mV
S/N ratio	S/N	f=1kHz, 1Vrms input (Fig. 3)	90	100	—	dB

(Logic system)

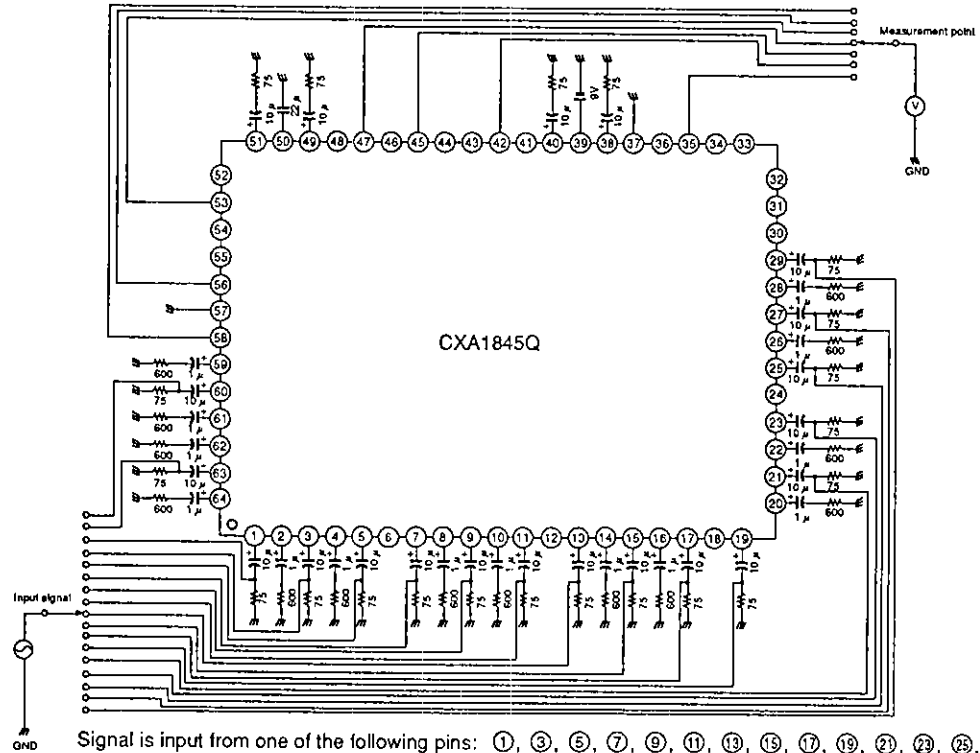
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
High level input voltage	V_{IH}		3.0	—	5.0	V
Low level input voltage	V_{IL}		0	—	1.5	V
Low level output voltage	V_{OL}	With SDA 3mA current supplied	0	—	0.4	V
High level input current	I_{IH}	V_{IH}=4.5V	0	—	10	μA
Low level input current	I_{IL}	V_{IL}=0.4V	0	—	10	μA
Maximum clock frequency	f_{SCL}		0	—	100	kHz
Minimum waiting time for data change	t_{BUF}		4.0	—	—	μs
Minimum waiting time for data transfer start	$t_{HD;STA}$		4.0	—	—	μs
Low level clock pulse width	t_{LOW}		4.7	—	—	μs
High level clock pulse width	t_{HIGH}		4.0	—	—	μs
Minimum waiting time for start preparation	$t_{SU;STA}$		4.7	—	—	μs
Minimum data hold time	$t_{HD;DAT}$		120	—	—	ns
Minimum data preparation time	$t_{SU;DAT}$		650	—	—	ns
Rise time	t_R		—	—	1	μs
Fall time	t_F		—	—	300	ns
Minimum waiting time for stop preparation	$t_{SU;STO}$		4.7	—	—	μs

Electrical Characteristics Measurement Circuit



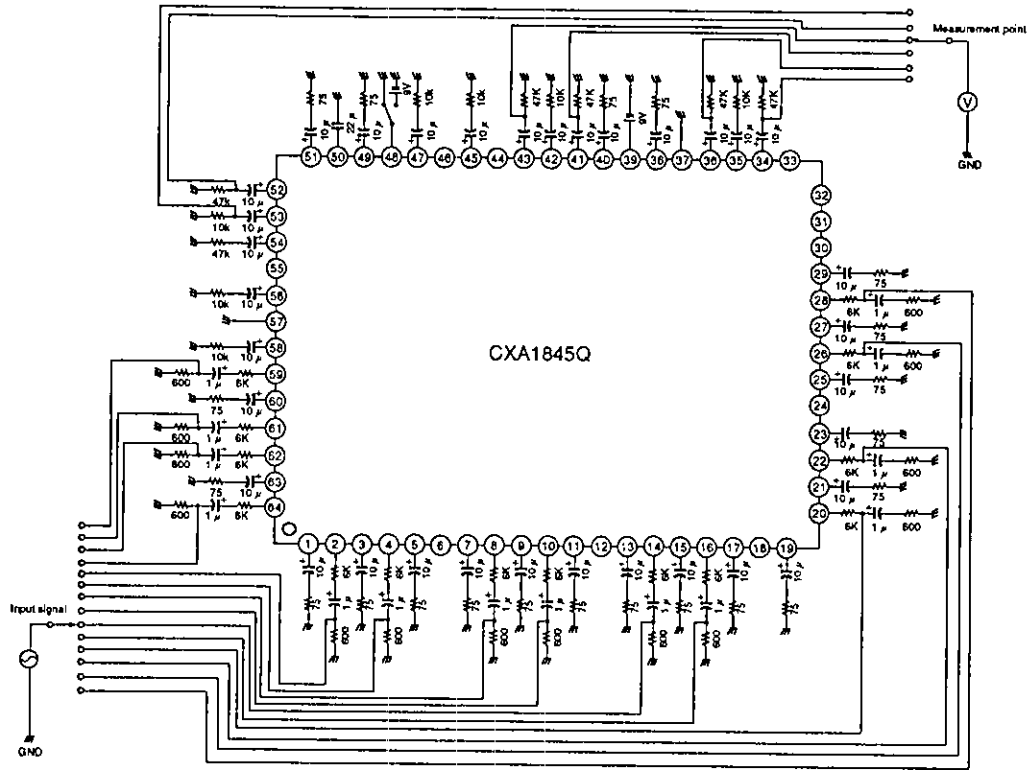
Signal is input from one of the following pins: ①, ③, ⑤, ⑦, ⑨, ⑪, ⑬, ⑮, ⑰, ⑲, ㉑, ㉓, ㉕, ㉗, ㉙, ㊵, ㊸
Output signal is measured from one of the following pins: ㉟, ㊷, ㊺, ㊼, ㊸, ㊻, ㊽

Fig. 1 Video system (gain, frequency response characteristics, input dynamic range)



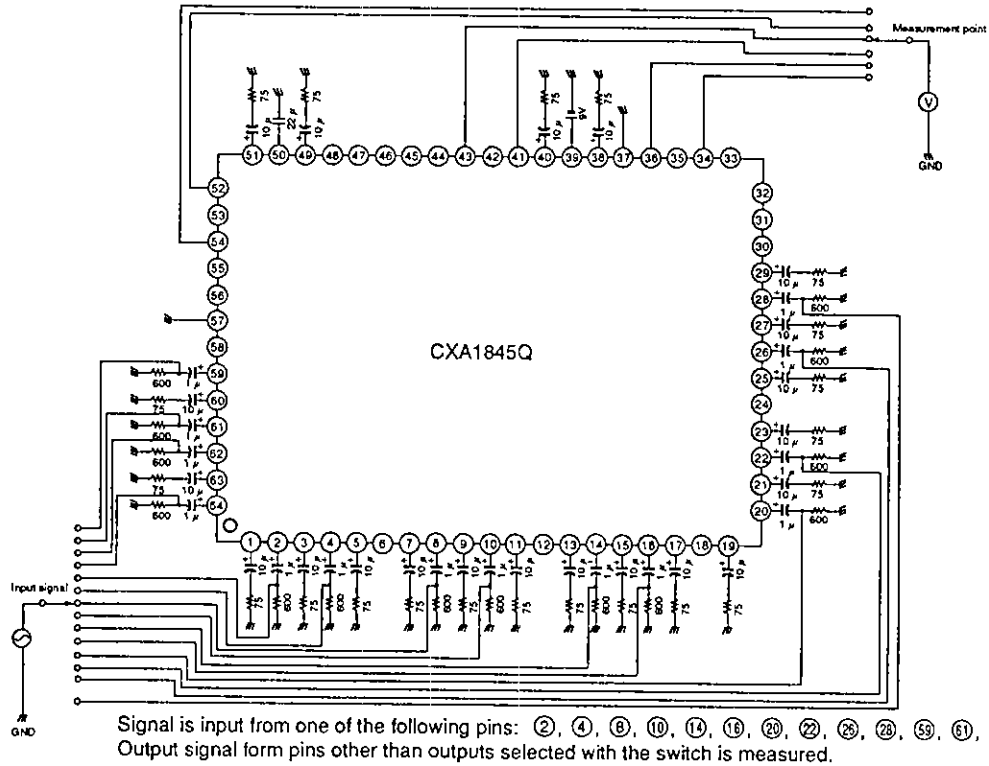
Signal is input from one of the following pins: ①, ③, ⑤, ⑦, ⑨, ⑪, ⑬, ⑮, ⑰, ⑲, ㉑, ㉓, ㉕, ㉗, ㉙, ㊵, ㊸
Output signal from pins other than outputs selected with the switch is measured.

Fig. 2 Video system (cross talk)



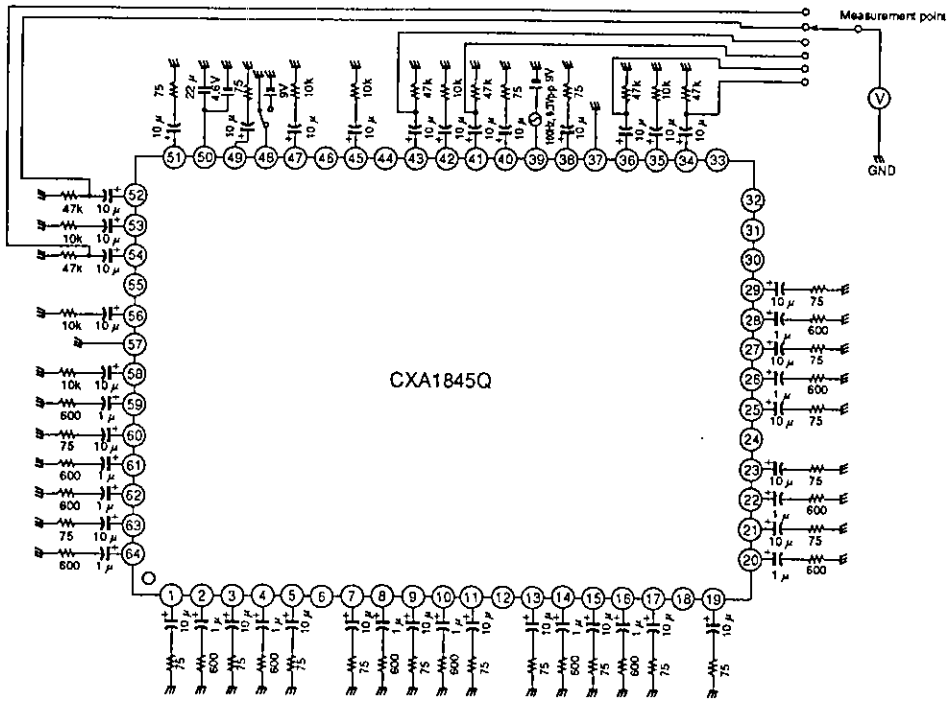
Signal is input from one of the following pins: ②, ④, ⑧, ⑩, ⑭, ⑯, ⑳, ㉒, ㉖, ㉘, ㊾, ㊶, ㊷, ㊹
Output signal is measured from one of the following pins: ㉞, ㉟, ㊶, ㊸, ㊷, ㊹
When 9V is applied to Pin ㊽, the signals from Pins ㊷ and ㊹ can be measured for output gain of −6dB.

Fig. 3 Audio system (gain, frequency response characteristics, total harmonic distortion, input dynamic range)



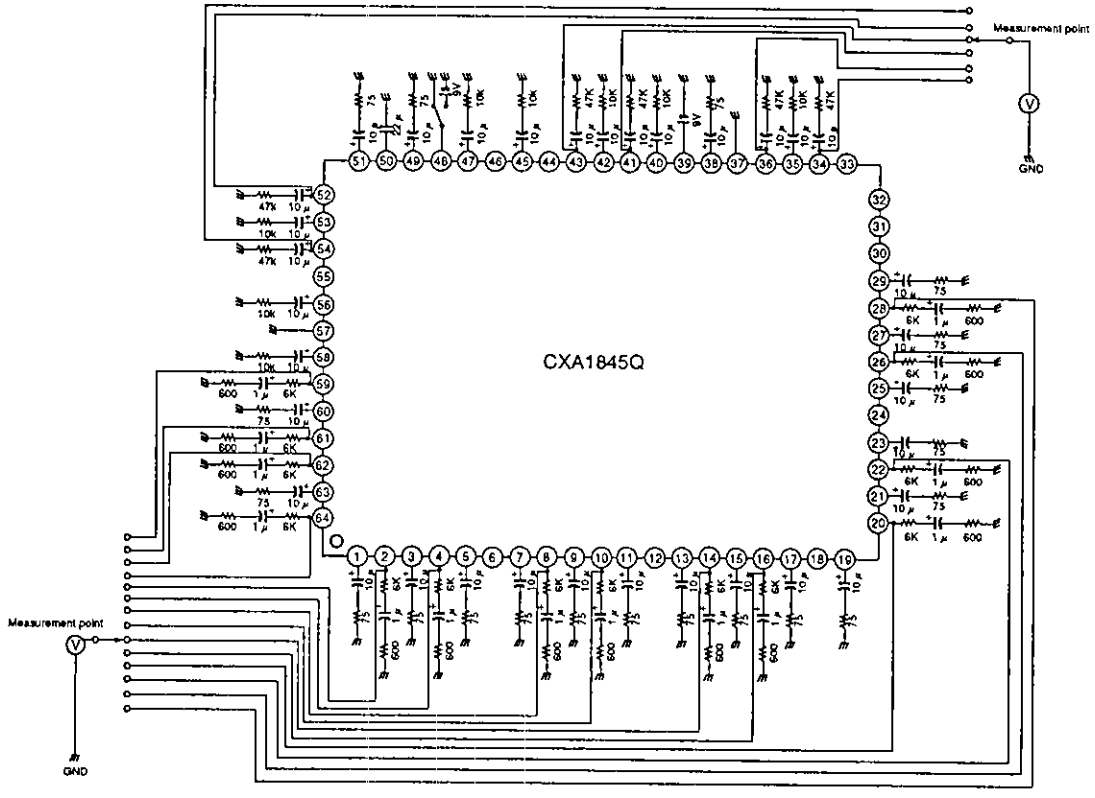
Signal is input from one of the following pins: ②, ④, ⑧, ⑩, ⑭, ⑯, ⑳, ㉒, ㉖, ㉘, ㊾, ㊶, ㊷, ㊹
Output signal form pins other than outputs selected with the switch is measured.

Fig. 4 Audio system (cross talk)



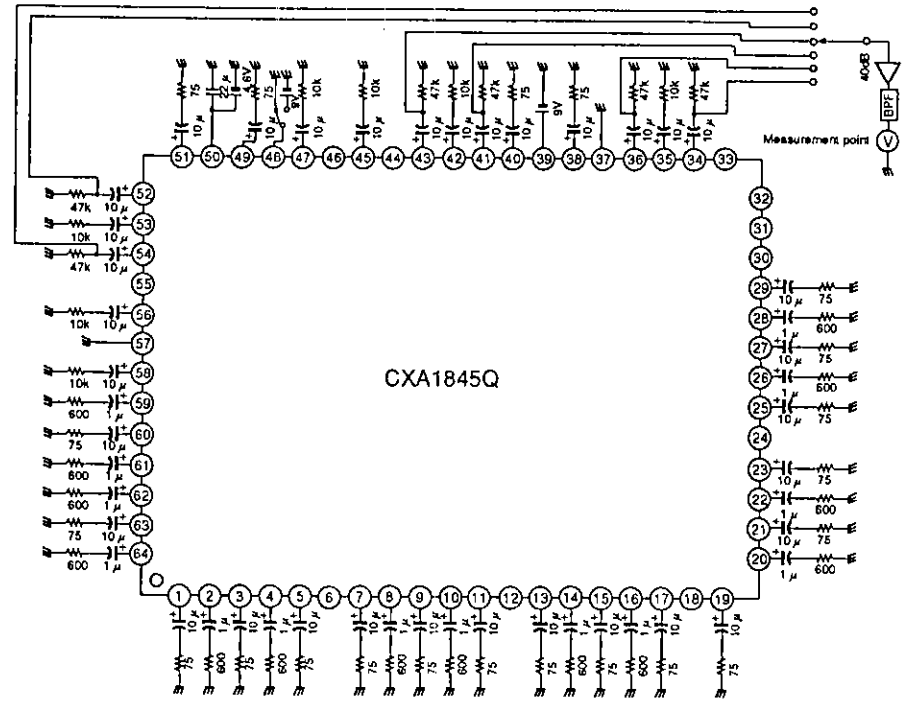
A f=100Hz, 0.3Vp-p signal is applied to Vcc and the output signals from Pins ㉞, ㉟, ㊶, ㊸, ㊷ and ㊹ are measured.
When 9V is applied to Pin ㊽, the signals from Pins ㊷ and ㊹ can be measured for output gain of −6dB.

Fig. 5 Audio system (ripple rejection)



When 9V is applied to Pin ㊽, the signals from Pins ㊷ and ㊹ can be measured for output gain of −6dB.

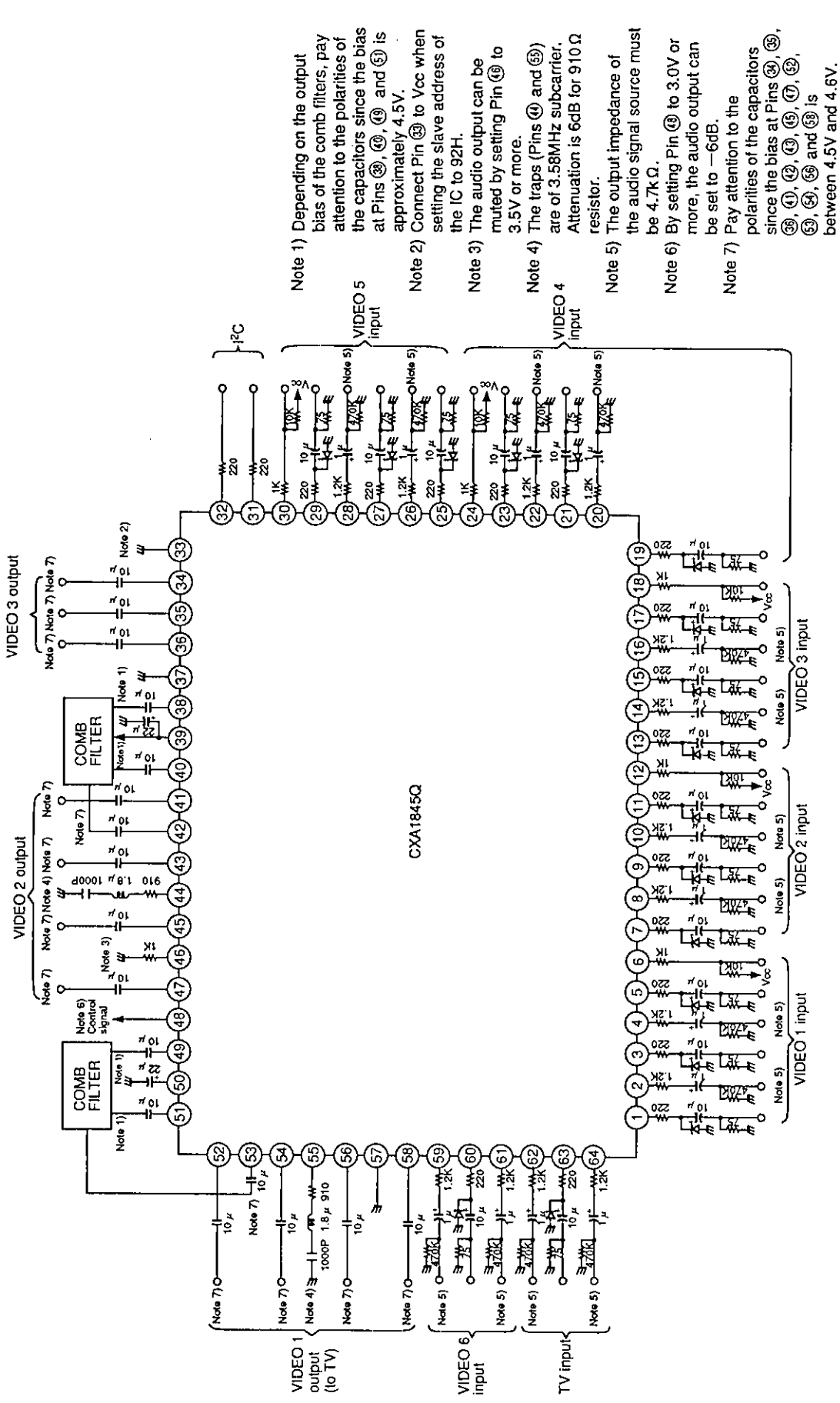
Fig. 6 Audio system (output DC offset)



When 9V is applied to Pin ㊽, the signals from Pins ㊿ and ㉞ can be measured for output gain of −6dB.

Fig. 7 Audio system (residual noise)

Application Circuit



Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

I²C Bus Control Signal

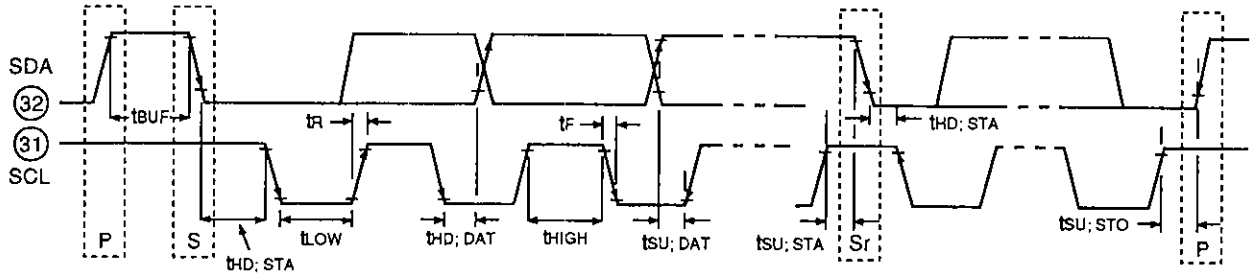


Fig. 7

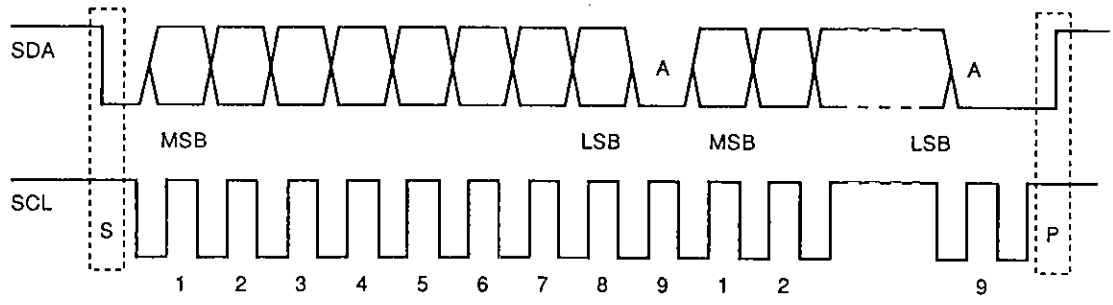
Description of Operation

The CXA1845Q is a TV I²C bus-compatible AV switch IC. The video system and the stereo audio system both have 7 inputs and 3 outputs each. Each video output is provided with a built-in 6dB amplifier. Desired inputs can be independently assigned to all outputs (in the audio system, the left and right channels are processed as one unit) by I²C bus control.

I²C Bus Registers

① I²C Bus

The I²C bus (Inter-IC bus) is an inter-IC bus system developed by Phillips.
Two wires (SDA-serial data, SCL-serial clock) provide control over start, stop, data transfer, synchronization, and collision avoidance. The IC outputs are either open collector or open drain, forming a bus line in the wired OR format.



S: Start condition; SDA is set at "Low" when SCL is "High"
P: Stop condition; SDA is set at "High" when SCL is "High"
A: Acknowledge signal sent from the slave

Data is transmitted by MSB-first. One data unit consists of 8 bits, to which the acknowledge signal, which indicates that the data has been accepted by the slave, is attached at the end. Normally, the slave*1 IC receives data at the rising edge of SCL and the master*2 IC changes data at the falling edge of SCL.

*1 Slave: An IC that is placed under the control of the master. In a normal system, all devices excluding the central microcomputer are slaves.
*2 Master: A central microcomputer or other controlling IC.

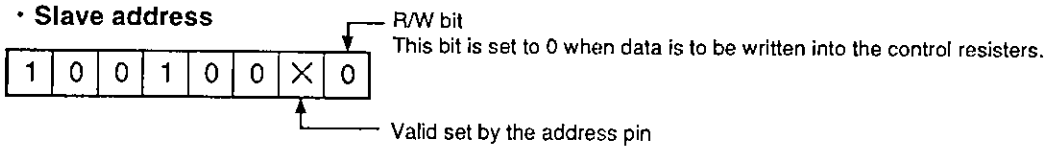
② Control Registers

The CXA1845Q control is exercised by writing 3-byte data into the three 8-bit control registers which control the 3 outputs selector circuits.

S	Slave address	A	DATA1	A	DATA2	A	DATA3	A	P

S: Start condition
A: Acknowledge
P: Stop condition

· Slave address



DATA1 Provides video 1 output control
DATA2 Provides video 2 output control
DATA3 Provides video 3 output control

· Control register structure (DATA1 to DATA3)

b7	b6	b5	b4	b3	b2	b1	b0
S CONT (2)		VIDEO (3)			AUDIO (3)		

Parenthesized numbers indicate the number of bits

Each register is set to 0 upon power ON.

Video switch control (VIDEO)

b5	b4	b3	Input signal selected
0	0	0	Mute
0	0	1	TV
0	1	0	V1
0	1	1	V2
1	0	0	V3
1	0	1	V4
1	1	0	V5
1	1	1	V6

V1 system; V1, Y1, C1
V2 system; V2, Y2, C2
V3 system; V3, Y3, C3
V4 system; V4, Y4, C4
V5 system; V5, Y5, C5
V6 system; V6

Audio switch control (AUDIO)

b2	b1	b0	Input signal selected
0	0	0	Mute
0	0	1	RTV/LTV
0	1	0	RV1/LV1
0	1	1	RV2/LV2
1	0	0	RV3/LV3
1	0	1	RV4/LV4
1	1	0	RV5/LV5
1	1	1	RV6/LV6

S input control (S CONT)

b7	b6	Output pin
0	X	Selected by S1 to 5 pins
1	0	Selects composite input.
1	1	Selects S input.

Composite input: TV, V1 to V6
S input: Y1 to Y5, C1 to C5

Note 1) When "b7" is set to 0, the S input/composite input is automatically switched by the voltages at S1 to 5 pins.

Note 2) The YOUT1/2 and COUT1/2 switches are also switched by this control.
Low: S input
High: Composite input

③ Status Registers

S	Slave address	A	DATA1	A	DATA2	NA	P

S	Slave address	A	DATA1	NA	P

S: Start condition
A: Acknowledge
P: Stop condition
NA: No acknowledge

When communication is to be terminated in the status register reading mode, the "no acknowledge" signal is needed to assure that the master does not issue the acknowledge signal to slave. Only DATA1 of status register can be read if NA is sent after DATA1.

• **Slave address**

1	0	0	1	0	0	X	1

R/W bit
This bit is set to 1 when the status register is to be read.

Value set by the address pin

• **DATA**

	b7			b4	b3	b2	b1	b0
DATA1	PONRES	X	X	S5 SEL	S4 SEL	S3 SEL	S2 SEL	S1 SEL
DATA2	PONRES	X	X	S5 OPEN	S4 OPEN	S3 OPEN	S2 OPEN	S1 OPEN

PONRES

When the CXA1845Q is reset upon power ON, logical 1 is returned. Once a read operation is completed, logical 0 is returned.

S1 to S5 OPEN

0: S1 to S5 pins are not open.

1: S1 to S5 pins are open.

S1 to S5 SEL

0: S1 to S5 pins are not grounded.

1: S1 to S5 pins are grounded.

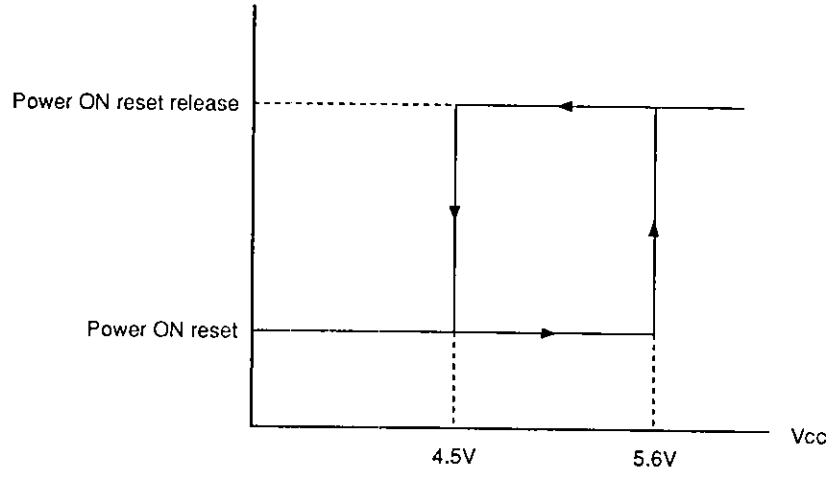
In actually, the logic states of the S1 to S5 OPEN and the S1 to S3 SEL bits are determined by comparing the DC voltages of S1 to S5 pins to two threshold values.

DC voltage of S1 to S5 pins	S1 to S5 OPEN	S1 to S5 SEL
0.8 V or less	0	1
1.3 V or more, 3.5 V or less	0	0
4.5 V or more	1	0

④ Power ON reset

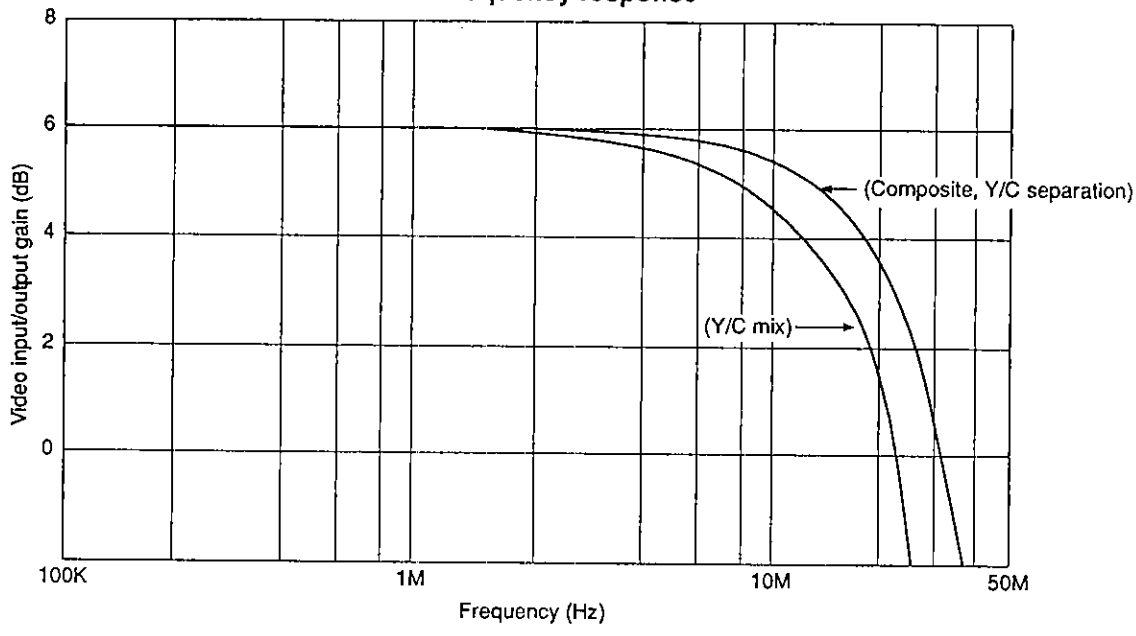
The CXA1845Q incorporates the power ON reset function. Therefore, each control register is reset to 0 upon power ON.

The power ON reset V_{TH} is hysteretical. The PONRES bit of the status register is read to determine whether the IC is reset upon power ON.

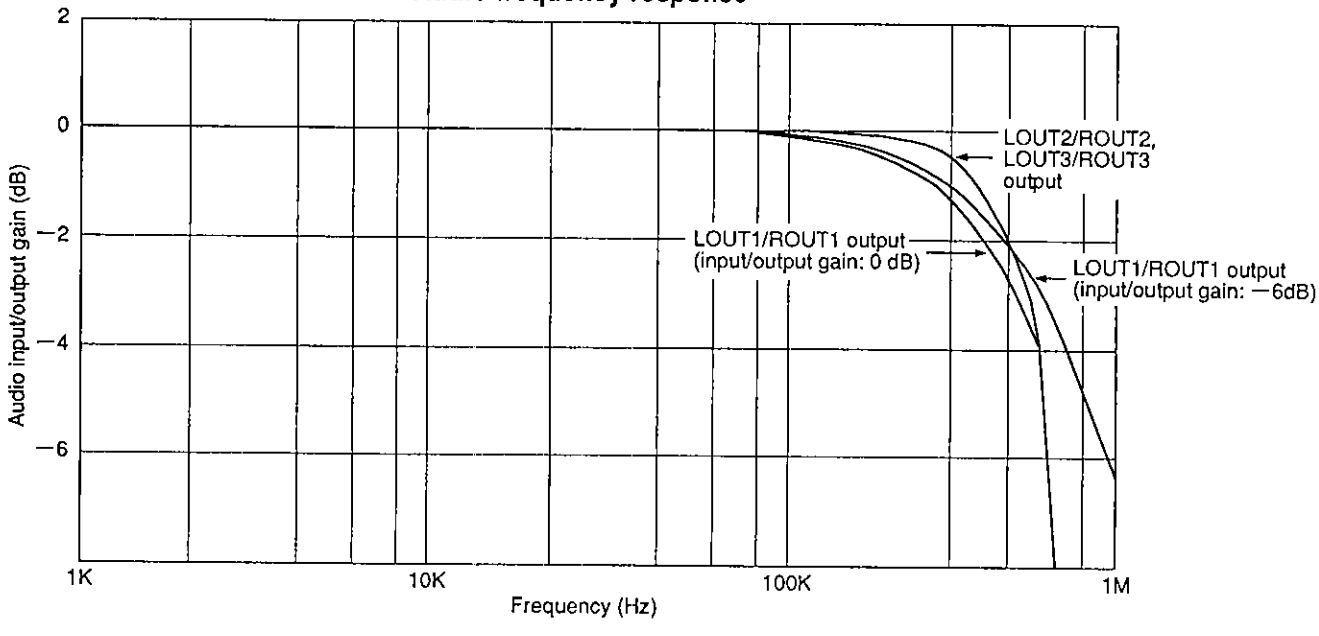


Example of Representative Characteristics

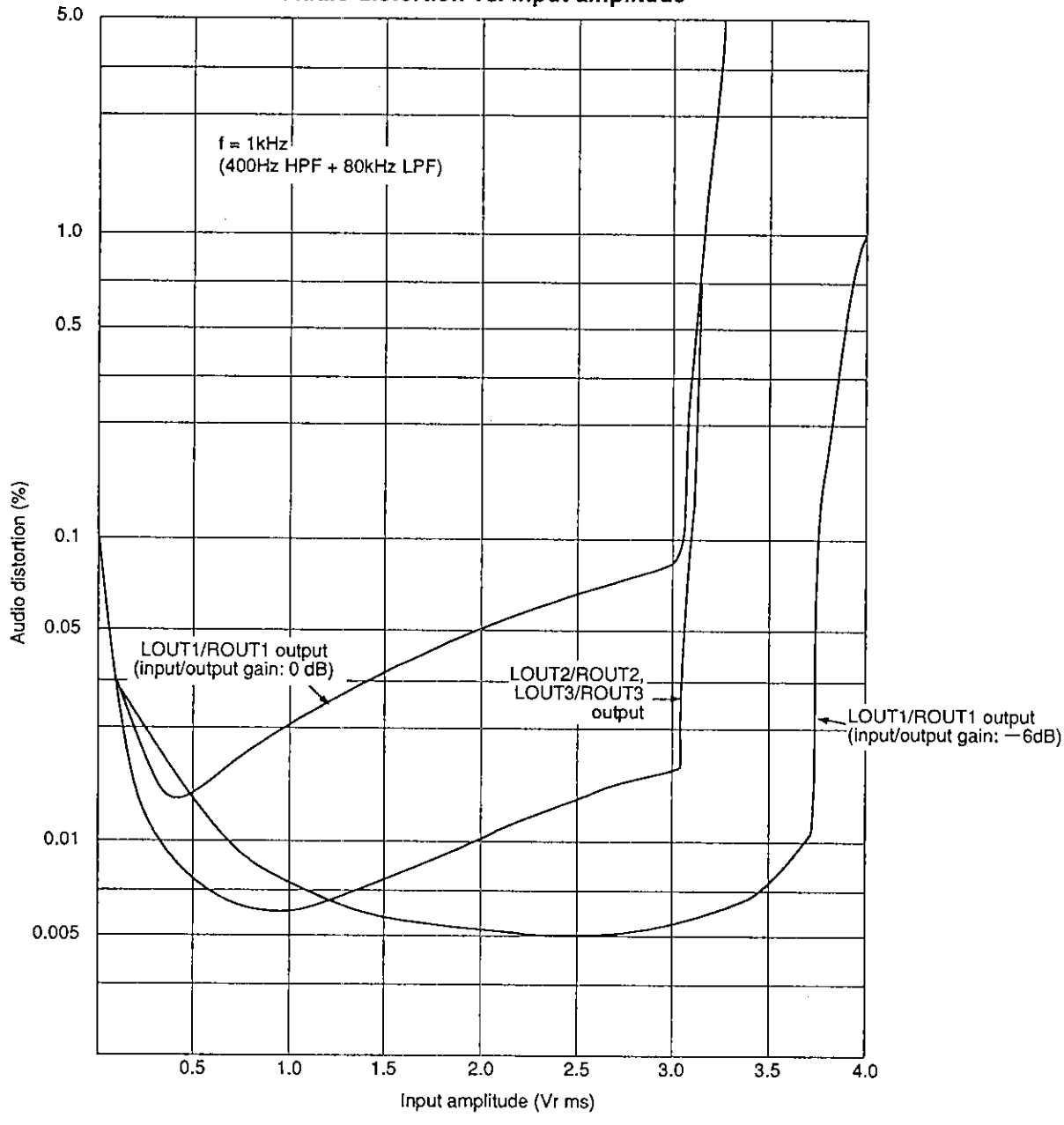
Video frequency response



Audio frequency response



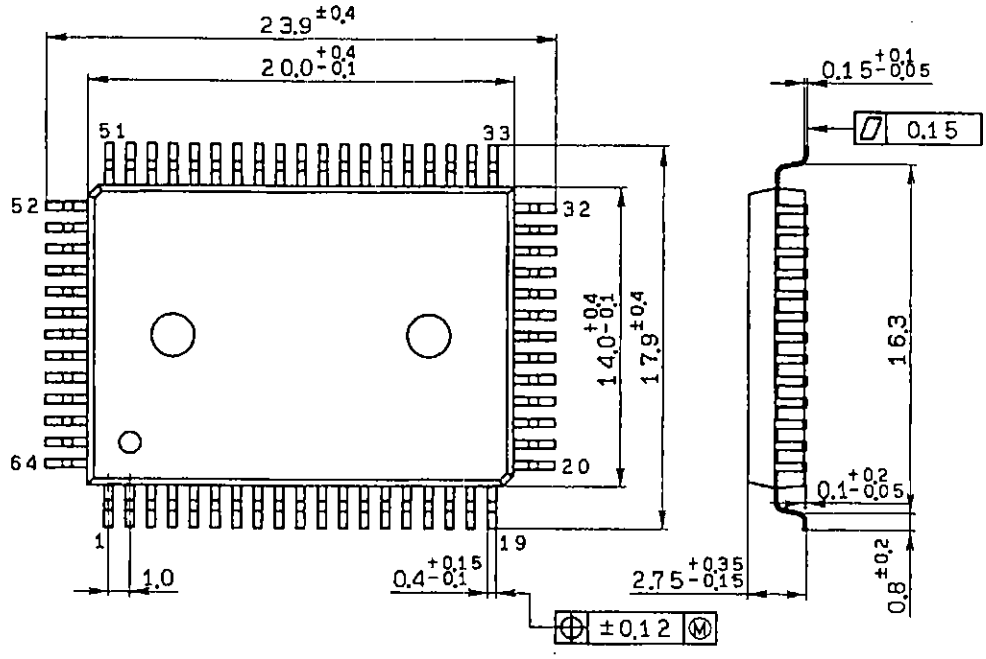
Audio distortion vs. Input amplitude



Package Outline

Unit: mm

64pin QFP (Plastic) 1.5g



SONY NAME	QFP-64P-L01
EIAJ NAME	*QFP064-P-1420-A
JEDEC CODE	———