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**MSM66509/66P509**

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**OLMS-66K Series 16-Bit Microcontroller**

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**GENERAL DESCRIPTION**

The MSM66509/66P509 is a high-performance 16-bit microcontroller that employs OKI original nX-8/500 CPU core.

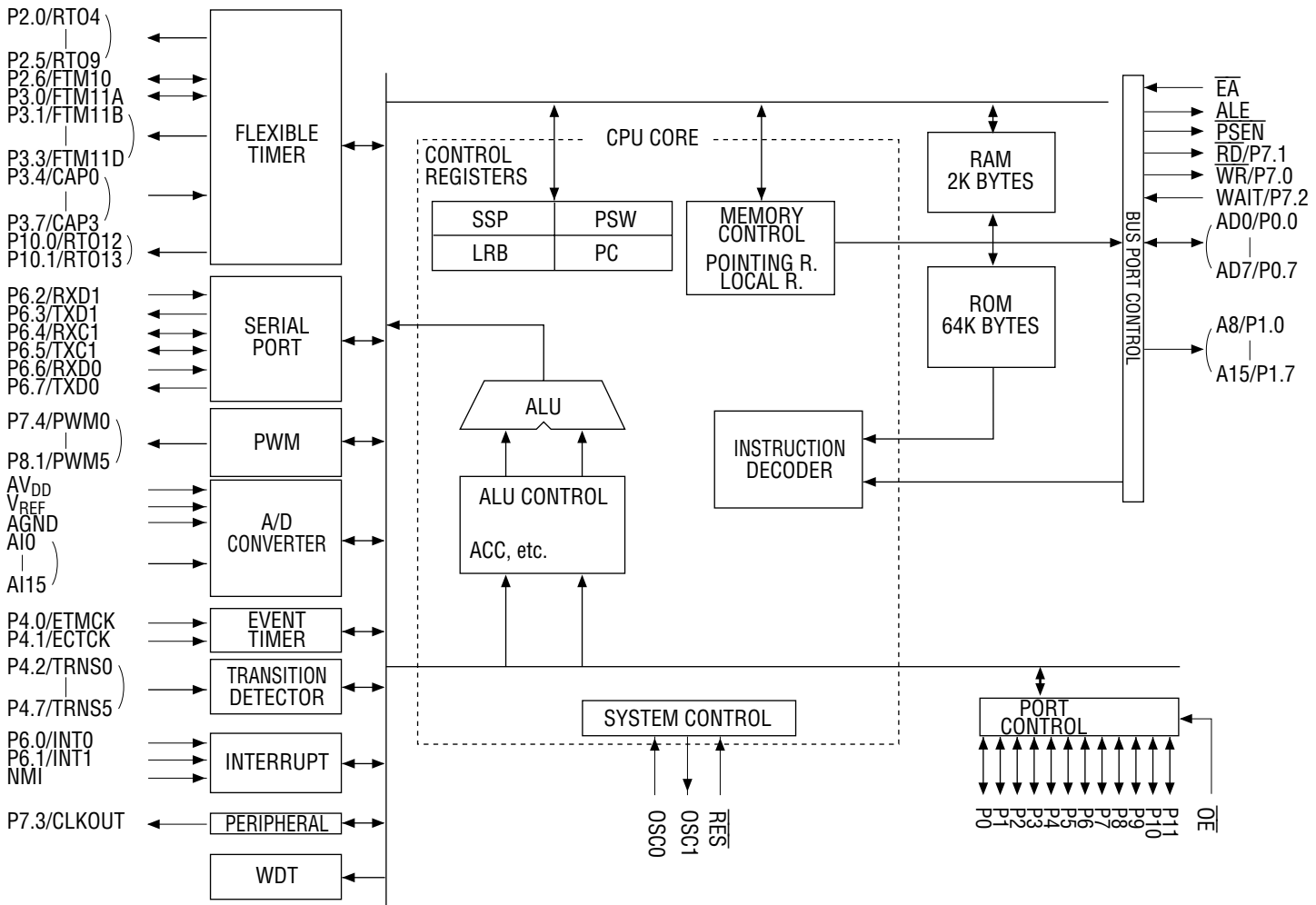
The MSM66509/66P509 includes a 16-bit CPU, ROM, RAM, a 10-bit A/D converter, serial ports, flexible timers, pulse-width modulator (PWM), and I/O ports.

**FEATURES**

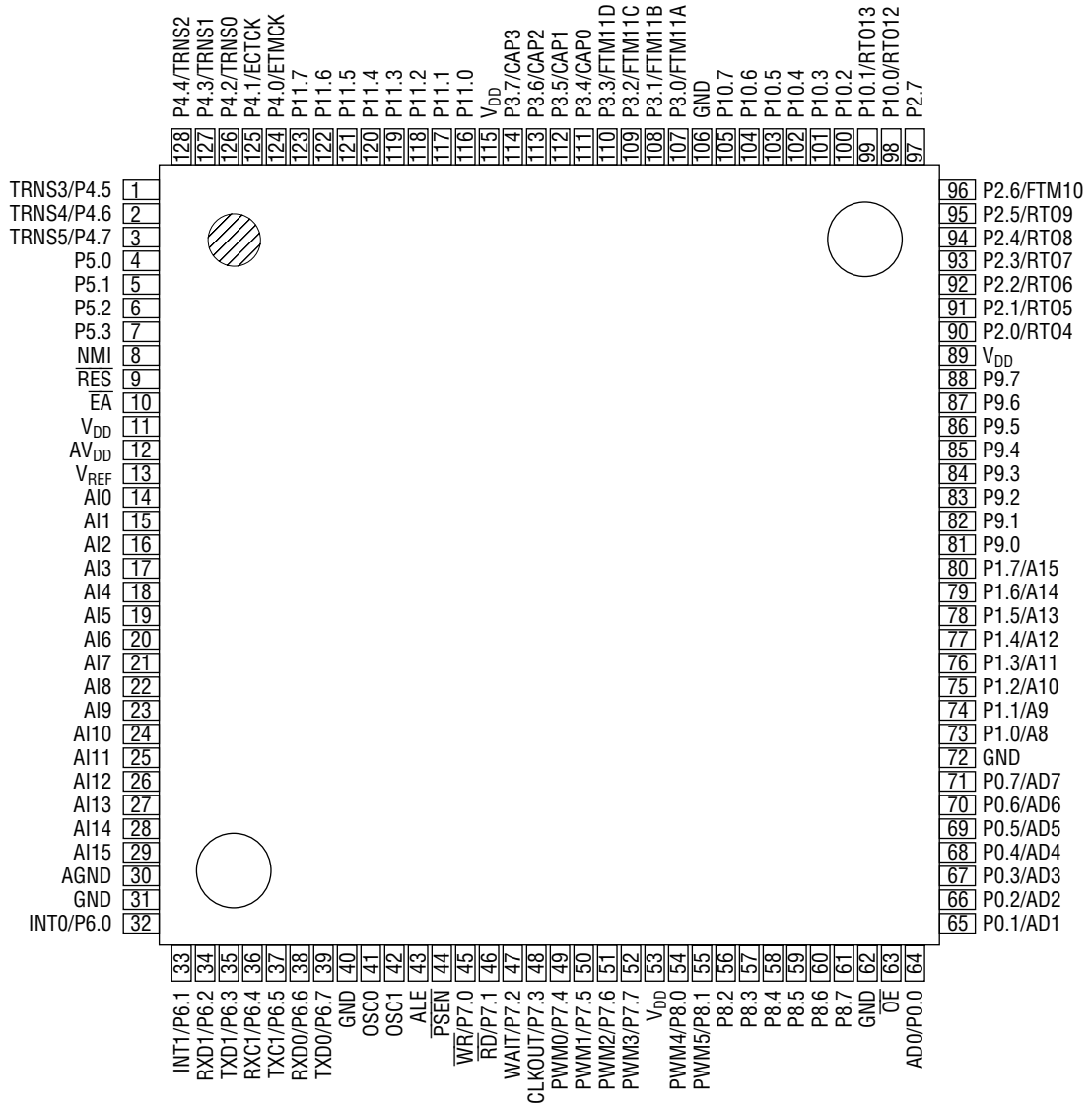
- Program memory space : 64K bytes
  - Internal ROM : 64K bytes
- Data memory space : 64K bytes
  - Internal RAM : 2K bytes
- High-speed execution
  - Minimum instruction execution time : 125nsec @ 32MHz
- Powerful instruction set : Instruction set superior in orthogonal matrix
  - 8/16-bit data transfer instructions
  - 8/16-bit arithmetic instructions
  - Multiplication and division operation instructions
  - Bit manipulation instructions
  - Bit logic instructions
  - ROM table reference instructions
- Abundant addressing modes : Register addressing
  - Page addressing
  - Pointing register indirect addressing
  - Stack addressing
  - Immediate addressing
- I/O port
  - Analog input port : 1 port × 16 bits
  - Input-output port : 11 ports × 8 bits, 1 port × 4 bits
  - (Input/output setting available in bit unit)
- Flexible timers
  - Free run counters : 19-bit × 1, 16-bit × 1
  - 19-bit CAP with a divider : 4
  - 16-bit double buffer RTO : 6
  - 16-bit PWM/RTO : 2
  - 16-bit CAP/RTO : 2
- 8-bit general timer : 1
  - 8-bit event counter : 1
- 16-bit PWM : 6
  - Input clock divider : 4
- Serial ports
  - UART mode with BRG : 1
  - Synchronous/UART switchable mode with BRG : 1
- 10-bit A/D converter : 16 channels

- Transition detector : 6
- Watchdog timer : 1
- Interrupts
  - Non-maskable : 1
  - Maskable : Internal 32/external 2  
(4-level priority can be set)
- ROM window function
- Standby modes
  - HALT mode
  - STOP mode
- Package
  - 128-pin plastic QFP (QFP128-P-2828-0.80-BK): (Product name: MSM66509-xxxGS-BK)  
xxx indicates the code number.

**BLOCK DIAGRAM**



**PIN CONFIGURATION (TOP VIEW)**



**128-Pin Plastic QFP**

**PIN DESCRIPTIONS**

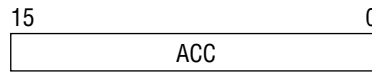
Symbol	Type	Description
P0.0-P0.7/ AD0-AD7	I/O	P0: 8-bit Input-output port. Each bit can be assigned to be an input or an output. AD: When an external memory is used, these pins output the lower 8 bits of the address. These pins also input or output the data.
P1.0-P1.7/ A8-A15	I/O	P1: 8-bit Input-output port. Each bit can be assigned to input or output. A: When an external memory is used, these pins output the upper 8 bits of the address.
P2.0-P2.5/ RT04-RT09 P2.6/FTM10 P2.7	I/O	P2: 8-bit Input-output port. Each bit can be assigned to input or output. RT0: Output pin for real time output FTM10: Capture input pin or real-time output pin
P3.0-P3.3/ FTM11A-FTM11D P3.4-P3.7/ CAP0-CAP3	I/O	P3: 8-bit Input-output port. Each bit can be assigned to input or output. FTM11A: Capture input pin or real-time output pin FTM11B-D: 4-port real-time output pin CAP : Capture input pin
P4.0/ETMCK P4.1/ECTCK P4.2-P4.7/ TRNS0-TRNS5	I/O	P4: 8-bit Input-output port. Each bit can be assigned to input or output. ETMCK: External clock input pin of 8-bit general timer ECTCK: External clock input pin of 8-bit event counter TRNS: Transition detector input pin
P5.0-P5.3	I/O	P5: 4-bit Input-output port. Each bit can be assigned to input or output.
P6.0/INT0 P6.1/INT1 P6.2/RXD1 P6.3/TXD1 P6.4/RXC1 P6.5/TXC1 P6.6/RXD0 P6.7/TXD0	I/O	P6: 8-bit Input-output port. Each bit can be assigned to input or output. INT0, 1: External interrupt request input pin RXD1 : SCI1 Receiver data input pin TXD1 : SCI1 Transmitter data output pin RXC1 : SCI1 Receiver circuit clock pin TXC1 : SCI1 Transmitter circuit clock pin RXD0 : SCIO Receiver data input pin TXD0 : SCIO Transmitter data output pin
P7.0/ $\overline{WR}$ P7.1/ $\overline{RD}$ P7.2/WAIT P7.3/CLKOUT P7.4-P7.7/ PWM0-PWM3	I/O	P7: 8-bit Input-output port. Each bit can be assigned to input or output. $\overline{WR}$ : Write strobe output pin for external data memory $\overline{RD}$ : Read strobe output pin for external data memory WAIT: CPU wait request input pin when accessing external data memory CLKOUT: Output pin for supplying a clock to peripheral circuits PWM: PWM output pin
P8.0-P8.1/ PWM4-PWM5 P8.2-P8.7	I/O	P8: 8-bit Input-output port. Each bit can be assigned to input or output. PWM: PWM output pin
P9.0-P9.7	I/O	P9: 8-bit Input-output port. Each bit can be assigned to input or output.
P10.0-P10.1/ RT012-RT013 P10.2-P10.7	I/O	P10: 8-bit Input-output port. Each bit can be assigned to input or output. RT0: Output pin for real time output.
P11.0-P11.7	I/O	P11: 8-bit Input-output port. Each bit can be assigned to input or output.

**PIN DESCRIPTION (Continued)**

<b>Symbol</b>	<b>Type</b>	<b>Description</b>
AIO-AI15	I	Analog signal input pin for A/D converter
AV <sub>DD</sub>	I	Power supply input pin for A/D converter
V <sub>REF</sub>	I	Reference voltage input pin for A/D converter
AGND	I	GND input pin for A/D converter
OSC0	I	Basic clock oscillation pin
OSC1	0	Basic clock oscillation pin
ALE	0	Timing pulse output pin to latch the lower 8 bits of the address output from port 0 when the CPU accesses the external memory
$\overline{\text{PSEN}}$	0	Strobe pulse output pin to fetch to external program memory
$\overline{\text{OE}}$	I	When P0, P1, P7.4-P7.7, and P8-P11 are in an output state and $\overline{\text{OE}}$ pin is "H" level, the ports go to a high-impedance state. When P0, P1, P7.4-P7.7, and P8-P11 are in an output state and $\overline{\text{OE}}$ pin is "L" level, the ports output "H" or "L" level. However, when P0, P1, P7.4-P7.7, and P8-P11 are in an input state, these ports are not under the influence of $\overline{\text{OE}}$ pin.
NMI	I	Nonmaskable interrupt request input pin
$\overline{\text{RES}}$	I	Low-active RESET input pin
$\overline{\text{EA}}$	I	Normally set to "H" level. If set to "L" level, the program memory goes into external access mode and accesses external program memory
V <sub>DD</sub>	I	Power supply pin
GND	I	Ground pin

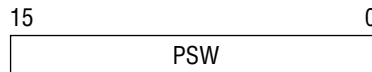
**REGISTERS**

**Accumulator**



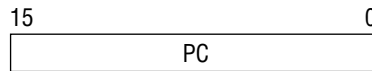
**Control Register (CR)**

Program Status Word



- Bit 15 : Carry flag (CY)
- Bit 14 : Zero flag (ZF)
- Bit 13 : Half carry flag (HC)
- Bit 12 : Data descriptor (DD)
- Bit 11 : Sign flag (S)
- Bit 10 : Master interrupt priority flag (MIP)
- Bit 9 : Overflow flag (OV)
- Bit 8 : Master interrupt enable flag (MIE)
- Bit 7-3 : User flag
- Bit 2-0 : System control base 2-0 (SCB2-0)

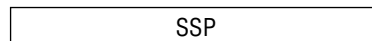
Program Counter



Local Register Base

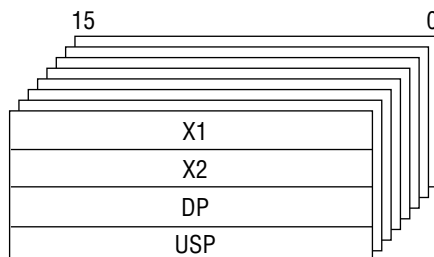


System Stack Pointer



**Pointing Register (PR)**

- Index Register 1
- Index Register 2
- Data pointer
- User Stack Pointer



**Local Register**

	7	0	7	0
ER0	R1		R0	
ER1	R3		R2	
ER2	R5		R4	
ER3	R7		R6	

SFR

Address [H]	Name	Symbol	R/W	8/16-bit Operation	Reset	
0000	System stack pointer	SSP	R/W	8/16	FF	
0001					FF	
0002	Local register base	LRBL	R/W		8	Undefined
0003		LRBH				
0004	Program status word	PSWL	R/W			00
0005		PSWH				00
0006	Accumulator	ACCL	R/W			00
0007		ACCH				00
0010	ROM window register	ROMWIN	R			00
0011☆	RAM ready control register	RAMRDY	R			FF
0012☆	ROM ready control register	ROMRDY	R			FF
0014	Stop code acceptor	STPACP	W			"0"
0015☆	Standby control register	SBYCON	R/W			C8
0018☆	Peripheral control register	PRPHF	R/W			*
001C	Watchdog timer	WDT	W			Halt
001D☆	TBC clock dividing counter	TBCKDVC	R			F0
001E☆	TBC clock dividing register	TBCKDVR	R	F0		
0020	Port 0 data register	P0	R/W	8/16		00
0021	Port 1 data register	P1			00	
0022	Port 2 data register	P2			00	
0023	Port 3 data register	P3			00	
0024	Port 4 data register	P4			00	
0025☆	Port 5 data register	P5			F0	
0026	Port 6 data register	P6			00	
0027	Port 7 data register	P7			00	
0028	Port 0 mode register	P0IO			00	
0029	Port 1 mode register	P1IO			00	
002A	Port 2 mode register	P2IO			00	
002B	Port 3 mode register	P3IO			00	
002C	Port 4 mode register	P4IO			00	
002D☆	Port 5 mode register	P5IO			F0	
002E	Port 6 mode register	P6IO			00	
002F	Port 7 mode register	P7IO			00	

Note: A ☆ mark in the address column indicates that there is a bit that does not exist in the register.

- \* The initial values of PRPHF (SFR=18H) are as follows :  
 When RES pin is reset : VBFF (bit 6) is set to "1" and CKOUT1 or 0 is set to "0".  
 When WDT, BRK instruction, and operation code trap are reset : VBFF (bit 6) keeps the value just before it is reset and CKOUT 1 or 0 is set to "0". In any case, the state of OE pin is read for OERD (bit 7).



SFR (Continued)

Address [H]	Name	Symbol	R/W	8/16-bit Operation	Reset		
0031	Port 1 secondary function control register	P1SF	R/W	8	00		
0032☆	Port 2 secondary function control register	P2SF		8/16	80		
0033	Port 3 secondary function control register	P3SF		00			
0034	Port 4 secondary function control register	P4SF		8	00		
0036	Port 6 secondary function control register	P6SF		8/16	00		
0037	Port 7 secondary function control register	P7SF			00		
0038	TRNS control register 0	TRNSCON0			00		
0039☆	TRNS control register 1	TRNSCON1			F0		
003A☆	Transition detector	TRANSIT		8	C0		
003C☆	Port 8 secondary function control register	P8SF		R/W	8/16	FC	
003D☆	Port 10 secondary function control register	P10SF				FC	
0040	Interrupt request register 0	IRQOL				00	
0041		IRQOH				00	
0042	Interrupt request register 1	IRQ1L				00	
0043☆		IRQ1H				F8	
0044	Interrupt enable register 0	IE0L				00	
0045		IE0H				00	
0046	Interrupt enable register 1	IE1L				00	
0047☆		IE1H				F8	
0048	Interrupt request flag disable register 0	IRQD0L				00	
0049		IRQD0H				00	
004A	Interrupt request flag disable register 1	IRQD1L				00	
004B☆		IRQD1H				F8	
004E☆	NMI control register	NMICON					FC or 7C
004F☆	External interrupt control register	EXICON					F0
0050	Interrupt priority control register 00	IP00L				00	
0051		IP00H				00	
0052	Interrupt priority control register 01	IP01L				00	
0053		IP01H				00	
0054	Interrupt priority control register 10	IP10L				00	
0055☆		IP11H				F8	
0056	Interrupt priority control register 11	IP11L				00	
0057☆		IP11H	F8				
0058	Port 8 data register	P8				00	
0059	Port 9 data register	P9				00	
005A	Port 10 data register	P10				00	
005B	Port 11 data register	P11				00	
005C	Port 8 mode register	P8IO				00	
005D	Port 9 mode register	P9IO				00	
005E	Port 10 mode register	P10IO				00	
005F	Port 11 mode register	P11IO				00	

Note: A ☆ mark in the address column indicates that there is a bit that does not exist in the register.

SFR (Continued)

Address [H]	Name	Symbol	R/W	8/16-bit Operation	Reset		
0060	SCI0 timer counter	S0TM	R/W	8/16	00		
0061	SCI0 timer register	S0TMR			00		
0062☆	SCI0 timer control register	S0CON		8	02		
0063☆	SCI0 transmission control register	ST0CON			82		
0064☆	SCI0 reception control register	SR0CON			12		
0065	SCI0 transmission and reception buffer register	S0BUF			Undefined		
0066	SCI0 status register	S0STAT			00		
0068	SCI1 timer counter	S1TM			8/16	00	
0069	SCI1 timer register	S1TMR		00			
006A☆	SCI1 timer control register	S1CON		8	02		
006B☆	SCI1 transmission control register	ST1CON			80		
006C	SCI1 reception control register	SR1CON			00		
006D	SCI1 transmission and reception buffer register	S1BUF			Undefined		
006E	SCI1 status register	S1STAT			00		
0070☆	8-bit general timer control register	GTMCON			30		
0071	8-bit event counter	GEVC		00			
0072	8-bit general timer counter	GTMC		8/16	00		
0073	8-bit general timer register	GTMR			00		
0074	PWM counter 0	PWC0		R	16	0000	
0075						0000	
0076	PWM counter 1	PWC1				0000	
0077						0000	
0078	PWM counter 2	PWC2				0000	
0079			0000				
007A	PWM counter 3	PWC3	0000				
007B			0000				
007C	PWM counter 4	PWC4	0000				
007D			0000				
007E	PWM counter 5	PWC5	0000				
007F			0000				
0080	PWR0 buffer register	PW0BF	R/W	8/16	00		
0081					00		
0082	PWR1 buffer register	PW1BF			00		
0083					00		
0084	PWR2 buffer register	PW2BF			00		
0085					00		
0086	PWR3 buffer register	PW3BF			00		
0087					00		
0088	A/DC result register 10	ADCR10			R	*8/16	Undefined
0089	A/DC result register 11	ADCR11					
008A	A/DC result register 12	ADCR12					
008B	A/DC result register 13	ADCR13					
008C	A/DC result register 14	ADCR14					
008D	A/DC result register 15	ADCR15					
008E	A/DC result register lower 3 bits	LADCR3					
008F	A/DC result register lower 4 bits	LADCR4					

Note: A ☆ mark in the address column indicates that there is a bit that does not exist in the register.

\* 8/16 means a special word manipulation. (For details, refer to the User's Manual.)

SFR (Continued)

Address [H]	Name	Symbol	R/W	8/16-bit Operation	Reset	
0090	PWR4 buffer register	PW4BF	R/W	8/16	00	
0091					00	
0092	PWR5 buffer register	PW5BF			00	
0093					00	
0094	TMR12 buffer register	TMR12BF			00	
0095					00	
0096	TMR13 buffer register	TMR13BF			00	
0097					00	
0098	PWM interrupt control register	PWINTCON			00	
0099☆	PWM interrupt control register 1	PWINTCON1			CC	
009A	PWM control register 0	PWCON0			00	
009B	PWM control register 1	PWCON1			00	
009C	PWM clock counter	PWDVC			00	
009D	PWM clock register	PWDVR			00	
009E☆	PWM run register	PWRUN			00	
009F☆	PWM active register	PWACT			C0	
00A0	Timer register 0	TMR0		R/W	16	0000
00A1						0000
00A2	Timer register 1	TMR1				0000
00A3						0000
00A4	Timer register 2	TMR2	0000			
00A5			0000			
00A6	Timer register 3	TMR3	0000			
00A7			0000			
00A8	Timer register 4	TMR4	0000			
00A9			0000			
00AA	Timer register 5	TMR5	0000			
00AB			0000			
00AC	Timer register 6	TMR6	0000			
00AD			0000			
00AE	Timer register 7	TMR7	0000			
00AF			0000			
00B0	Timer register 8	TMR8	0000			
00B1			0000			
00B2	Timer register 9	TMR9	0000			
00B3			0000			
00B4	Timer register 10	TMR10	0000			
00B5			0000			
00B6	Timer register 11	TMR11	0000			
00B7			0000			
00B8☆	TMR0 lower 3 bits	TMR0L	1F			
00B9☆	TMR1 lower 3 bits	TMR1L	1F			
00BA☆	TMR2 lower 3 bits	TMR2L	1F			
00BB☆	TMR3 lower 3 bits	TMR3L	1F			
00BC	TM setting register	TMSELL	8/16	00		
00BD☆		TMSELH	C0			
00BE	PWM control register 2	PWCON2	8	00		

Note: A ☆ mark in the address column indicates that there is a bit that does not exist in the register.

SFR (Continued)

Address [H]	Name	Symbol	R/W	8/16-bit Operation	Reset
00C0	TMR4 buffer register	TMR4BF	R/W	8/16	00
00C1					00
00C2	TMR5 buffer register	TMR5BF			00
00C3					00
00C4	TMR6 buffer register	TMR6BF			00
00C5					00
00C6	TMR7 buffer register	TMR7BF			00
00C7					00
00C8	Timer control register	TMCON		8	00
00C9☆	Timer counter 0 lower 3 bits	TM0L			1F
00CA	Timer counter 0	TM0		8/16	00
00CB					00
00CC	Timer counter 1	TM1			00
00CD					00
00CE	Capture control register 0	CAPCON0			00
00CF☆	Capture control register 1	CAPCON1			F0
00D0☆	Event control register	EVNTCONL			88
00D1☆		EVNTCONH			88
00D2	TMR mode register	TMRMODE		8	00
00D4	Timer register 12	TMR12		16	0000
00D5					0000
00D6	Timer register 13	TMR13		8/16	00
00D7					00
00D8☆	Event dividing counter 0	EVDV0			C0
00D9☆	Event dividing counter 1	EVDV1			C0
00DA☆	Event dividing counter 2	EVDV2			C0
00DB☆	Event dividing counter 3	EVDV3			C0
00DC☆	EVDV0 buffer register	EVDV0BF			C0
00DD☆	EVDV1 buffer register	EVDV1BF	C0		
00DE☆	EVDV2 buffer register	EVDV2BF	C0		
00DF☆	EVDV3 buffer register	EVDV3BF	C0		
00E0	A/DC result register 0	ADCR0	R	*8/16	Undefined
00E1	A/DC result register 1	ADCR1			
00E2	A/DC result register 2	ADCR2			
00E3	A/DC result register 3	ADCR3			
00E4	A/DC result register 4	ADCR4			
00E5	A/DC result register 5	ADCR5			
00E6	A/DC result register 6	ADCR6			
00E7	A/DC result register 7	ADCR7			
00E8	A/DC result register 8	ADCR8			
00E9	A/DC result register 9	ADCR9			
00EA	A/DC result register lower 0	LADCR0			
00EB	A/DC result register lower 1	LADCR1			
00EC☆	A/DC result register lower 2	LADCR2			
00ED☆	A/D interrupt control register	ADINTCON			
00EE☆	A/DC control register L	ADCONL	80		
00EF☆	A/DC control register H	ADCONH	80		

Note: A ☆ mark in the address column indicates that there is a bit that does not exist in the register.

\* 8/16 means a special word manipulation. (For details, refer to the User's Manual.)

**SFR (Continued)**

Address [H]	Name	Symbol	R/W	8/16-bit Operation	Reset	
00F0☆	RTO control register 0	RTOCON0	R/W	8/16	F8	
00F1☆	RTO control register 1	RTOCON1			F8	
00F2☆	RTO control register 2	RTOCON2			F8	
00F3☆	RTO control register 3	RTOCON3			F8	
00F4☆	RTO control register 4	RTOCON4			FC	
00F5☆	RTO control register 5	RTOCON5			FC	
00F6☆	RTO control register 6	RTOCON6			F8	
00F7☆	RTO control register 7	RTOCON7			F8	
00F8	RTO control register 8	RTOCON8			00	
00F9☆	RTO control register 9	RTOCON9			F8	
00FA☆	RTO control register 10	RTOCON10		F8		
00FB☆	PWM clock counter 34 run register	PWDVRN		8	FC	
00FC	PWM clock counter 34	PWDVC34		8/16	00	
00FD	PWM clock register 34	PWDRC34			00	
00FE	Emulator using area*					
00FF						

Note: A ☆ mark in the address column indicates that there is a bit that does not exist in the register.

\* For the emulator using area, if the write is manipulated, the write data becomes invalid, and if the read is manipulated, the read data becomes undefined.

## ADDRESSING MODES

The MSM66509/66P509 provides independent 64K-byte data and 64K-byte program spaces with various types of addressing modes. These modes are shown below for both RAM (for data space) and ROM (for program space).

### RAM Addressing Mode (for data space)

- Register addressing

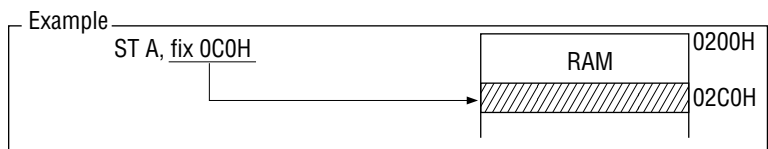


- Page addressing

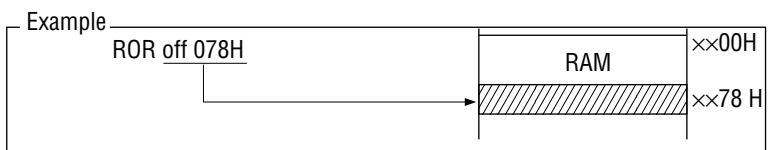
a) sfr page



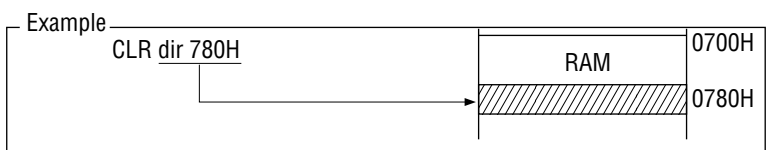
b) Fixed page



c) Current page

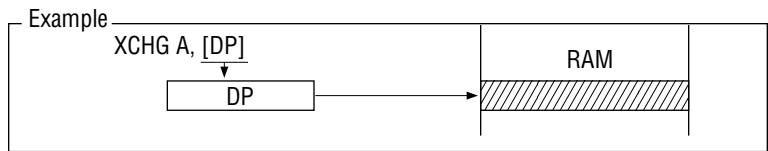


- Direct data addressing

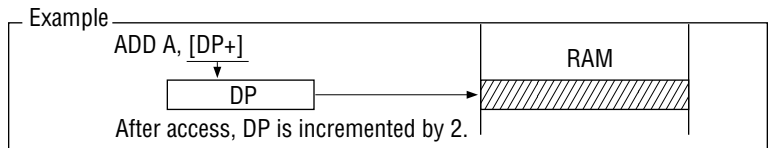


• Pointing register indirect addressing

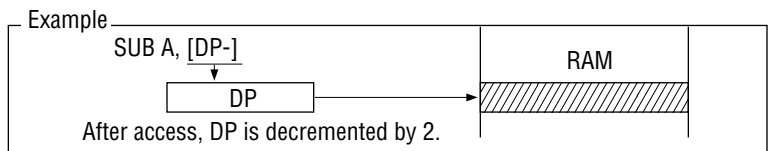
a) DP/X1 indirect



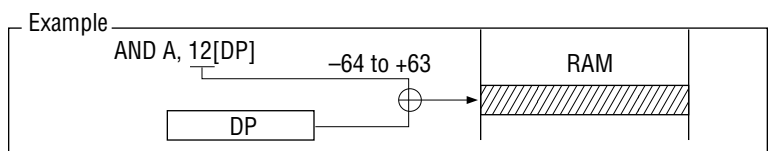
b) DP indirect with post increment



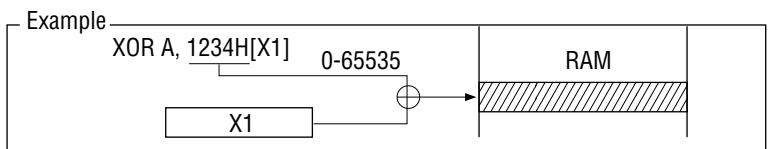
c) DP indirect with post decrement



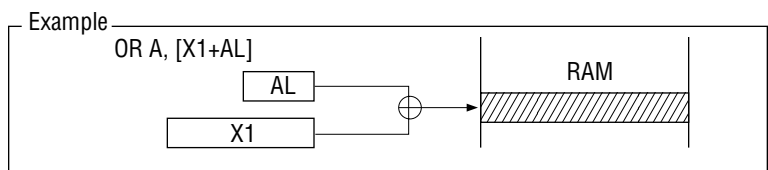
d) DP/USP indirect with 7-bit displacement



e) X1/X2 indirect with 16-bit base

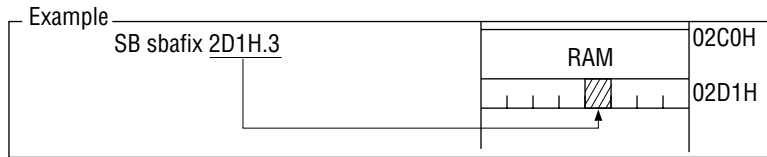


f) X1 indirect with 8-bit register (AL, R0) displacement

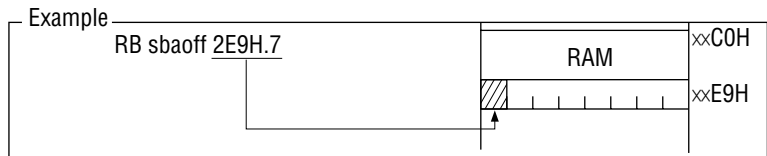


- **Special bit area addressing**

a) Fixed page SBA area (02C0H to 02FFH)

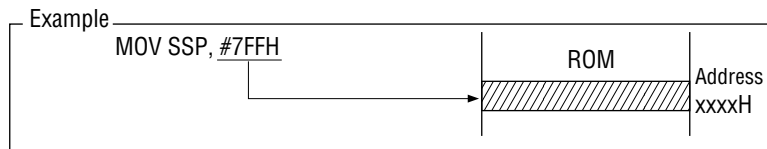


b) Current page SBA area (××C0H to ××FFH)



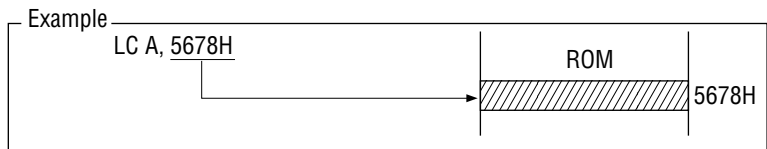
**ROM Addressing Mode (for program space)**

- **Immediate addressing**

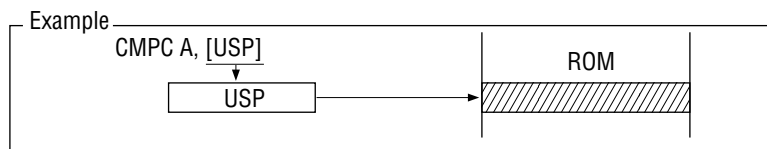


- **Table data addressing**

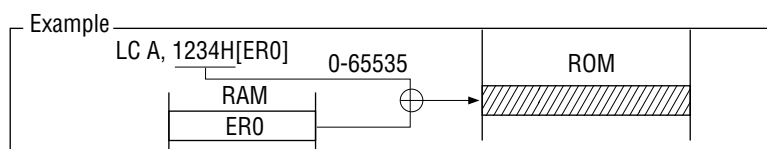
a) Direct



b) RAM addressing indirect



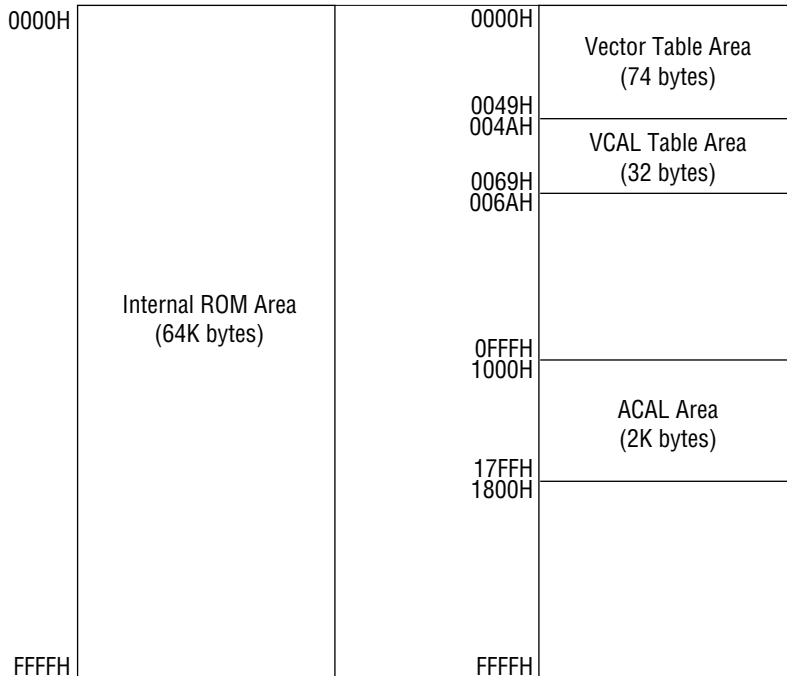
c) RAM addressing indirect with 16-bit base



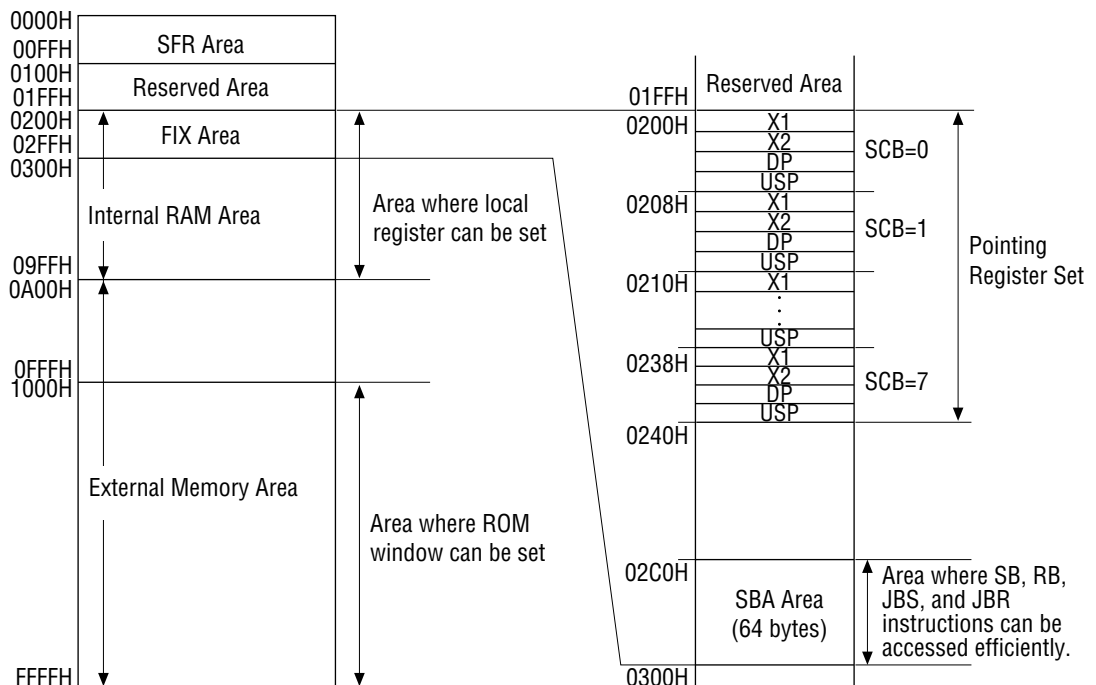


## MEMORY MAP

### Program Memory Space



### Data Memory Space



**ABSOLUTE MAXIMUM RATINGS**

(Ta=25°C)

Parameter	Symbol	Condition		Rating	Unit
Digital Power Supply Voltage	V <sub>DD</sub>	GND=AGND=0V		-0.3 to +7.0	V
Input Voltage	V <sub>I</sub>			-0.3 to V <sub>DD</sub> +0.3	
Output Voltage	V <sub>O</sub>			-0.3 to V <sub>DD</sub> +0.3	
Analog Power Supply Voltage	AV <sub>DD</sub>			-0.3 to V <sub>DD</sub> +0.3	
Analog Reference Voltage	V <sub>REF</sub>			-0.3 to AV <sub>DD</sub> +0.3	
Analog Input Voltage	V <sub>AI</sub>			-0.3 to V <sub>REF</sub>	
Power Dissipation	P <sub>D</sub>	Ta=85°C	Per package	855	mW
			Per output	50	
Storage Temperature	T <sub>STG</sub>	—		-50 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	Condition	Range	Unit	
Digital Power Supply Voltage	V <sub>DD</sub>	f <sub>OSC</sub> ≤32MHz	4.5 to 5.5	V	
Analog Power Supply Voltage	AV <sub>DD</sub>	V <sub>DD</sub> =AV <sub>DD</sub>	4.5 to 5.5		
Analog Reference Voltage	V <sub>REF</sub>	—	AV <sub>DD</sub> -0.3 to AV <sub>DD</sub>		
Analog Input Voltage	V <sub>AI</sub>	—	AGND to V <sub>REF</sub>		
Memory Hold Voltage	V <sub>DDH</sub>	f <sub>OSC</sub> =0Hz	2.0 to 5.5		
Operating Frequency	f <sub>OSC</sub>	V <sub>DD</sub> =5V±10%	0 to 32	MHz	
Ambient Temperature	Ta	—	-40 to +85	°C	
Fan Out	N	MOS load	20	—	
		TTL load	P0	2	—
			P1 to P11	1	—

**ELECTRICAL CHARACTERISTICS**

**DC Characteristics**

( $V_{DD}=5V\pm 10\%$ ,  $T_a=-40$  to  $+85^\circ C$ )

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
H Level Input Voltage *1	$V_{IH}$	-	2.2	-	$V_{DD}+0.3$	V
H Level Input Voltage *2, 5, 6			$0.80V_{DD}$	-	$V_{DD}+0.3$	
H Level Input Voltage *7			$0.85V_{DD}$	-	$V_{DD}+0.3$	
L Level Input Voltage *1	$V_{IL}$	-	-0.3	-	0.8	
L Level Input Voltage *2, 5, 6			-0.3	-	$0.2V_{DD}$	
L Level Input Voltage *7			-0.3	-	$0.15V_{DD}$	
H Level Output Voltage *1, 4	$V_{OH}$	$I_O=-400\mu A$	$V_{DD}-0.4$	-	-	
H Level Output Voltage *2		$I_O=-200\mu A$	$V_{DD}-0.4$	-	-	
L Level Output Voltage *1, 4	$V_{OL}$	$I_O=3.2mA$	-	-	0.4	
L Level Output Voltage *2		$I_O=1.6mA$	-	-	0.4	
Input Leakage Current *3, 6	$I_{IH}/I_{IL}$	$V_I=V_{DD}/0V$	-	-	1/-1	$\mu A$
Input Current *5			-	-	1/-250	
Input Current *7			-	-	15/-15	
H Level Output Current *1, 4	$I_{OH}$	$V_O=2.4V$	-2	-	-	mA
H Level Output Current *2			-1	-	-	
L Level Output Current *1, 4	$I_{OL}$		10	-	-	
L Level Output Current *2			5	-	-	
Output Leakage Current *1, 2, 4	$I_{LO}$	$V_O=V_{DD}/0V$	-	-	$\pm 2$	$\mu A$
Input Capacity	$C_I$	$f=1MHz, T_a=25^\circ C$	-	5	-	pF
Output Capacity	$C_O$		-	7	-	
Analog Reference Current	$I_{REF}$	A/D in operation	-	-	4	mA
		A/D stopped	-	-	10	$\mu A$
Current Consumption (in STOP mode)	$I_{DDS}$	$V_{DD}=2V, T_a=25^\circ C^*$ *8	-	0.2	10	$\mu A$
			-	1	100	
Current Consumption (in HALT mode)	$I_{DDH}$	$f_{OSC}=32MHz$ No load	-	30	60	mA
Current Consumption	$I_{DD}$		-	80	140	

\*1. Applied to P0

\*2. Applied to P1 to P11

\*3. Applied to  $A_{in}$

\*4. Applied to  $ALE, \overline{PSEN}$

\*5. Applied to  $\overline{RES}$

\*6. Applied to  $\overline{EA}, \overline{OE}, NMI$

\*7. Applied to OSC0

\*8. Ports for input pins are  $V_{DD}$  or GND, otherwise no load.

**AC Characteristics**

• **External program memory control**

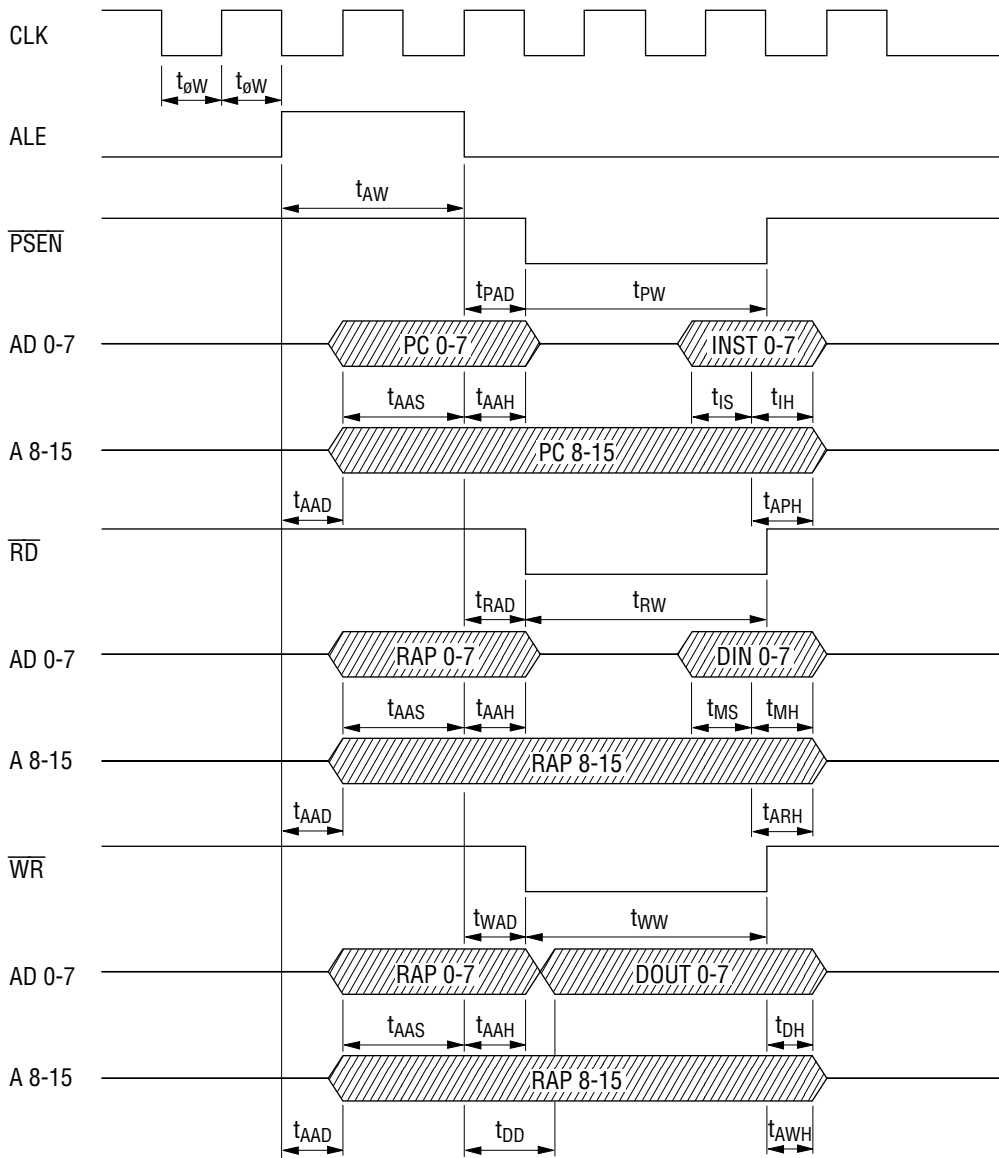
( $V_{DD}=5V\pm 10\%$ ,  $T_a=-40$  to  $+85^\circ C$ )

Parameter	Symbol	Condition	Min.	Max.	Unit
Clock Pulse Width (OSC)	$t_{\phi W}$	–	15.625	–	ns
ALE Pulse Width	$t_{AW}$	$C_L=50PF$	$3t_{\phi W}-10$	–	
$\overline{PSEN}$ Pulse Width	$t_{PW}$		$4t_{\phi W}-10$	–	
$\overline{PSEN}$ Pulse Delay Time	$t_{PAD}$		$t_{\phi W}-5$	$t_{\phi W}+5$	
Low-Order Address Setup Time	$t_{AAS}$		$2t_{\phi W}-10$	$2t_{\phi W}+10$	
Low-Order Address Hold Time	$t_{AAH}$		$t_{\phi W}-5$	$t_{\phi W}+5$	
High-Order Address Delay Time	$t_{AAD}$		$t_{\phi W}-0$	$t_{\phi W}+10$	
High-Order Address Hold Time	$t_{APH}$		$t_{\phi W}-0$	$t_{\phi W}+10$	
Instruction Setup Time	$t_{IS}$		35	–	
Instruction Hold Time	$t_{IH}$		0	$t_{\phi W}-10$	

• **External data memory control**

( $V_{DD}=5V\pm 10\%$ ,  $T_a=-40$  to  $+85^\circ C$ )

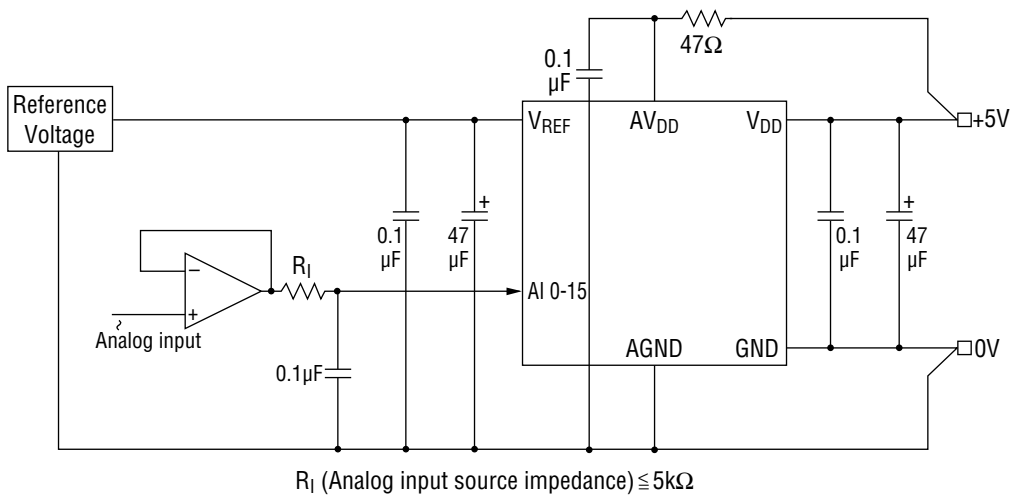
Parameter	Symbol	Condition	Min.	Max.	Unit
Clock Pulse Eidth (OSC)	$t_{\phi W}$	–	15.625	–	ns
ALE Pulse Width	$t_{AW}$	$C_L=50PF$	$3t_{\phi W}-10$	–	
$\overline{RD}$ Pulse Width	$t_{RW}$		$4t_{\phi W}-10$	–	
$\overline{WR}$ Pulse Width	$t_{WW}$		$4t_{\phi W}-10$	–	
$\overline{RD}$ Pulse Delay Time	$t_{RAD}$		$t_{\phi W}-5$	$t_{\phi W}+5$	
$\overline{WR}$ Pulse Delay Time	$t_{WAD}$		$t_{\phi W}-5$	$t_{\phi W}+5$	
Low-Order Address Setup Time	$t_{AAS}$		$2t_{\phi W}-10$	$2t_{\phi W}+10$	
Low-Order Address Hold Time	$t_{AAH}$		$t_{\phi W}-5$	$t_{\phi W}+5$	
High-Order Address Setup Time	$t_{AAD}$		$t_{\phi W}-0$	$t_{\phi W}+10$	
High-Order Address Hold Time	$t_{ARH}$		$t_{\phi W}-0$	$t_{\phi W}+10$	
High-Order Address Hold Time	$t_{AWH}$		$t_{\phi W}-0$	$t_{\phi W}+10$	
Memory Data Setup Time	$t_{MS}$		35	–	
Memory Data Hold Time	$t_{MH}$		0	$t_{\phi W}-10$	
Data Delay Time	$t_{DD}$		$t_{\phi W}-0$	$t_{\phi W}+10$	
Data Hold Time	$t_{DH}$		$t_{\phi W}-0$	$t_{\phi W}+10$	



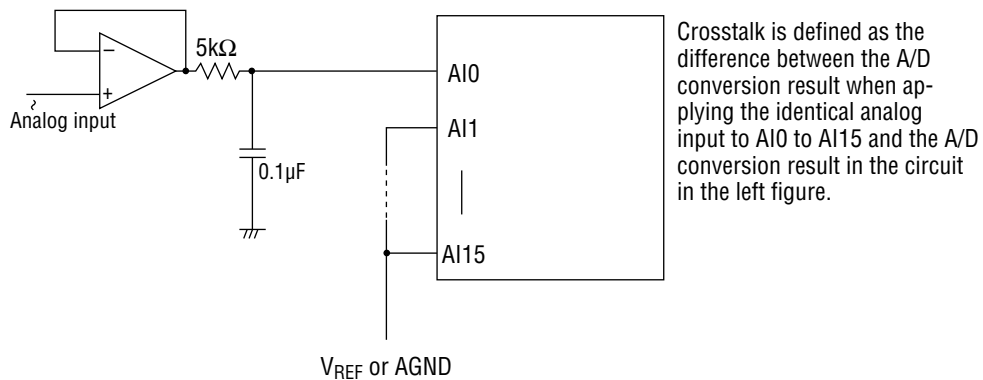
**A/D CONVERTER CHARACTERISTICS**

( $T_a = -40$  to  $+85^\circ\text{C}$ ,  $AV_{DD} = V_{DD} = V_{REF} = 5V \pm 10\%$ ,  $AGND = GND = 0V$ ,  $f_{OSC} = 32\text{MHz}$ )

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	Refer to the recommended circuit. (Figure 1) Analog input source impedance $R_I \leq 5k\Omega$ $t_{CONV} = 16\mu\text{sec}$	-	-	10	Bit
Linearity Error	$E_L$		-	-	$\pm 3$	
Differential Linearity Error	$E_D$		-	-	$\pm 1$	
Zero Scale Error	$E_{ZS}$		0	-	+3	
Full Scale Error	$E_{FS}$		-	-	-3	
Crosstalk	$E_{CT}$	Refer to the measuring circuit. (Figure 2)	-	-	$\pm 1$	LSB
Conversion Time	$t_{CONV}$	by ADTM set data	8	-	24	$\mu\text{s/CH}$



**Figure 1 Recommended Circuit**



**Figure 2 Crosstalk Measuring Circuit**

## Definitions of Terms

### Resolution

The minimum distinguishable analog value. For 10 bits,  $2^{10}=1024$ , i.e.  $(V_{REF}-AGND) \div 1024$ .

### Linearity error

The variance between the ideal conversion characteristics as a 10-bit A/D converter and the actual conversion characteristics. (Quantized error is therefore not included.)

In the ideal conversion, a voltage between  $V_{REF}$  and AGND is divided into 1,024 equal steps.

### Differential linearity error

The smoothness of the conversion. The width of analog input voltage corresponding to the change by one bit of digital output is 1 LSB= $(V_{REF}-AGND) \div 1024$  ideally. The variance between this ideal bit size and bit size at arbitrary point in the conversion range.

### Zero scale error

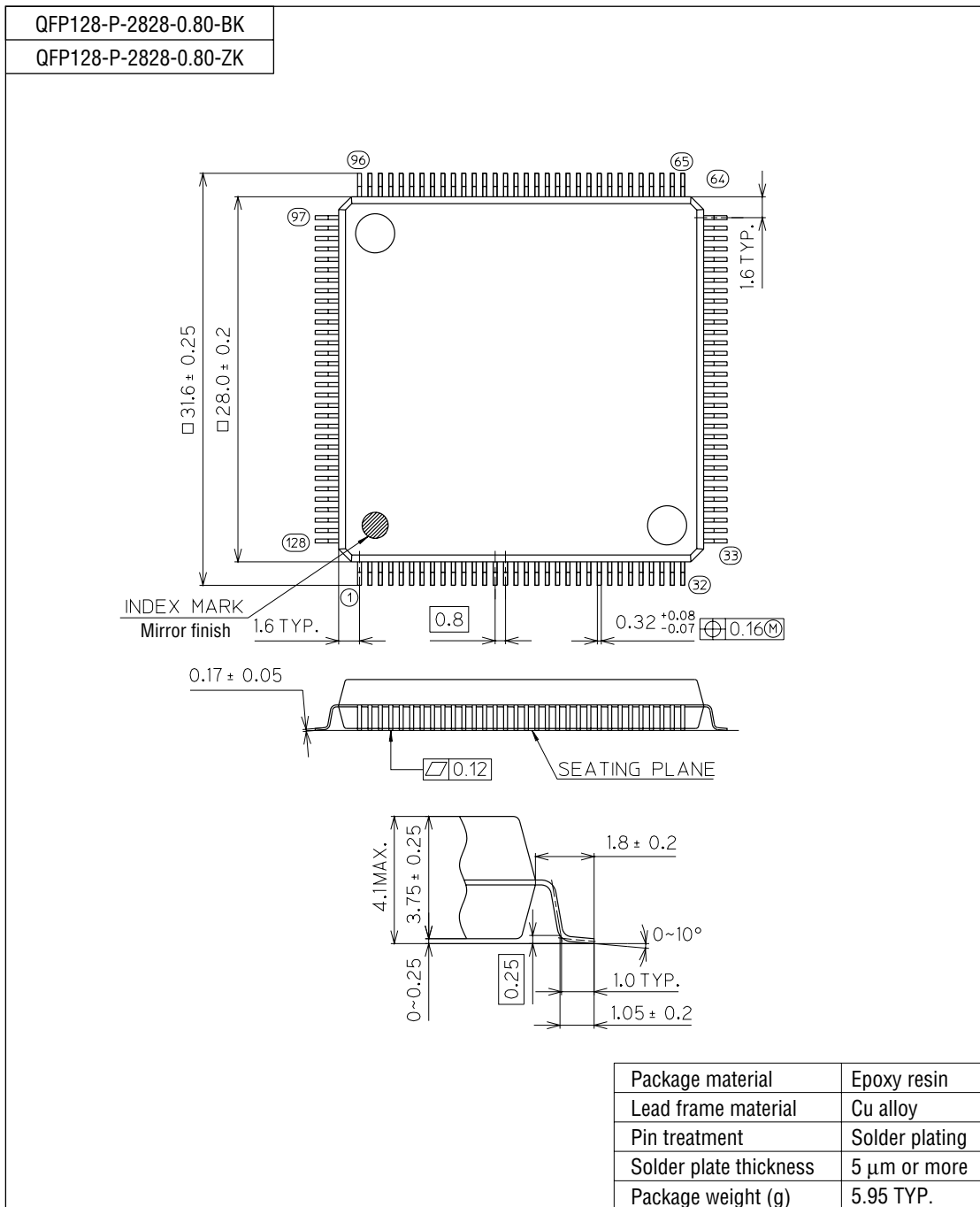
The variance between the ideal conversion characteristics at the switching point of digital output "000H to 001H" and actual conversion characteristics.

### Full scale error

The variance between the ideal conversion characteristics at the switching point of digital output "3FEH to 3FFH" and actual conversion characteristics.

PACKAGE DIMENSIONS

(Unit : mm)



Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).