SRAM

64K x 4 SRAM

5V ASYNCHRONOUS SRAM

FEATURES
- High speed: 10, 12, 15, 20 and 25
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with $\overline{CE}$ option
- All inputs and outputs are TTL-compatible

OPTIONS   MARKING
- Timing
  - 10ns access   -10
  - 12ns access   -12
  - 15ns access   -15
  - 20ns access   -20
  - 25ns access   -25

- Packages
  - Plastic DIP (300 mil)   None
  - Plastic SOJ (300 mil)   DJ

- 2V data retention (optional)   L
- Low power (optional)   P

- Temperature
  - Commercial (0°C to +70°C)   None
  - Industrial   (-40°C to +85°C)   IT
  - Automotive (-40°C to +125°C)   AT
  - Extended   (-55°C to +125°C)   XT

- Part Number Example: MT5C2564DJ-15 L

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

PIN ASSIGNMENT (Top View)

24-Pin DIP
(SA-3)

A0	1	24	Vcc
A1	2	23	A15
A2	3	22	A14
A3	4	21	A13
A4	5	20	A12
A5	6	19	A11
A6	7	18	A10
A7	8	17	DQ4
A8	9	16	DQ3
A9	10	15	DQ2
$\overline{CE}$	11	14	DQ1
Vss	12	13	$\overline{WE}$

24-Pin SOJ
(SD-1)

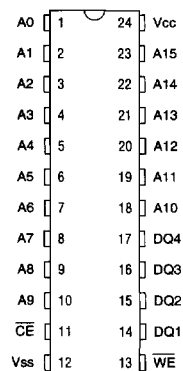|			
A0	1	24	Vcc
A1	2	23	A15
A2	3	22	A14
A3	4	21	A13
A4	5	20	A12
A5	6	19	A11
A6	7	18	A10
A7	8	17	DQ4
A8	9	16	DQ3
A9	10	15	DQ2
$\overline{CE}$	11	14	DQ1
Vss	12	13	$\overline{WE}$

GENERAL DESCRIPTION

The MT5C2564 is organized as a 65,536 x 4 SRAM using a four-transistor memory cell with a high-speed, low-power CMOS process. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) with all organizations. This enhancement can place the outputs in High-Z for additional flexibility in system design.
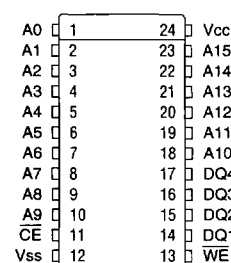
Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ goes LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "P" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$ and address lines, which also facilitates the design of battery backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL-compatible.

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FUNCTIONAL BLOCK DIAGRAM
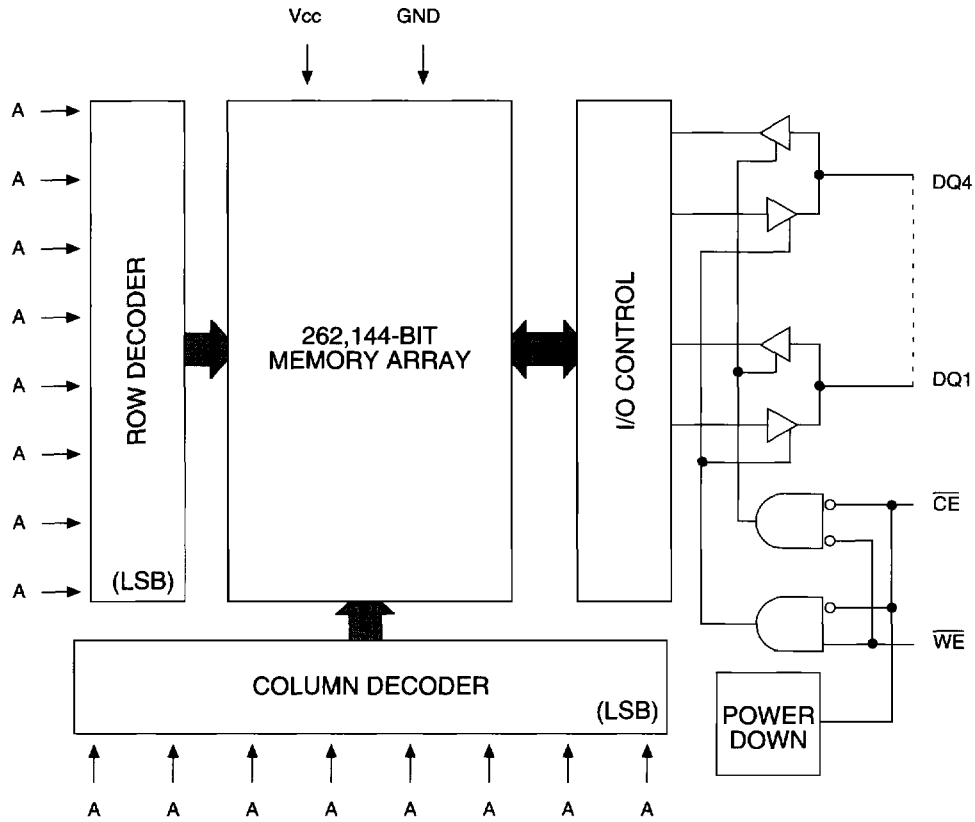
TRUTH TABLE

MODE	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	D	ACTIVE

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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss .... -1V to +7V
Storage Temperature (plastic) .... -55°C to +150°C
Short Circuit Output Current 50mA
Voltage on Any Pin Relative to Vss .... -1V to Vcc +1V
Junction Temperature** .... +150°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
**Maximum junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See technical note TN-05-14 for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS
(0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ Vcc	I_{LI}	-5	5	μA	
Output Leakage Current	Output(s) disabled 0V ≤ V_{OUT} ≤ Vcc	I_{LO}	-5	5	μA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		Vcc	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX					UNITS	NOTES
				-10†	-12†	-15	-20	-25		
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; Vcc = MAX f = MAX = 1/ ^{t}RC outputs open	Icc	130	200	180	165	150	140	mA	3, 13
	P version	Icc	100	-	-	140	125	120	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; Vcc = MAX f = MAX = 1/ ^{t}RC outputs open	I_{SB1}	24	55	50	45	40	35	mA	13
	P version	I_{SB1}	1.4	-	-	4	4	4	mA	13
	$\overline{CE}$ ≥ Vcc -0.2V; Vcc = MAX V_{IN} ≤ Vss +0.2V or V_{IN} ≥ Vcc -0.2V; f = 0	I_{SB2}	0.6	5	5	5	5	7	mA	13
	P version	I_{SB2}	0.4	-	-	3	3	3	mA	13

†P version not available with this speed.

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CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	$T_A = 25°C; f = 1$ MHz	C_I	6	pF	4
Output Capacitance	$Vcc = 5V$	C_O	6	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = 5V ±10%)

DESCRIPTION	SYM	-10 MIN	-10 MAX	-12 MIN	-12 MAX	-15 MIN	-15 MAX	-20 MIN	-20 MAX	-25 MIN	-25 MAX	UNITS	NOTES
READ Cycle													
READ cycle time	t_{RC}	10		12		15		20		25		ns	
Address access time	t_{AA}		10		12		15		20		25	ns	
Chip Enable access time	t_{ACE}		10		12		15		20		25	ns	
Output hold from address change	t_{OH}	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	t_{LZCE}	3		3		3		3		3		ns	7
Chip disable to output in High-Z	t_{HZCE}		5		6		8		9		9	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		0		ns	4
Chip disable to power-down time	t_{PD}		10		12		15		20		25	ns	4
WRITE Cycle													
WRITE cycle time	t_{WC}	10		12		15		20		25		ns	
Chip Enable to end of write	t_{CW}	7		8		10		12		15		ns	
Chip Enable to end of write (P and LP version)	t_{CW}	-		-		12		12		15		ns	
Address valid to end of write	t_{AW}	7		8		10		12		15		ns	
Address valid to end of write (P and LP version)	t_{AW}	-		-		12		12		15		ns	
Address setup time	t_{AS}	0		0		0		0		0		ns	
Address hold from end of write	t_{AH}	1		1		1		1		1		ns	
WRITE pulse width	t_{WP1}	7		8		10		12		15		ns	
WRITE pulse width	t_{WP2}	10		12		12		15		15		ns	
Data setup time	t_{DS}	6		7		7		10		10		ns	
Data hold time	t_{DH}	0		0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	2		2		2		2		2		ns	7
Write Enable to output in High-Z	t_{HZWE}		5		6		7		8		10	ns	6, 7

INDUSTRIAL TEMPERATURE SPECIFICATIONS (IT)

The following specifications are to be used for Industrial Temperature (IT) MT5C2564 SRAMs.
(-40°C ≤ T$_A$ ≤ 85°C)

DESCRIPTION	CONDITIONS	SYMBOL	MAX -10	-12	-15	-20	-25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V$_{IL}$; V$_{CC}$ = MAX f = MAX = 1/ ^{t}RC outputs open	I$_{CC}$	210	190	170	160	150	mA	3
Power Supply Current: Standby	$\overline{CE}$ ≥ V$_{IH}$; V$_{CC}$ = MAX f = MAX = 1/ ^{t}RC outputs open	I$_{SB1}$	65	60	50	45	40	mA	
	$\overline{CE}$ ≥ V$_{CC}$ -0.2V; V$_{CC}$ = MAX V$_{IN}$ ≤ V$_{SS}$ +0.2V or V$_{IN}$ ≥ V$_{CC}$ -0.2V; f = 0	I$_{SB2}$	6	6	6	6	6	mA	

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MAX	UNITS	NOTES
Data Retention Current	$\overline{CE}$ ≥ (V$_{CC}$ -0.2V) V$_{IN}$ ≥ (V$_{CC}$ -0.2V) or ≤ 0.2V	V$_{CC}$ = 2V	I$_{CCDR}$	400	μA	
		V$_{CC}$ = 3V	I$_{CCDR}$	600	μA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T$_A$ ≤ 85°C)

DESCRIPTION	SYM	-12 MIN	MAX	-15 MIN	MAX	-20 MIN	MAX	-25 MIN	MAX	UNITS	NOTES
READ Cycle											
Output hold from address change	^{t}OH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^{t}LZCE	2		2		2		2		ns	7
WRITE Cycle											
Address hold from end of write	^{t}AH	2		2		2		2		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T$_A$ ≤ 85°C)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V$_{IH}$	2.3	V$_{CC}$ +1	V	1

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AUTOMOTIVE AND EXTENDED TEMPERATURE SPECIFICATIONS (AT AND XT)

The following specifications are to be used for Automotive Temperature (AT) and Extended Temperature (XT) MT5C2564 SRAMs. (-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

DESCRIPTION	CONDITIONS	SYMBOL	MAX -12	MAX -15	MAX -20	MAX -25	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX f = MAX = 1/ ^{t}RC outputs open	I_{CC}	195	175	165	155	mA	3, 13
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX f = MAX = 1/ ^{t}RC outputs open	I_{SB1}	60	50	45	40	mA	13
	$\overline{CE}$ ≥ V_{CC} -0.2V; V_{CC} = MAX V_{IN} ≤ V_{SS} +0.2V or V_{IN} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	7	7	7	7	mA	13

DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MAX	UNITS	NOTES
Data Retention Current	$\overline{CE}$ ≥ (V_{CC} -0.2V) V_{IN} ≥ (V_{CC} -0.2V) or ≤ 0.2V	V_{CC} = 2V	I_{CCDR}	500	µA	
		V_{CC} = 3V	I_{CCDR}	800	µA	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

Refer to commercial temperature timing parameters for specifications not listed here.
(Notes 5, 13) (-40°C ≤ T_A ≤ 125°C - AT; -55°C ≤ T_A ≤ 125°C - XT; V_{CC} = 5V ±10%)

DESCRIPTION	SYM	-12 MIN	-12 MAX	-15 MIN	-15 MAX	-20 MIN	-20 MAX	-25 MIN	-25 MAX	UNITS	NOTES
READ Cycle											
Output hold from address change	^{t}OH	2		2		2		2		ns	
Chip Enable to output in Low-Z	^{t}LZCE	2		2		2		2		ns	7
WRITE Cycle											
Address hold from end of write	^{t}AH	2		2		2		2		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-40°C ≤ T_A ≤ 125°C - AT) (-55°C ≤ T_A ≤ 125°C - XT)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.3	V_{CC} +1	V	1

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AC TEST CONDITIONS

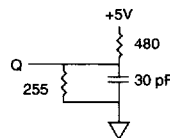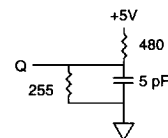|	
Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

Fig. 1 OUTPUT LOAD EQUIVALENT

Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < $^tRC/2$.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^tHZCE and ^tHZWE are specified with $C_L = 5pF$ as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE, and ^tHZWE is less than ^tLZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^tRC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Typical values are measured at 5V, 25°C and 15ns cycle time.
14. Typical currents are measured at 25°C.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP versions only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			VDR	2			V	
Data Retention Current L version	$\overline{CE} \geq (Vcc -0.2V)$ VIN $\geq$ (Vcc -0.2V) or $\leq 0.2V$	Vcc = 2V	ICCDR		125	300	µA	14
		Vcc = 3V	ICCDR		175	500	µA	14
Data Retention Current LP version	$\overline{CE} \geq (Vcc -0.2V)$	Vcc = 2V	ICCDR		100	300	µA	14
		Vcc = 3V	ICCDR		150	500	µA	14
Chip Deselect to Data Retention Time			^tCDR	0			ns	4
Operation Recovery Time			^tR	^tRC			ns	4, 10

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LOW Vcc DATA RETENTION WAVEFORM
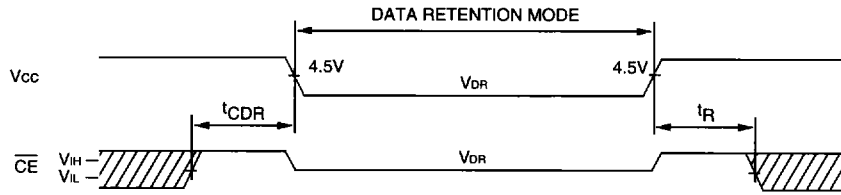
READ CYCLE NO. 1 [8, 9]
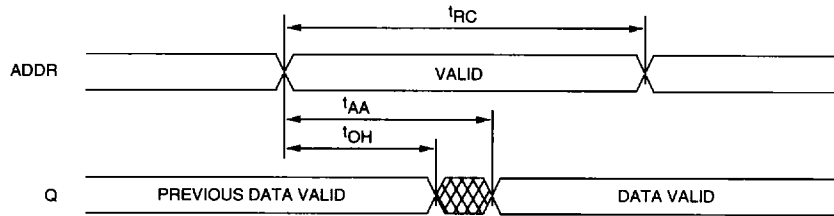
READ CYCLE NO. 2 [7, 8, 10]

//// DON'T CARE

▨ UNDEFINED
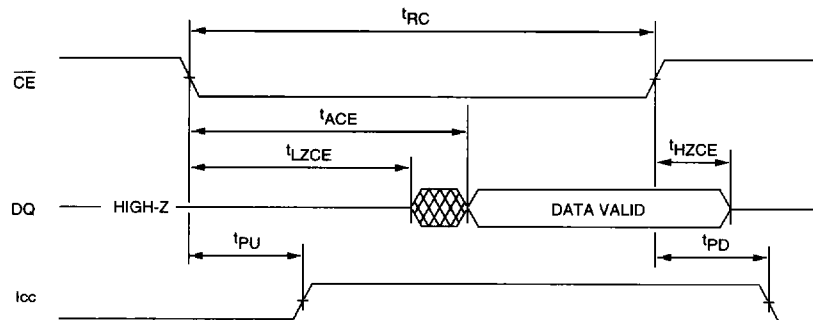
WRITE CYCLE NO. 1
(Chip Enable Controlled)
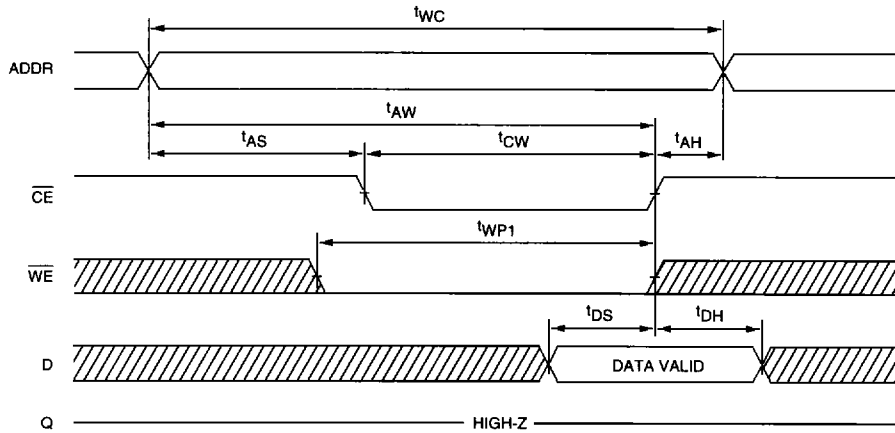
WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)

▨ DON'T CARE

▩ UNDEFINED