Features

- JEDEC Standard 144-pin PC133 SDRAM SODIMM
- Fast 5.4 ns Clock Access Time
- Supports CAS Latency = 2, 3
- On-board Serial Presence Detect (SPD)
- Unbuffered 144-pin SODIMM
- 4K Refresh / 64ms (8K Refresh for 512MB DIMM)
- Single 3.3V ± 0.3V Power Supply

Description

The Enhanced Memory Systems 64MB, 128MB, 256MB, and 512MB Small Outline DIMMs (1.05-inch height) are the fastest SODIMMs available for notebook and embedded system applications. This PC133 product provides the lowest cost for both PC133 and PC100 sockets. The fast 5.4 ns clock access time allows unbuffered operation at 133 MHz for lower memory latency, and lower costs than registered DIMMs.

The 64MB module is organized as 8Mx64, the 128MB module is organized as 16Mx64, the 256MB module is organized as 32Mx64, and the 512MB module is organized as 64Mx64. Each module has a serial presence EEPROM, which contains information on the module type, module organization, component speed, and other attributes relevant to the system controller.

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	Vss	37	DQ8	73	RSVD	109	Vss
2	Vss	38	DQ40	74	CK1	110	A9
3	DQ0	39	DQ9	75	Vss	111	A10/AP
4	DQ32	40	DQ41	76	Vss	112	NC
5	DQ1	41	DQ10	77	RSVD	113	Vdd
6	DQ33	42	DQ42	78	RSVD	114	Vdd
7	DQ2	43	DQ11	79	RSVD	115	DQMB2
8	DQ34	44	DQ43	80	RSVD	116	DQMB6
9	DQ3	45	Vdd	81	Vdd	117	DQMB3
10	DQ35	46	Vdd	82	Vdd	118	DQMB7
11	Vdd	47	DQ12	83	DQ16	119	Vss
12	Vdd	48	DQ44	84	DQ48	120	Vss
13	DQ4	49	DQ13	85	DQ17	121	DQ24
14	DQ36	50	DQ45	86	DQ49	122	DQ56
15	DQ5	51	DQ14	87	DQ18	123	DQ25
16	DQ37	52	DQ46	88	DQ50	124	DQ57
17	DQ6	53	DQ15	89	DQ19	125	DQ26
18	DQ38	54	DQ47	90	DQ51	126	DQ58
19	DQ7	55	Vss	91	Vss	127	DQ27
20	DQ39	56	Vss	92	Vss	128	DQ59
21	Vss	57	NC	93	DQ20	129	Vdd
22	Vss	58	RSVD	94	DQ52	130	Vdd
23	DQMB0	59	NC	95	DQ21	131	DQ28
24	DQMB4	60	RSVD	96	DQ53	132	DQ60
25	DQMB1	61	CK0	97	DQ22	133	DQ29
26	DQMB5	62	CKE0	98	DQ54	134	DQ61
27	Vdd	63	Vdd	99	DQ23	135	DQ30
28	Vdd	64	Vdd	100	DQ55	136	DQ62
29	A0	65	RAS#	101	Vdd	137	DQ31
30	A3	66	CAS#	102	Vdd	138	DQ63
31	A1	67	WE#	103	A6	139	Vss
32	A4	68	CKE1	104	A7	140	Vss
33	A2	69	S0#	105	A8	141	SDA
34	A5	70	A12	106	BA0	142	SCL
35	Vss	71	S1#	107	Vss	143	Vdd
36	Vss	72	NC	108	Vss	144	Vdd

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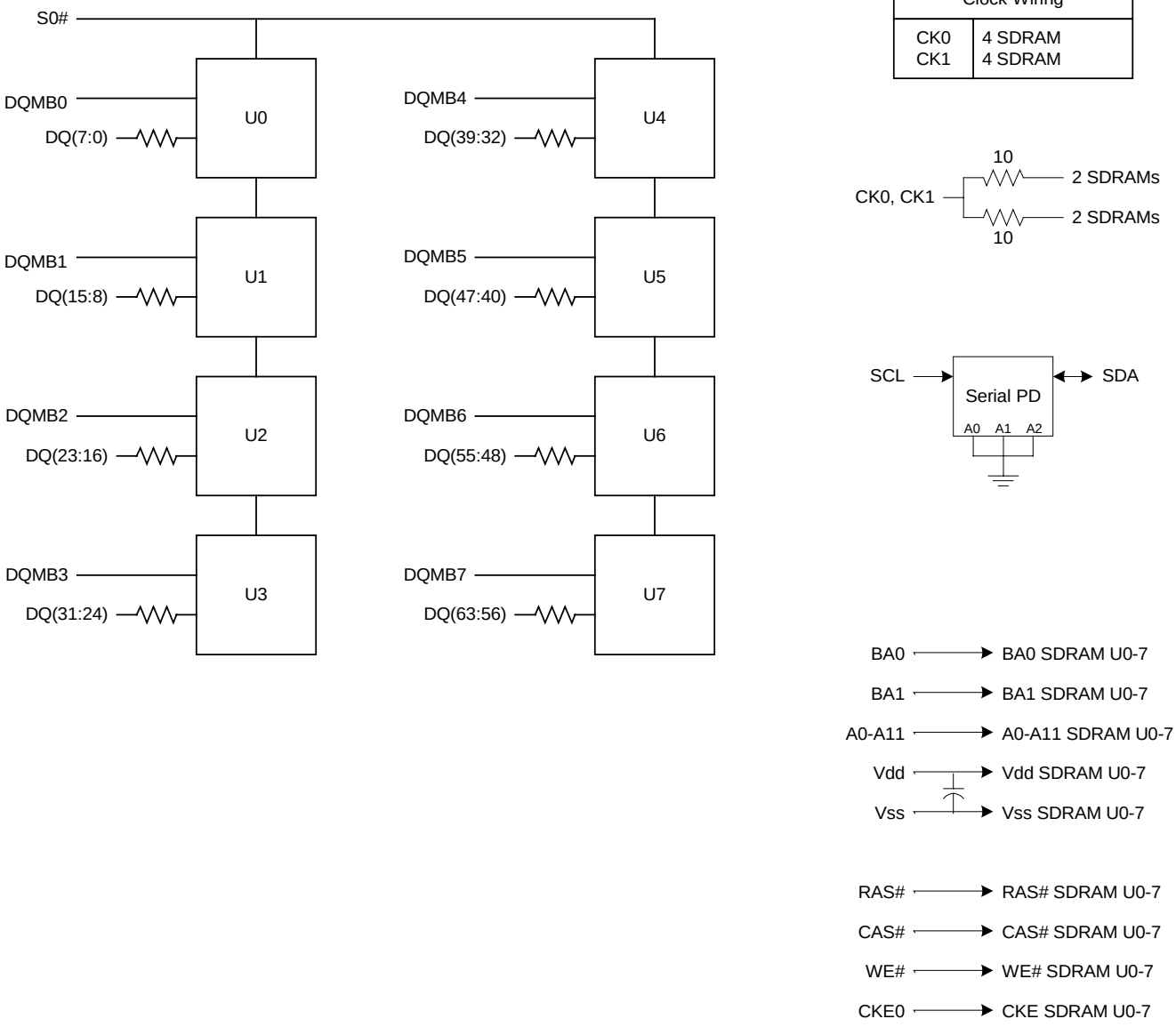
Pin Descriptions

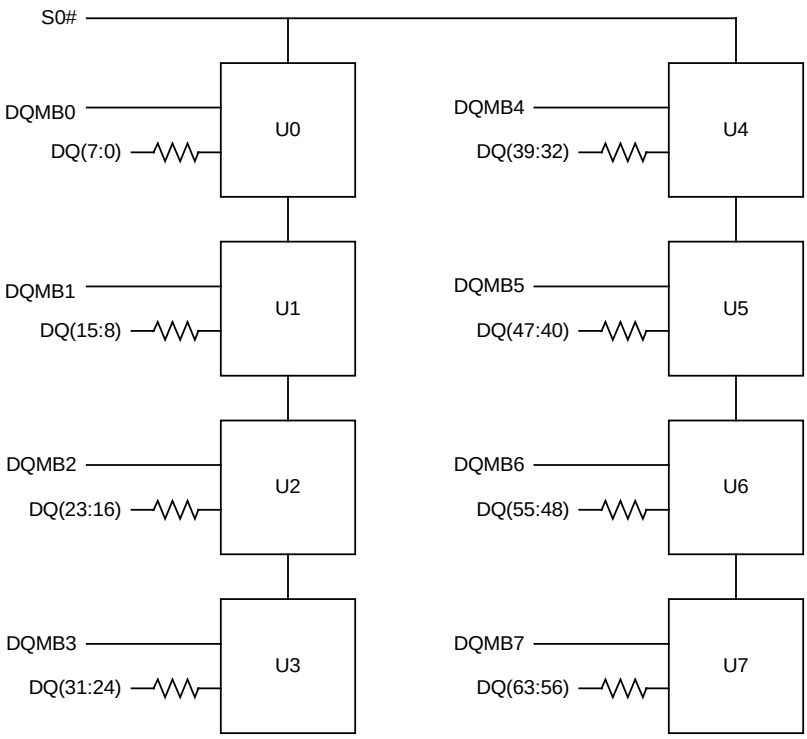
Symbol	Type	Function
CK(0:1)	Input	Clocks: All SDRAM input signals are sampled on the positive edge of CK.
CKE(0:1)	Input	Clock Enables: CKE activate (high) or deactivate (low) the CK signals. Deactivating the clock initiates the Power-Down and Self-Refresh operations (all banks idle), or Clock Suspend operation. CKE is synchronous until the device enters Power-Down and Self-Refresh modes where it is asynchronous until the mode is exited.
S(0:1)#	Input	Chip Select: S# enables (low) or disables (high) the command decoder. When the command decoder is disabled, new commands are ignored but previous operations continue.
RAS#, CAS#, WE#	Input	Command Inputs: Sampled on the rising edge of CK, these inputs define the command to be executed.
BA(0:1)	Input	Bank Addresses: These inputs define to which of the 4 banks a given command is being applied.
A(0:12)	Input	Address Inputs: A0-A12 define the row address during the Bank Activate command. A0-A9 define the column address during Read and Write commands. A10/AP invokes the Auto-precharge operation. During manual Precharge commands, A10/AP low specifies a single bank precharge while A10/AP high precharges all banks. The address inputs are also used to program the Mode Register.
DQ(0:63)	Input/ Output	Data I/O: Data bus inputs and outputs. For Write cycles, input data is applied to these pins and must be set-up and held relative to the rising edge of clock. For Read cycles, the device drives output data on these pins after the CAS latency is satisfied.
DQMB(0-7)	Input	Data I/O Mask Inputs: DQMB0-7 inputs mask write data (zero latency) and acts as a synchronous output enable (2-cycle latency) for read data.
V_{DD}	Supply	Power Supply: +3.3 V
V_{SS}	Supply	Ground
SDA	Input/ Output	Serial Presence-Detect Data: SDA is a bi-directional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence detect data transfer to and from the module
RFU	-	Reserved for Future Use: These pins should be left unconnected.
DNU	-	Do not use.
NC	-	No connect - open pin.

64MB DIMM Functional Block Diagram – SM6408SDT

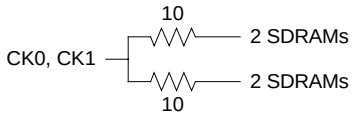


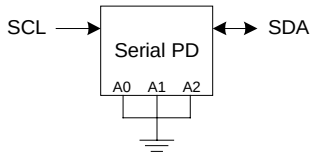
Note:
All DQ resistor values are 10 ohms.
All CK resistor values are 10 ohms.
U0-U7 are 8Mx8 PC133 SDRAM devices.

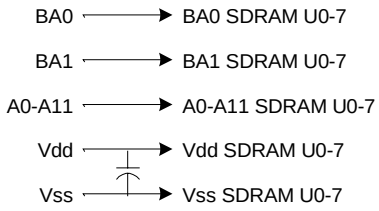
128MB DIMM Functional Block Diagram – SM12808ASDT

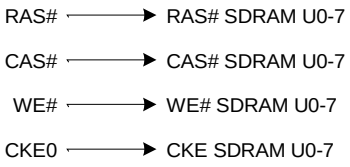


Clock Wiring	
CK0	4 SDRAM
CK1	4 SDRAM



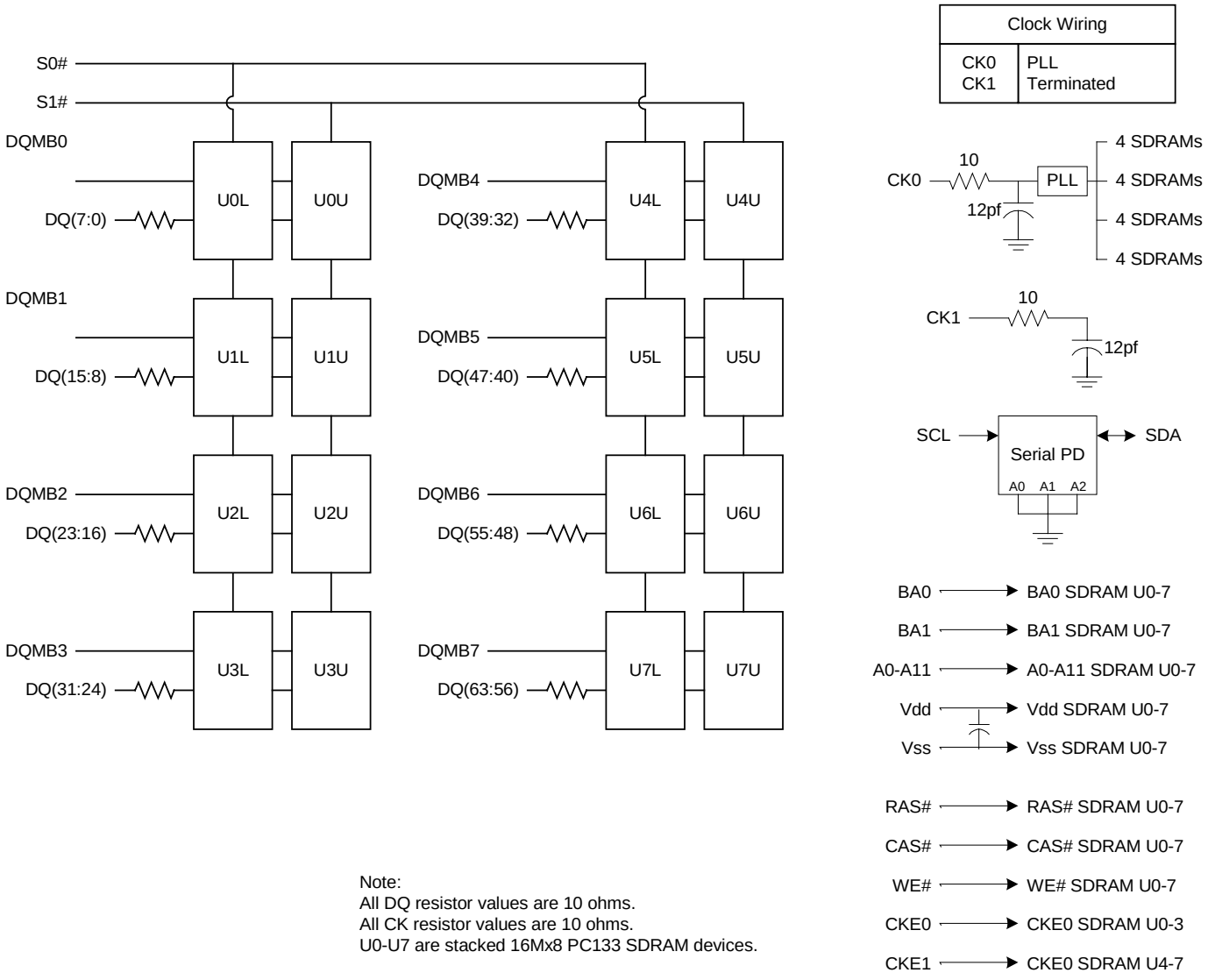






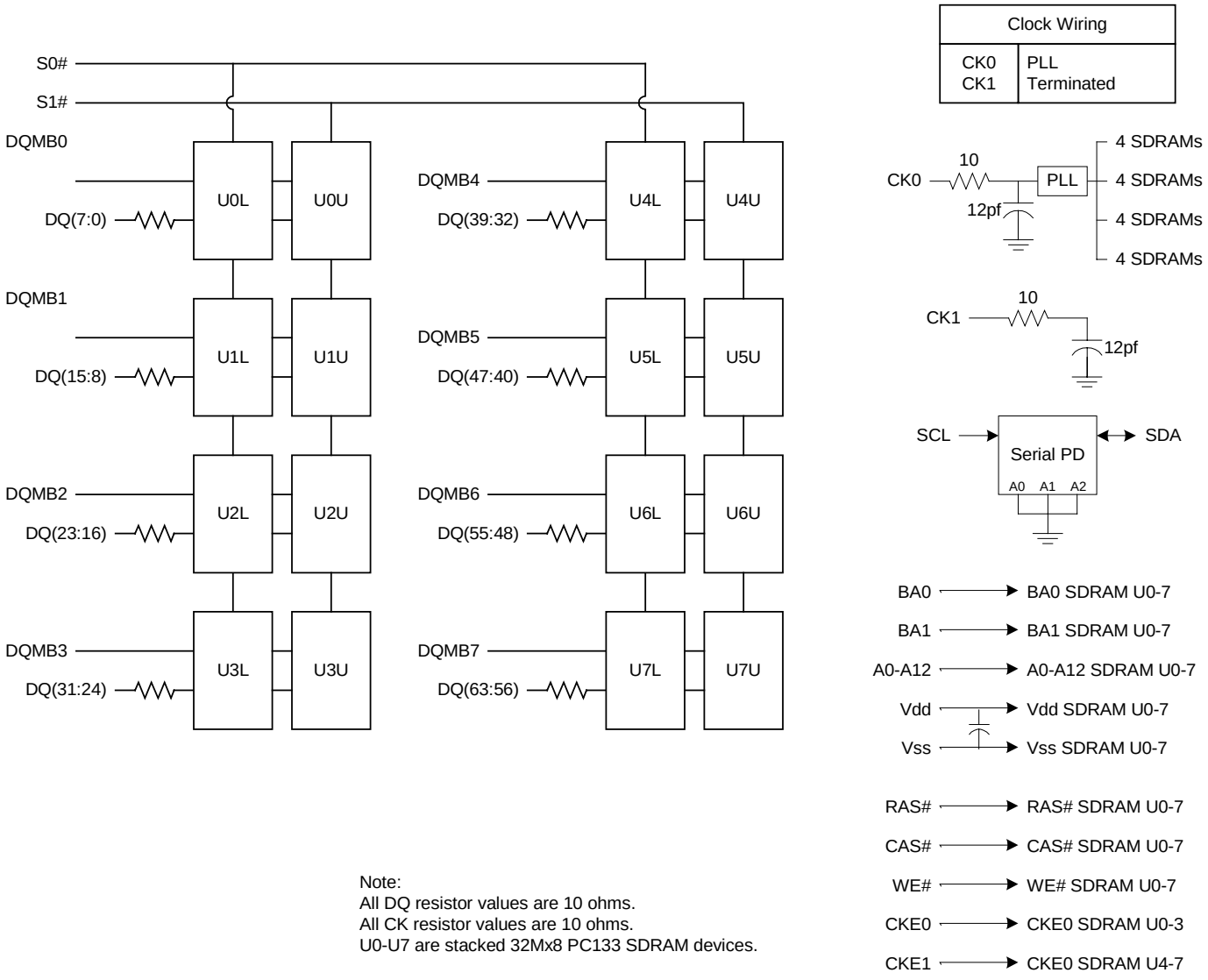
Note:
All DQ resistor values are 10 ohms.
All CK resistor values are 10 ohms.
U0-U7 are 16Mx8 PC133 SDRAM devices.

256MB DIMM Functional Block Diagram – SM25608ASDT



Note:
All DQ resistor values are 10 ohms.
All CK resistor values are 10 ohms.
U0-U7 are stacked 16Mx8 PC133 SDRAM devices.

512MB DIMM Functional Block Diagram – SM51208BSDT



Note:
All DQ resistor values are 10 ohms.
All CK resistor values are 10 ohms.
U0-U7 are stacked 32Mx8 PC133 SDRAM devices.

Electrical Characteristics

Absolute Maximum Ratings

Description	Symbol	Value
Power Supply Voltage	V_{DD}	-1V to +4.6V
Voltage on any Pin with Respect to Ground	V_{IN}, V_{OUT}	-0.5V to +4.6V
Operating Temperature (ambient)	T_A	0°C to +70°C
Storage Temperature	T_{stg}	-55°C to +125°C
Power Dissipation	P_D	TBD
DC Output Current (I/O pins)	I_{OUT}	50mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these, or any other conditions above those listed in the operational section of the specification, is not implied. Exposure to conditions at absolute maximum ratings for extended periods may affect device reliability.

DC Operating Conditions (T_A = 0°C to 70°C)

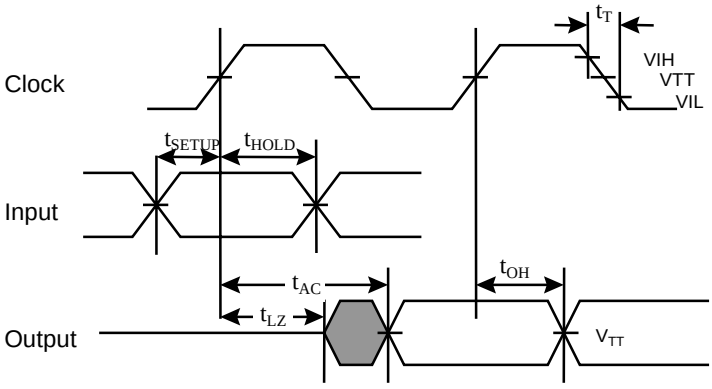
Symbol	Parameter	Min	Typical	Max	Units	Notes
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	
V_{IH}	Input High Voltage	2.0	3.3	V_{DD} + 0.3	V	
V_{IL}	Input Low Voltage	-0.3	0.0	0.8	V	
$I_{I(L)}$	Input Leakage Current	-	-	±1	µA	
$I_{O(L)}$	Output Leakage Current	-	-	±1	µA	
V_{OH}	Output High Voltage (I_{OUT} = -4mA)	2.4	-	V_{DD}	V	
V_{OL}	Output Low Voltage (I_{OUT} = +4mA)	0.0	-	0.4	V	

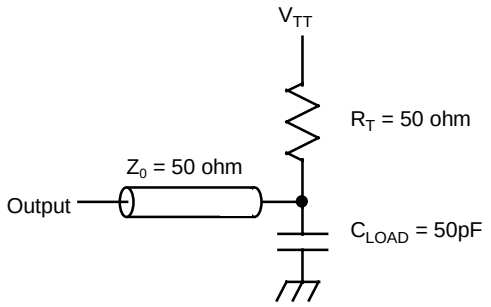
Capacitance (T_A = 25°C, f = 1MHz, VDD = 3.3V ±0.3V, not 100% tested)

Symbol	Parameter	64MB	128MB	256MB	512MB	Units
C_{In1}	Input Capacitance (BA1, BA0, A0-12, RAS, CAS,WE)	36	36	55	55	pF
C_{In2}	Input Capacitance (S0, S1)	20	20	32	32	pF
C_{In3}	Input Capacitance (CK0, CK1)	20	20	6	6	pF
C_{In4}	Input Capacitance (CKE0, CKE1)	32	32	32	32	pF
C_{In5}	Input Capacitance (DQMB0-7)	7	7	10	10	pF
C_{In6}	Input Capacitance (SCL)	10	10	10	10	pF
$C_{I/O1}$	I/O Capacitance (SDA)	10	10	10	10	pF
$C_{I/O2}$	I/O Capacitance (DQ0 - DQ63)	10	10	14	14	pF

AC Characteristics (T_A = 0°C to 70°C)

1. An initial pause of 200µs is required after power-up, then a Precharge All Banks command must be given followed by a minimum of eight Auto (CBR) Refresh cycles before the Mode Register Set operation can begin.
2. AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0V with the timing referenced to the V_{TT} = 1.4V crossover point.





AC Output Load Circuit

3. The transition time is measured between V_{IH} and V_{IL} (or between V_{IH} and V_{IL}).
4. AC measurements assume t_T = 1ns.
5. In addition to meeting the transition rate specification, the clock and CKE must transition V_{IH} and V_{IL} (or between V_{IH} and V_{IL}) in a monotonic manner.

AC Operating Conditions (T_A = 0°C to 70°C)

Clock and Clock Enable Parameters

Symbol	Parameter	-7.5		Units	Notes
		Min	Max		
t_{CK2}	Clock Cycle Time, CL = 2	10	-	ns	
t_{CK3}	Clock Cycle Time, CL = 3	7.5	-	ns	
t_{CKH2}, t_{CKL2}	Clock High & Low Times, CL=2	2.5	-	ns	1
t_{CKH3}, t_{CKL3}	Clock High & Low Times, CL=1	2.5	-	ns	1
t_{CKES}	Clock Enable Set-Up Time	1.5	-	ns	
t_{CKEH}	Clock Enable Hold Time	0.8	-	ns	
t_{CKSP}	CKE Set-Up Time (Power down mode)	1.5	-	ns	
t_T	Transition Time (Rise and Fall)	0.3	1.2	ns	

Notes:

1. Assumes clock rise and fall times are equal to 1ns. If rise or fall time exceeds 1ns, other AC timing parameters must be compensated by an additional $[(t_{rise}+t_{fall})/2\text{-}1]$ ns.

Common Parameters

Symbol	Parameter	-7.5		Units	Notes
		Min	Max		
t_{CS}	Command and Address Set-Up Time	1.5	-	ns	
t_{CH}	Command and Address Hold Time	0.8	-	ns	
t_{RCD}	RAS to CAS Delay Time	20	-	ns	
t_{RC}	Bank Cycle Time	67	-	ns	
t_{RAS}	Bank Active Time	45	100K	ns	
t_{RP}	Precharge Time	20	-	ns	
t_{RRD}	Bank to Bank Delay Time (Alt. Bank)	15	-	ns	
t_{CCD}	CAS to CAS Delay Time (Same Bank)	7.5	-	ns	
t_{MRD}	Mode Register Set to Active Delay	2	-	CLK	

Read and Write Parameters

Symbol	Parameter	-7.5		Units	Notes
		Min	Max		
t_{AC3}	Clock Access Time, CL = 3	-	5.4	ns	1,2
t_{AC2}	Clock Access Time, CL = 2	-	6.0	ns	1,2
t_{OH3}	Data Output Hold Time (CL=3)	3.0	-	ns	
t_{OH2}	Data Output Hold Time (CL=2)	3.0	-	ns	
t_{LZ}	Data Output to Low-Z Time	1	-	ns	
t_{HZ2}	Data Output to High-Z Time (CL=2, 3)	3	7	ns	3
t_{DQZ}	DQM Data Output Disable Time	2	-	CLK	
t_{DS}	Data Input Set-Up Time	1.5	-	ns	
t_{DH}	Data Input Hold Time	0.8	-	ns	
t_{DPL}	Data Input to Precharge	15	-	ns	
t_{DAL}	Data Input to ACTV/Refresh	35	-	ns	4
t_{DQW}	Data Write Mask Latency	0	-	CLK	

Notes:

1. Access time is measured at 1.4V (LVTTL) at max clock rate for the CAS latency specified. See AC Test Load.
2. Access time is based on a clock rise time of 1ns. If clock rise time is longer than 1ns, then (trise/2-0.5) ns must be added to the access time.
3. Referenced to the time at which the output achieves an open circuit condition.
4. tDAL is equal to tDPL + tRP.

Refresh Parameters

Symbol	Parameter	-6		-7.5		Units	Notes
		Min	Max	Min	Max		
t_{REF}	Refresh Period	-	64	-	64	ms	1,2
t_{SREX}	Self Refresh Exit Time	$2CLK+t_{RC}$		$2CLK+t_{RC}$	-	ns	3

Notes:

1. 4096 cycles (64, 128, and 256MB DIMMs), 8192 cycles (512MB DIMMs).
2. Any time that the refresh period has been exceeded, a minimum of two Auto-Refresh (CBR) commands must be given to “wake up” the device.
3. Self-Refresh exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self-Refresh Exit is not completed until tRC is satisfied once the Self-Refresh Exit command is registered.

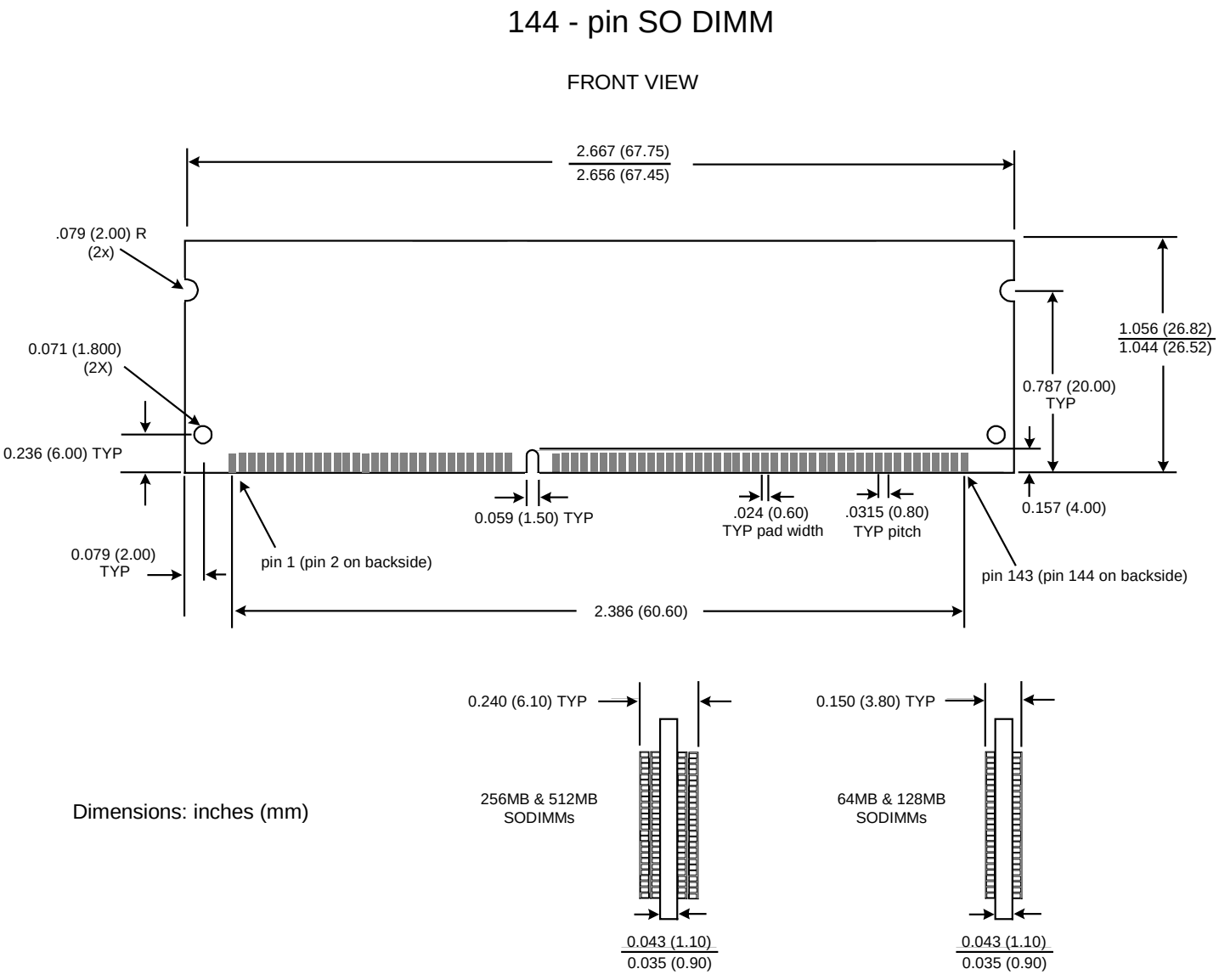
Serial Presence Detect (SPD) for SDRAM SODIMMs

		64MB	128MB	64MB	128MB
Byte	Description			** Hex Code **	
0	Number of bytes written into EEPROM	128	128	80	80
1	Total number of SPD bytes	256	256	08	08
2	Memory Type	SDRAM	SDRAM	04	04
3	Number of Row Addresses	12	12	0C	0C
4	Number of Column Addresses	9	10	09	0A
5	Number of Module Banks	1	1	01	01
6	Module Data Width	x64	x64	40	40
7	Module Data Width (cont'd)	0	0	00	00
8	Voltage Interface Levels	LVTTL	LVTTL	01	01
9	Cycle Time at max CAS Latency	7.5 ns	7.5 ns	75	75
10	SDRAM Clock Access Time	5.4 ns	5.4 ns	54	54
11	DIMM config (non-parity, parity, ECC)	--- Non-parity ---		00	00
12	Refresh Rate and Type	--- 15.625us / Self ---		80	80
13	Primary SDRAM Width	x8	x8	08	08
14	Error Checking Data Width	N/A	N/A	00	00
15	Min. CAS-to-CAS Delay (tCCD)	1 clk	1 clk	01	01
16	Burst Lengths Supported	--- 1,2,4,8,Full Pg ---		8F	8F
17	Number of Banks on SDRAM Device	4	4	04	04
18	CAS Latencies Supported	2,3	2,3	06	06
19	CS Latency	0	0	01	01
20	Write Latency	0	0	01	01
21	SDRAM Module Attributes	--- Unbuffered ---		00	00
22	SDRAM Device Attributes	+/-10% Vdd, Precharge All		07	07
23	Min. Clock Cycle Time at CL=2	10 ns	10 ns	A0	A0
24	Clock Access Time at CL=2 (tAC2)	6.0 ns	6.0 ns	60	60
25	Min. Clock Cycle Time at CL=1	N/A	N/A	00	00
26	Clock Access Time at CL=1 (tAC1)	N/A	N/A	00	00
27	Min. Row Precharge Time (tRP)	20 ns	20 ns	14	14
28	Min. Row-to-Row Delay (tRRD)	20 ns	20 ns	14	14
29	Min. RAS-to-CAS Delay (tRCD)	20 ns	20 ns	14	14
30	Min. RAS Pulse Width (tRAS)	45 ns	45 ns	2D	2D
31	Density of each bank on module	64MB	128MB	10	20
32	Cmd/Addr input set-up time	1.5 ns		15	15
33	Cmd/Addr input hold time	0.8 ns		08	08
34	Data input set-up time	1.5 ns		15	15
35	Data input hold time	0.8 ns		08	08
36-61	Superset Information	-	-	00	00
62	SPD Rev.	1.2		12	12
63	Checksum for bytes 0-62	-	-	9C	AD
64-71	JEDEC ID code	Enhanced Memory Systems		7F32FFFFFFFFFFF	
72	Manufacturing Location	-	-	xxxx	xxxx
73-90	Manufacturer's Part #	SM6408SDT	SM12808ASDT	xxxx	xxxx
91,92	PCB Rev. Code	-		rrrr	rrrr
93,94	Manufacturing Date	yyww code		yyww	yyww
95-98	Assembly Serial #	serial number		ssss	ssss
99-125	Manufacturer's Specific Data	open		00	00
126	Intel specification frequency	100MHz		64	64
127	Intel specification CL and clock support	-	-	AF	FF
128-255	Open for Customer Use	-	-	00	00

Serial Presence Detect (SPD) for SDRAM SODIMMs

Byte	Description	256MB	512MB	256MB	512MB
				** Hex Code **	
0	Number of bytes written into EEPROM	128	128	80	80
1	Total number of SPD bytes	256	256	08	08
2	Memory Type	SDRAM	SDRAM	04	04
3	Number of Row Addresses	12	13	0C	0D
4	Number of Column Addresses	10	10	0A	0A
5	Number of Module Banks	2	2	02	02
6	Module Data Width	x64	x64	40	40
7	Module Data Width (cont'd)	0	0	00	00
8	Voltage Interface Levels	LVTTL	LVTTL	01	01
9	Cycle Time at max CAS Latency	7.5 ns	7.5 ns	75	75
10	SDRAM Clock Access Time	5.4 ns	5.4 ns	54	54
11	DIMM config (non-parity, parity, ECC)	--- Non-parity ---		00	00
12	Refresh Rate and Type	--- 15.625us / Self ---	7.8 us	80	82
13	Primary SDRAM Width	x8	x8	08	08
14	Error Checking Data Width	N/A	N/A	00	00
15	Min. CAS-to-CAS Delay (tCCD)	1 clk	1 clk	01	01
16	Burst Lengths Supported	--- 1,2,4,8,Full Pg ---		8F	8F
17	Number of Banks on SDRAM Device	4	4	04	04
18	CAS Latencies Supported	2,3	2,3	06	06
19	CS Latency	0	0	01	01
20	Write Latency	0	0	01	01
21	SDRAM Module Attributes	--- Unbuffered ---		00	00
22	SDRAM Device Attributes	+/-10% Vdd, Precharge All		07	07
23	Min. Clock Cycle Time at CL=2	10 ns	10 ns	A0	A0
24	Clock Access Time at CL=2 (tAC2)	6.0 ns	6.0 ns	60	60
25	Min. Clock Cycle Time at CL=1	N/A	N/A	00	00
26	Clock Access Time at CL=1 (tAC1)	N/A	N/A	00	00
27	Min. Row Precharge Time (tRP)	20 ns	20 ns	14	14
28	Min. Row-to-Row Delay (tRRD)	20 ns	20 ns	14	14
29	Min. RAS-to-CAS Delay (tRCD)	20 ns	20 ns	14	14
30	Min. RAS Pulse Width (tRAS)	45 ns	45 ns	2D	2D
31	Density of each bank on module	128MB	256MB	20	40
32	Cmd/Addr input set-up time	1.5 ns		15	15
33	Cmd/Addr input hold time	0.8 ns		08	08
34	Data input set-up time	1.5 ns		15	15
35	Data input hold time	0.8 ns		08	08
36-61	Superset Information	-	-	00	00
62	SPD Rev.	1.2		12	12
63	Checksum for bytes 0-62	-	-	AE	D1
64-71	JEDEC ID code	Enhanced Memory Systems		7F32FFFFFFFFFFF	
72	Manufacturing Location	-	-	xxxx	xxxx
73-90	Manufacturer's Part #	SM25608ASDT	SM51208BSDT	xxxx	xxxx
91,92	PCB Rev. Code	-		rrrr	rrrr
93,94	Manufacturing Date	yyww code		yyww	yyww
95-98	Assembly Serial #	serial number		ssss	ssss
99-125	Manufacturer's Specific Data	open		00	00
126	Intel specification frequency	100MHz		64	64
127	Intel specification CL and clock support	-	-	AF	FF
128-255	Open for Customer Use	-	-	00	00

Mechanical Drawing



Dimensions: inches (mm)

Revision Log

Revision	Date	Summary of Changes
1.0	3/29/01	First Draft

Ordering Information

Part Number	Capacity	I/O Width	I/O Type	Package	Power Supply	Maximum Operating Frequency (MHz)
SM6408SDT-7.5	64 MB	x64	LVTTL	144-pin SODIMM	3.3V	133
SM12808ASDT-7.5	128 MB	x64	LVTTL	144-pin SODIMM	3.3V	133
SM25608ASDT-7.5	256 MB	x64	LVTTL	144-pin SODIMM	3.3V	133
SM51208BSDT-7.5	512 MB	x64	LVTTL	144-pin SODIMM	3.3V	133

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