



128Kx8 MONOLITHIC FLASH

PRELIMINARY*

FEATURES

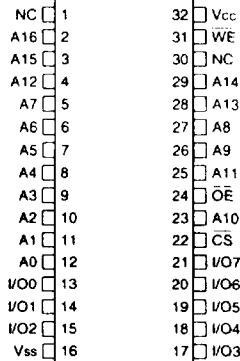
- Access Times of 60, 70, 90, 120 and 150nS
- Packaging
 - 32 pin, Hermetic Ceramic, 0.600" DIP (Package 300)
 - 32 lead, Hermetic Ceramic, 0.400" SOJ (Package 101)
- 10,000 Erase/Program Cycles
- Sector Erase Architecture
 - 8 equal size sectors of 16KBytes each
 - Any combination of sectors can be concurrently erased. Also supports full chip erase
- Organized as 128Kx8
- Commercial, Industrial and Military Temperature Ranges
- 5 Volt Programming. 5V ± 10% Supply.
- Low Power CMOS, 20mA Read Current, Typical
- Embedded Erase and Program Algorithms
- TTL Compatible Inputs and CMOS Outputs
- Built in Decoupling Caps for Low Noise Operation
- Page Program Operation and Internal Program Control Time

* This data sheet describes a product under development and is subject to change or cancellation without notice.

Note: Programming information available upon request.

PIN CONFIGURATION FOR WMF128K8-XXX5

32 DIP
32 CSOJ
TOP VIEW



PIN DESCRIPTION

A0-16	Address Inputs
I/O0-7	Data Input/Output
\overline{CS}	Chip Select
\overline{OE}	Output Enable
\overline{WE}	Write Enable
Vcc	+5.0V Power
Vss	Ground

WMES025*



ABSOLUTE MAXIMUM RATINGS

Table with 3 columns: Parameter, Value, Unit. Rows include Operating Temperature, Supply Voltage Range, Signal voltage range, Storage Temperature Range, Lead Temperature, Data Retention, Endurance, and A9 Voltage for sector protect.

RECOMMENDED OPERATING CONDITIONS

Table with 5 columns: Parameter, Symbol, Min, Max, Unit. Rows include Supply Voltage, Input High Voltage, Input Low Voltage, Operating Temp. (Mil.), Operating Temp. (Ind.), and A9 Voltage for Sector Protect.

CAPACITANCE (TA = +25°C)

Table with 5 columns: Parameter, Symbol, Conditions, Max, Unit. Rows include Address Input capacitance, Output Enable capacitance, Write Enable capacitance, Chip Select capacitance, and Data I/O capacitance.

This parameter is guaranteed by design but not tested.

NOTES:

- 1. Stresses above the absolute maximum rating may cause permanent damage to the device.
2. Minimum DC voltage on input or I/O pins is -0.5V.
3. Minimum DC input voltage on A9 pin is -0.5V.

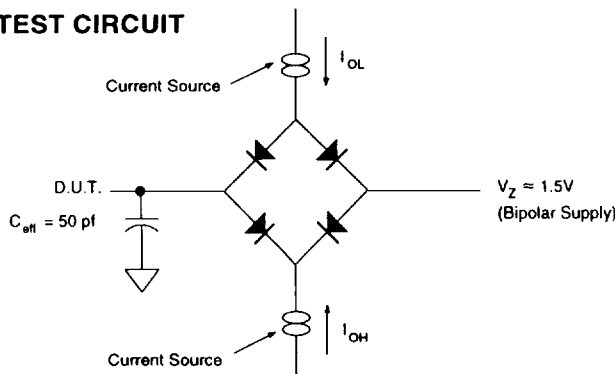
DC CHARACTERISTICS - CMOS COMPATIBLE (VCC = 5.0V, VSS = 0V, TA = -55°C to +125°C)

Table with 6 columns: Parameter, Symbol, Conditions, Min, Max, Unit. Rows include Input Leakage Current, Output Leakage Current, VCC Active Current for Read, VCC Active Current for Program or Erase, VCC Standby Current, Output Low Voltage, Output High Voltage, and Low VCC Lock Out Voltage.

NOTES:

- 1. The ICC current listed includes both the DC operating current and the frequency dependent component (at 5 MHz).
2. ICC active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: VIL = 0.3V, VIH = VCC - 0.3V

AC TEST CIRCUIT



AC TEST CONDITIONS

Table with 3 columns: Parameter, Typ, Unit. Rows include Input Pulse Levels, Input Rise and Fall, Input and Output Reference Level, and Output Timing Reference Level.

NOTES:

Vz is programmable from -2V to +7V. IOL & IOH programmable from 0 to 16mA. Tester Impedance Z0 = 75 Ohm. Vz is typically the midpoint of VOH and VOL. IOL & IOH are adjusted to simulate a typical resistive load circuit. ATE tester includes jig capacitance.



AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, WE CONTROLLED
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{AVAV}	t _{WC}	60		70		90		120		150		nS
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		0		0		0		nS
Write Enable Pulse Width	t _{WLWH}	t _{WP}	35		35		45		50		50		nS
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		0		0		nS
Data Setup Time	t _{DVWH}	t _{DS}	30		30		45		50		50		nS
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		0		0		nS
Address Hold Time	t _{WLAX}	t _{AH}	45		45		45		50		50		nS
Chip Select Hold Time	t _{WHEH}	t _{CH}	0		0		0		0		0		nS
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		20		20		20		nS
Duration of Byte Programming Operation (min)	t _{WHWH1}		14		14		14		14		14		μS
Chip and Sector Erase Time	t _{WHWH2}		2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	Sec
Read Recovery Time Before Write	t _{GHWL}		0		0		0		0		0		μS
V _{CC} Setup Time		t _{VCS}	50		50		50		50		50		μS
Chip Programming Time				12.5		12.5		12.5		12.5		12.5	Sec
Output Enable Setup Time		t _{OES}	0		0		0		0		0		nS
Output Enable Hold Time (1)		t _{OEH}	10		10		10		10		10		nS

1 For Toggle and Data Polling.

AC CHARACTERISTICS – READ ONLY OPERATIONS
(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{AVAV}	t _{RC}	60		70		90		120		150		nS
Address Access Time	t _{AVQV}	t _{ACC}		60		70		90		120		150	nS
Chip Select Access Time	t _{ELQV}	t _{CE}		60		70		90		120		150	nS
\overline{OE} to Output Valid	t _{GLQV}	t _{OE}		30		35		40		50		55	nS
Chip Select to Output High Z (1)	t _{EHQZ}	t _{OF}		20		20		25		30		35	nS
\overline{OE} High to Output High Z (1)	t _{GHQZ}	t _{OF}		20		20		25		30		35	nS
Output Hold from Address, \overline{CS} or \overline{OE} Change, whichever is first	t _{AXOX}	t _{OH}	0		0		0		0		0		nS

1 Guaranteed by design, not tested.

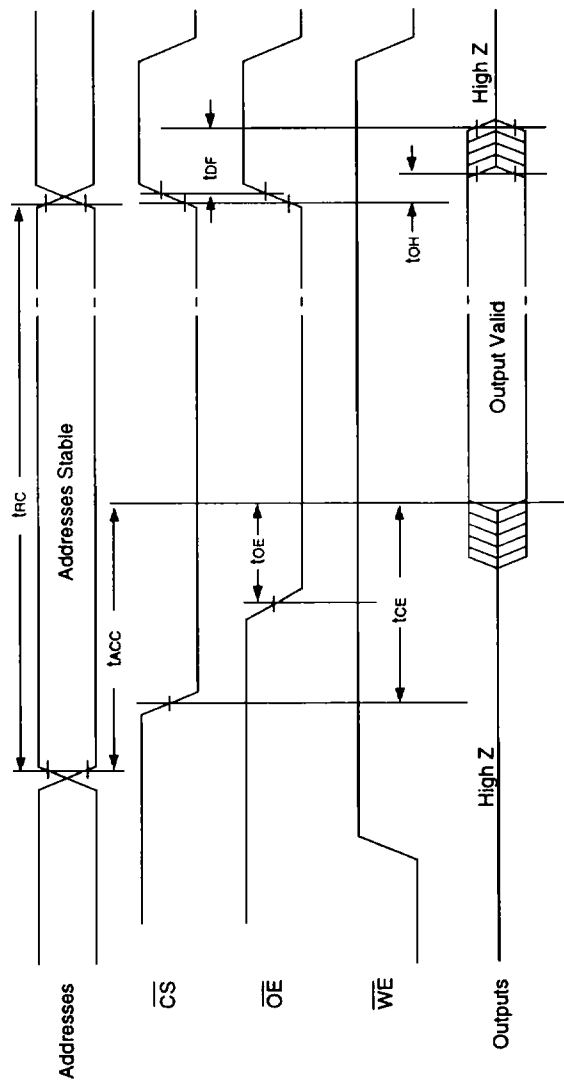


AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, \overline{CS} CONTROLLED
 (V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol		-60		-70		-90		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	tAVAV	tWC	60		70		90		120		150		nS
\overline{WE} Setup Time	tWLEL	tWS	0		0		0		0		0		nS
\overline{CS} Pulse Width	tELEH	tCP	30		35		45		50		55		nS
Address Setup Time	tAVEL	tAS	0		0		0		0		0		nS
Data Setup Time	tOVEH	tDS	30		30		45		50		55		nS
Data Hold Time	tEHDX	tDH	0		0		0		0		0		nS
Address Hold Time	tELAX	tAH	45		45		45		50		55		nS
\overline{WE} Hold from \overline{WE} High	tEHWH	tWH	0		0		0		0		0		nS
\overline{CS} Pulse Width High	tEHEL	tCPH	20		20		20		20		20		nS
Duration of Programming Operation	tWHWH1		14		14		14		14		14		μS
Duration of Erase Operation	tWHWH2		2.2	60	2.2	60	2.2	60	2.2	60	2.2	60	Sec
Read Recovery before Write	tGHEL		0		0		0		0		0		nS
Chip Programming Time				12.5		12.5		12.5		12.5		12.5	Sec

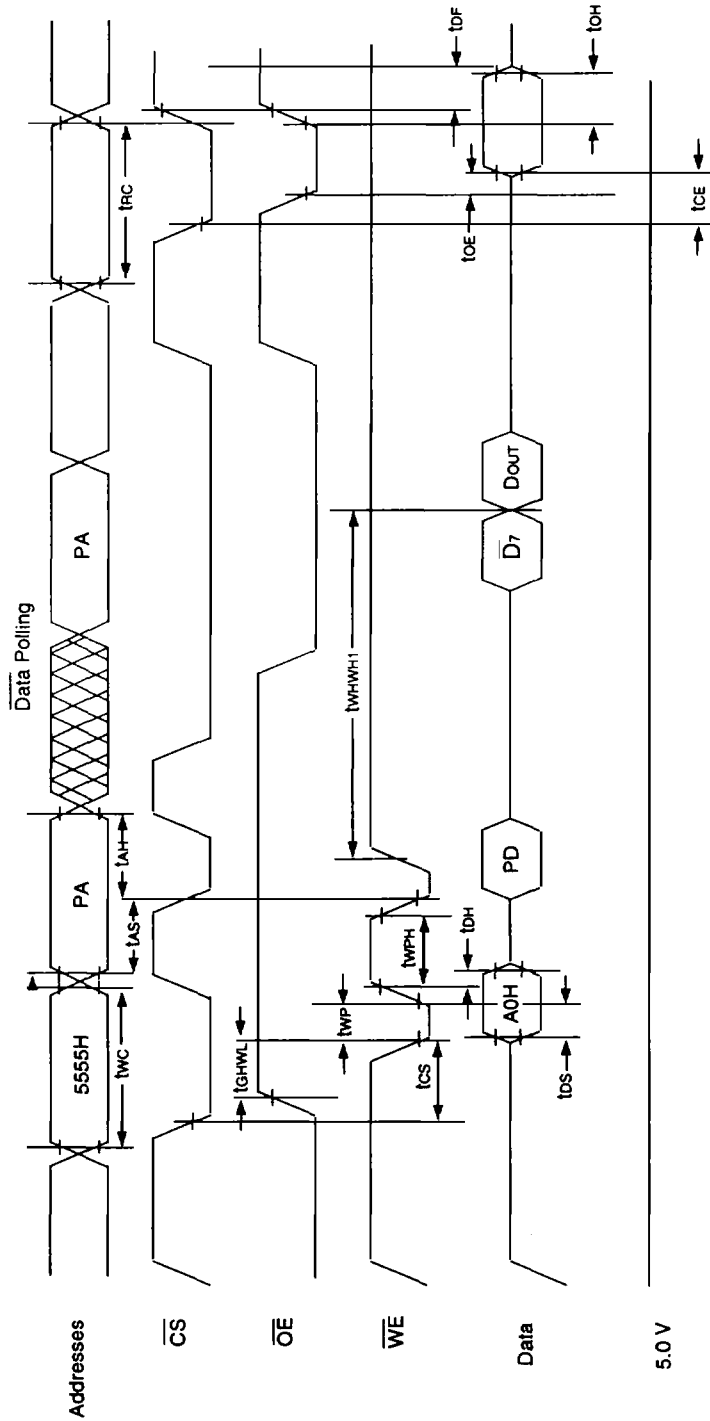


AC WAVEFORMS FOR READ OPERATIONS





WRITE/ERASE/PROGRAM OPERATION, WE CONTROLLED

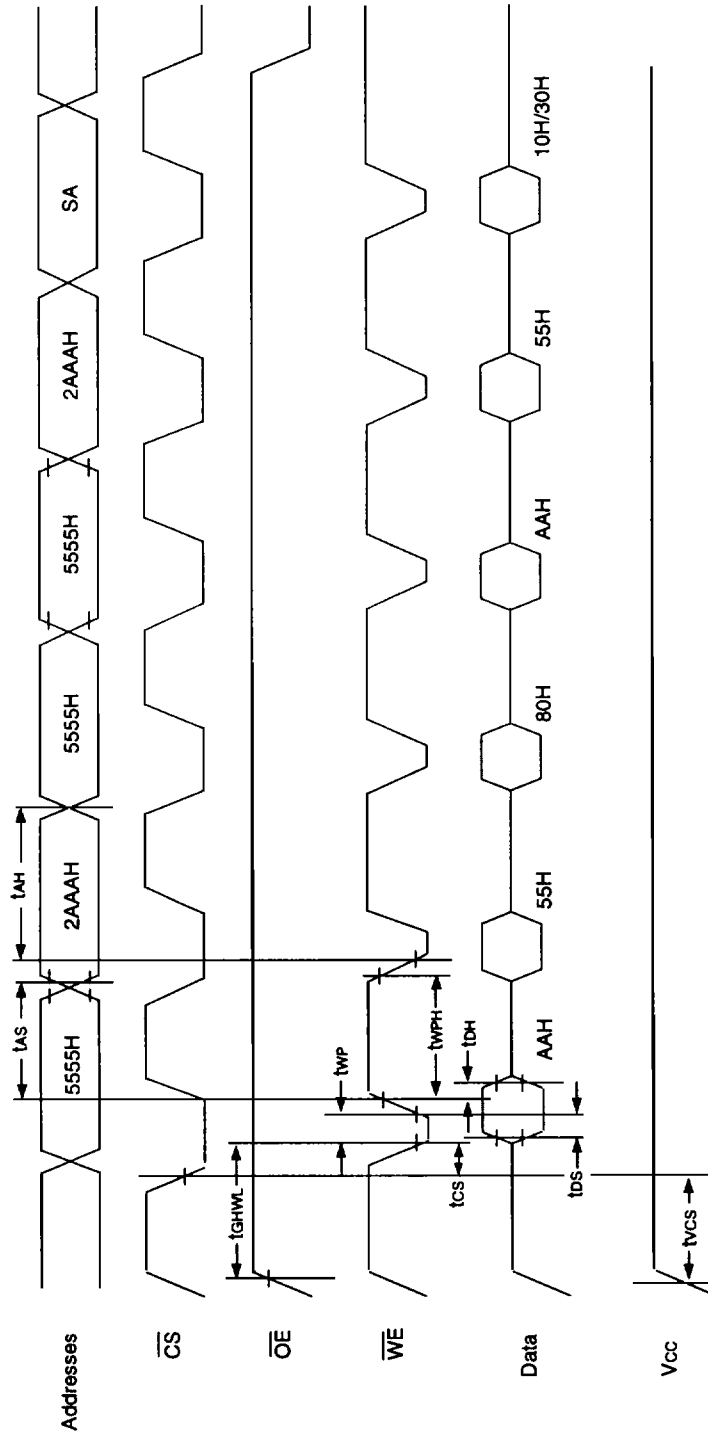


NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D7 is the output of the complement of the data written to the device.
4. DOUT is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.



AC WAVEFORMS CHIP/SECTOR ERASE OPERATIONS

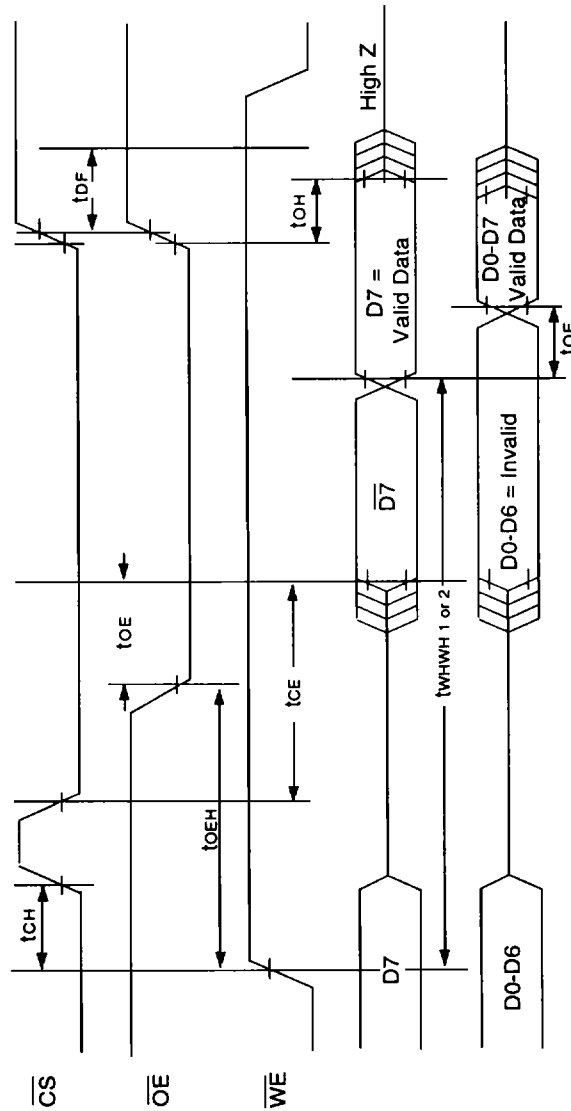


NOTES:

- 1. SA is the sector address for Sector Erase.

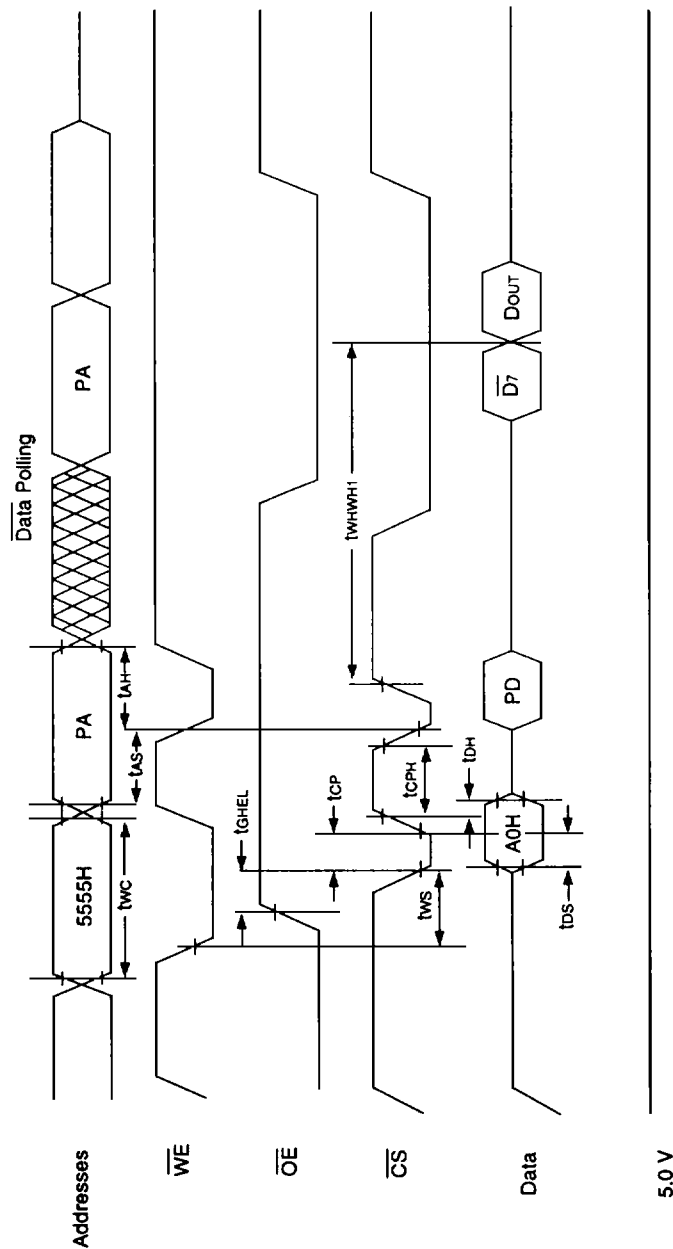


AC WAVEFORMS FOR DATA POLLING DURING EMBEDDED ALGORITHM OPERATIONS





WRITE/ERASE/PROGRAM OPERATION, \overline{CS} CONTROLLED

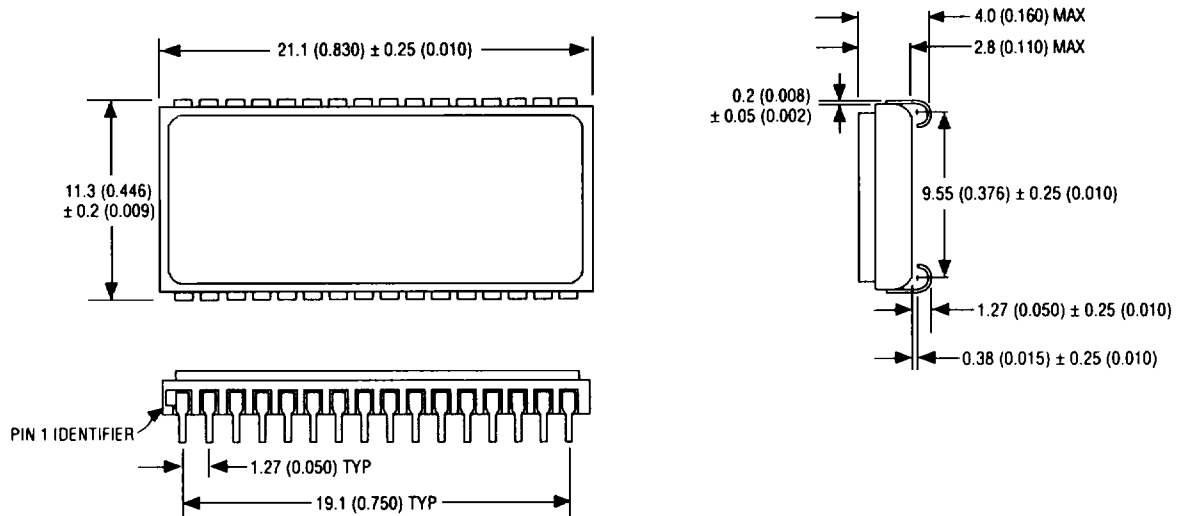


NOTES:

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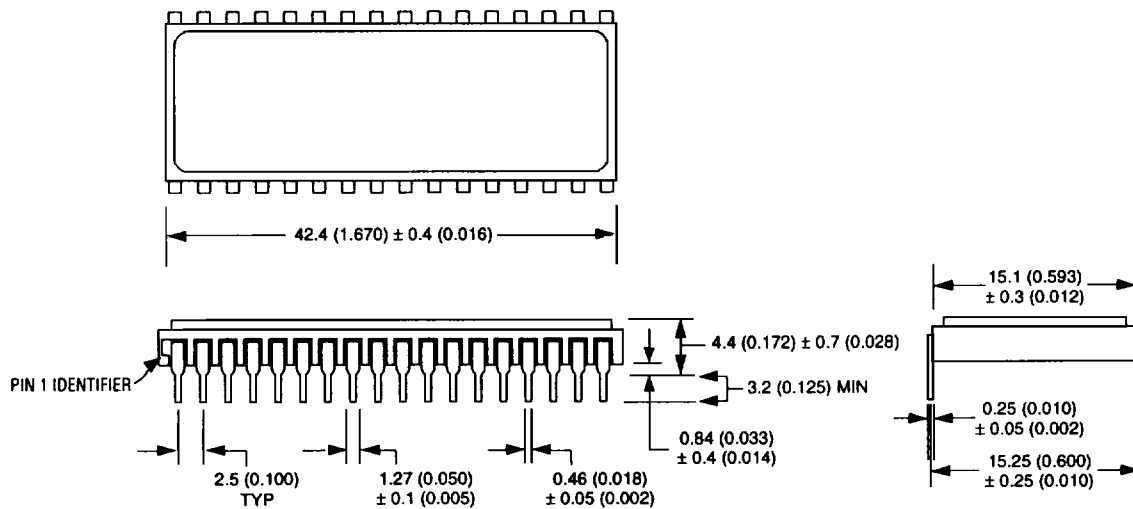


PACKAGE 101: 32 LEAD, CERAMIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 300: 32 PIN, CERAMIC DIP, SINGLE CAVITY SIDE BRAZED



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

