

# 2N6905 SERIES

## N-Channel JFET Pairs

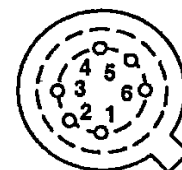
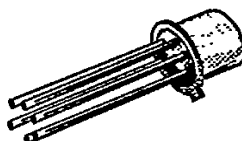
The 2N6905 Series of high-performance monolithic dual JFETs features extremely low noise, tight offset voltage and drift over temperature specifications. It is targeted for use in a wide range of precision instrumentation applications. The 2N6905 Series has a wide selection of both offset and drift ranges with the prime device, the 2N6905, featuring 5 mV offset and 10  $\mu\text{V}/^\circ\text{C}$  drift. The three devices allow designers to make important cost/benefit decisions. This series is available in a TO-71 hermetically sealed package and is available with military screening. (See Section 1.)

For additional design information please see performance curves NNR, which are located in Section 7.

PART NUMBER	$V_{(BR)GSS}$ MIN (V)	$g_{fs}$ MIN (mS)	$I_G$ MAX (pA)	$ V_{GS1} - V_{GS2} $ MAX (mV)
2N6905	-35	2	-5	5
2N6906	-35	2	-5	10
2N6907	-35	2	-5	25

TO-71

BOTTOM VIEW



- 1 SOURCE 1
- 2 DRAIN 1
- 3 GATE 1
- 4 SOURCE 2
- 5 DRAIN 2
- 6 GATE 2

## SIMILAR PRODUCTS

- High-Gain, See 2N5911 Series
- SO-8, See SST404 Series
- Chips, Order 2N690XCHP

## ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMIT	UNITS	
Gate-Drain Voltage	$V_{GD}$	-35	V	
Gate-Source Voltage	$V_{GS}$	-35		
Forward Gate Current	$I_G$	10	mA	
Power Dissipation	$P_D$	Per Side	300	mW
		Total	500	
Power Derating		Per Side	2.6	mW/ $^\circ\text{C}$
		Total	5	
Operating Junction Temperature	$T_J$	-55 to 150	$^\circ\text{C}$	
Storage Temperature	$T_{stg}$	-65 to 200		
Lead Temperature (1/16" from case for 10 seconds)	$T_L$	300		



ELECTRICAL CHARACTERISTICS <sup>1</sup>				LIMITS						
PARAMETER	SYMBOL	TEST CONDITIONS	TYP <sup>2</sup>	2N6905		2N6906		2N6907		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
<b>STATIC</b>										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	$I_G = -1 \mu A, V_{DS} = 0 V$	-55	-35		-35		-35		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	$V_{DS} = 15 V, I_D = 1 nA$	-1.5	-0.2	-3	-0.2	-3	-0.2	-3	
Saturation Drain Current <sup>3</sup>	$I_{DSS}$	$V_{DS} = 10 V, V_{GS} = 0 V$	3.5	0.5	10	0.5	10	0.5	10	mA
Gate Reverse Current	$I_{GSS}$	$V_{GS} = -15 V, V_{DS} = 0 V$								
			$T_A = 125^\circ C$	-2		-15		-15		-15
Gate Operating Current	$I_G$	$V_{DG} = 15 V, I_D = 200 \mu A$								
			$T_A = 125^\circ C$	-2		-5		-5		-5
Drain-Source On-Resistance <sup>4</sup>	$r_{DS(ON)}$	$V_{GS} = 0 V, I_D = 0.1 mA$								
				250						
Gate-Source Voltage	$V_{GS}$	$V_{DG} = 15 V, I_D = 200 \mu A$	-1		-2.3		-2.3		-2.3	V
Gate-Source Forward Voltage <sup>4</sup>	$V_{GS(F)}$	$I_G = 1 mA, V_{DS} = 0 V$	0.7							
<b>DYNAMIC</b>										
Common-Source Forward Transconductance	$g_{fs}$	$V_{DS} = 10 V, V_{GS} = 0 V, f = 1 kHz$	4	2	7	2	7	2	7	mS
Common-Source Output Conductance	$g_{os}$		4		20		20		20	$\mu S$
Common-Source Input Capacitance	$C_{iss}$	$V_{DG} = 15 V, I_D = 200 \mu A, f = 1 MHz$	4		8		8		8	pF
Common-Source Reverse Transfer Capacitance	$C_{rss}$		1.5		3		3		3	
Equivalent Input Noise Voltage	$\bar{e}_n$	$V_{DS} = 10 V, V_{GS} = 0 V, f = 10 Hz$	10		15		15		15	$nV/\sqrt{Hz}$
<b>MATCHING</b>										
Differential Gate-Source Voltage	$ V_{GS1} - V_{GS2} $	$V_{DG} = 10 V, I_D = 200 \mu A$			5		10		25	mV
Gate-Source Voltage Differential Change with Temperature	$\frac{\Delta  V_{GS1} - V_{GS2} }{\Delta T}$	$V_{DG} = 10 V, I_D = 200 \mu A$	$T = -55 to 25^\circ C$		10		25		25	$\mu V/^\circ C$
			$T = 25 to 125^\circ C$		10		25		50	
Saturation Drain Current Ratio <sup>4</sup>	$\frac{I_{DSS1}}{I_{DSS2}}$	$V_{DS} = 10 V, V_{GS} = 0 V$	0.97							
Transconductance Ratio <sup>4</sup>	$\frac{g_{fs1}}{g_{fs2}}$	$V_{DG} = 10 V, I_D = 0.2 mA, f = 1 kHz$	0.97							
Differential Output Conductance <sup>4</sup>	$ g_{os1} - g_{os2} $		0.1							$\mu S$
Differential Gate Current <sup>4</sup>	$ I_{G1} - I_{G2} $	$V_{DG} = 15 V, I_D = 0.2 mA, T_A = 25^\circ C$	1							pA
Common Mode Rejection Ratio	CMRR	$V_{DG} = 10 to 20 V, I_D = 200 \mu A$	102	95		95		95		dB

- NOTES: 1.  $T_A = 25^\circ C$  unless otherwise noted.  
 2. For design aid only, not subject to production testing.  
 3. Pulse test; PW = 300  $\mu s$ , duty cycle  $\leq 3\%$ .  
 4. This parameter not registered with JEDEC.