19-5482; Rev 3; 8/10

5-Cell to 10-Cell Li+ Protector with Cell Balancing

DS2726

General Description

The DS2726 provides full charge and discharge protection for 5- to 10-cell lithium-ion (Li+) battery packs. The protection circuit monitors individual cell voltages to detect overvoltage and undervoltage conditions. Protection against discharge overcurrent and short-circuit current is provided with user-selectable thresholds using external resistors. P-channel protection FETs are employed high side and driven from on-chip 10V FET drivers. Cell balancing can be enabled to ensure that all cells are equally charged.

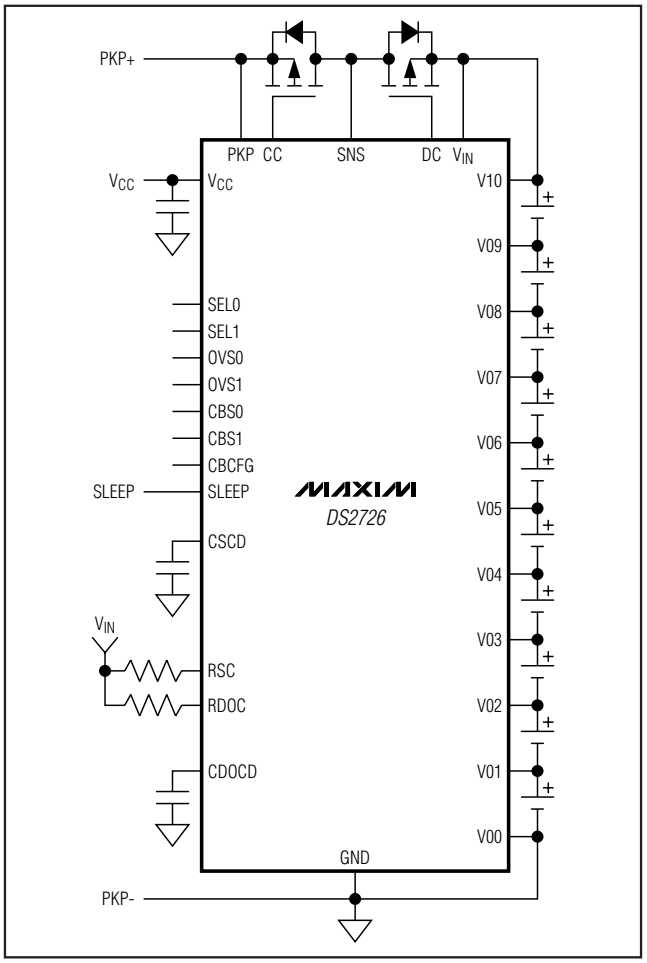
Applications

Power Tools

Electric Bikes

Home Appliances

Simplified Typical Application Circuit



Features

- **Complete Protection for 5-Cell to 10-Cell Li+ Packs**
- **Pin Programmable for 5 to 10 Cells**
- **Internal Cell-Balancing Circuit, Shunts Up to 300mA**
- **Pin-Programmable V_{OV} Threshold**
- **Pin-Programmable Cell-Balance Voltage**
- **Overdischarge Current and Short-Circuit Current Set with External Resistors**
- **Overdischarge Current and Short-Circuit Current Timeout Delay Set with External Capacitors**
- **Low Power Consumption: 60µA (typ)**
- **Low Shutdown Power Consumption: 5µA (typ)**
- **7mm x 7mm, 32-Pin TQFN Lead-Free Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS2726G+	-20°C to +85°C	32 TQFN-EP*
DS2726G+T&R	-20°C to +85°C	32 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
T&R = Tape and reel.
**EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

5-Cell to 10-Cell Li+ Protector with Cell Balancing

ABSOLUTE MAXIMUM RATINGS

Voltage Range on V00–V10, PKP, RDOC, RSC Pins Relative to GND .....-0.3V to +60V
Voltage Range on DC Pin Relative to V_{IN} .....-12V to +0.3V
Voltage Range on CC Pin Relative to PKP.....-12V to +0.3V
Voltage Range on CSCD, SEL0, SEL1, OVS0, OVS1, CBS0, CBS1, SLEEP, CBCFG, V_{CC} Pins Relative to GND.....-0.3V to +6.0V
Human Body Model (HBM) ESD Limit of
V05–V09, PKP, CC, DC.....±500V
All Other Pins .....±2kV
Voltage Range on Any V_X to V_{X-1} (V10 to V09).....-0.3V to +12V
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 37mW/°C above +70°C) 2963mW
Junction Temperature.....+150°C
Operating Temperature Range .....-20°C to +85°C
Storage Temperature Range.....-55°C to +125°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -20°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Range	V_{IN}	(Notes 1, 2, 3, 4)	5		50	V
Input Range: SEL0, SEL1, OVS0, OVS1, CBS0, CBS1, CSCD, CDOCD, SLEEP, CBCFG		(Note 1)	-0.3		V_{CC} + 0.3	V

DC ELECTRICAL CHARACTERISTICS

(T_A = -20°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{DD}	Protector mode, no fault (Notes 4, 9)		70	90	µA
	I_{DD_BAL}	Load balancing (Note 11)			400	
	I_{SLEEP}	Sleep mode		5.0	7.5	
V00–V10 Leakage Current		All cell voltages = 4.2V (Note 10)	-2		+2	µA
Input Logic-High: SEL0, SEL1, OVS0, OVS1, CBS0, CBS1, SLEEP	V_{IH}	I_{LOAD} = 2µA (Notes 1, 5)	V_{CC} - 0.4			V
Input Logic-Mid: SEL0, SEL1, OVS0, OVS1, CBS0, CBS1, SLEEP	V_{IM}	I_{LOAD} = 0 (Notes 1, 5)	1.30	1.65	2.00	V
Input Logic-Low: SEL0, SEL1, OVS0, OVS1, CBS0, CBS1, SLEEP	V_{IL}	I_{LOAD} = -2µA (Notes 1, 5)			V_{GND} + 0.4	V
V_{CC} Output Voltage		I_{LOAD} = 1mA (Notes 1, 5, 8)	4.75	5.00	5.25	V
V_{CC} Dropout Voltage		(Note 6)			5.5	V
Output Low: CC	V_{OLCC}	I_{OL} = -100µA, $V_{PKP} \geq$ 13V (Notes 3, 5)	V_{PKP} - 12		V_{PKP} - 8	V
Output Low: CC Driver Current		CC = V_{OLCC} + 2V	-3		-1	mA
		CC = V_{OHCC} - 1V	-15		-7	

DC ELECTRICAL CHARACTERISTICS (continued)

(T_A = -20°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High: CC	V_{OHCC}	I_{OH} = 100µA	V_{PKP} - 0.5		V_{PKP} + 0.3	V
Output High: CC Driver Current		CC = V_{OLCC} + 2V	7		15	mA
		CC = V_{OHCC} - 1V	0.5		1.5	
Output Low: DC	V_{OLDC}	I_{OL} = -100µA, $V_{IN} \geq$ 13V (Notes 3, 5)	V_{IN} - 12		V_{IN} - 8	V
Output Low: DC Driver Current		DC = V_{OLDC} + 2V	-3		-1	mA
		DC = V_{OHDC} - 1V	-15		-7	
Output High: DC	V_{OHDC}	I_{OH} = 100µA	V_{IN} - 0.5		V_{IN} + 0.3	V
Output High: DC Driver Current		DC = V_{OLDC} + 2V	7		15	mA
		DC = V_{OHDC} - 1V	0.5		1.5	
Maximum Balancing Current	I_{BAL}				300	mA
Balance FET: On-Resistance		I_{BAL} = 180mA	1.7	3.2	7.0	Ω

ELECTRICAL CHARACTERISTICS: PROTECTION CIRCUIT

(T_A = 0°C to +50°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overvoltage Detect	V_{OV}	OVS1 = GND, OVS0 = GND	4.05	4.10	4.15	V
		OVS1 = GND, OVS0 = N.C.	4.10	4.15	4.20	
		OVS1 = GND, OVS0 = V_{CC}	4.15	4.20	4.25	
		OVS1 = N.C., OVS0 = GND	4.20	4.25	4.30	
		OVS1 = N.C., OVS0 = N.C.	4.25	4.30	4.35	
		OVS1 = N.C., OVS0 = V_{CC}	4.30	4.35	4.40	
		OVS1 = V_{CC}, OVS0 = GND	4.35	4.40	4.45	
		OVS1 = V_{CC}, OVS0 = N.C.	4.40	4.45	4.50	
		OVS1 = V_{CC}, OVS0 = V_{CC}	4.45	4.50	4.55	
Charge-Enable Voltage	V_{CE}		V_{OVMIN} - 0.15		V_{OVMAX} - 0.15	V
Charge-Balance Voltage	V_{BAL}	V_{BAL} lowest typical set point limited to 3.75V	V_{OVMIN} - Cell-Balancing Threshold		V_{OVMAX} - Cell-Balancing Threshold	V
Undervoltage Release	V_{UVREL}		2.7	2.8	2.9	V
Undervoltage Detect	V_{UV}		2.2	2.3	2.4	V
RDOC, RSC Output Current		V_{IN} - V_{RDOC} = V_{IN} - V_{RSC} = 2V	0.95	1.00	1.05	µA
RDOC, RSC Input Offset Voltage			-3		+3	mV

5-Cell to 10-Cell Li+ Protector with Cell Balancing

ELECTRICAL CHARACTERISTICS: PROTECTION CIRCUIT (continued)

(T_A = 0°C to +50°C.)

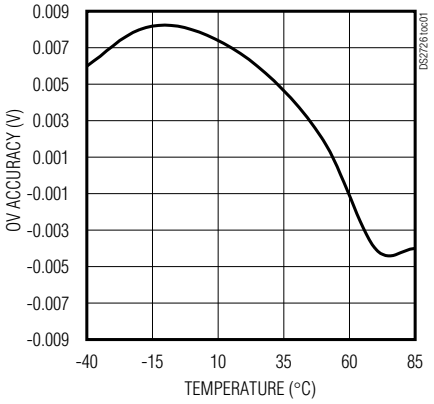
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Overvoltage Delay	t_{OVD}		128 x $t_{DOCDMIN}$		128 x $t_{DOCDMAX}$	ms
Undervoltage Delay	t_{UVD}		128 x $t_{DOCDMIN}$		128 x $t_{DOCDMAX}$	ms
Discharge Overcurrent Delay	t_{DOCD}	C_{DOCD} = 100pF (Notes 7, 12)	2.56	3.20	3.84	ms
		C_{DOCD} = 1000pF (Notes 7, 12)	25.6	32.0	38.4	
Short-Circuit Delay	t_{SCD}	C_{SCD} = 100pF (Notes 7, 12)	45	58	72	µs
		C_{SCD} = 1000pF (Notes 7, 12)	405	508	612	
Charger-Detect Threshold (V_{PKP} - V_{VIN})	V_{CDET}		3		17	mV
Test Threshold	V_{TP}	DOC conditions	0.8	1.2	1.7	V
Test Current	I_{TST}	DOC condition, V_{IN} - V_{PKP} = 2V	68	120	200	µA
		DOC condition, V_{IN} - V_{PKP} = 50V	0.5	1.20	1.8	mA

Note 1: All voltages relative to GND.
Note 2: Voltages below this level cannot be monitored; therefore, CC and DC are off below this value.
Note 3: Full-gate drive is not achieved until the voltage source for the gate driver (V_{PKP} or V_{VIN}) is above 13V.
Note 4: With 10µF decoupling capacitor.
Note 5: I_{LOAD} is the current load on the pin specified in the parameter.
Note 6: V_{CC} cannot meet specification if V_{VIN} is below this value.
Note 7: Capacitance tolerance introduces additional error.
Note 8: With ≥ 0.1µF decoupling capacitor.
Note 9: Current is an average. Spikes up to 200µA when measuring cell voltages.
Note 10: Current is an average. Spikes up to 15µA when measuring cell voltages.
Note 11: Current depends on the number of cells being balanced.
Note 12: Includes switching time and comparator delay with 25mV overdrive.

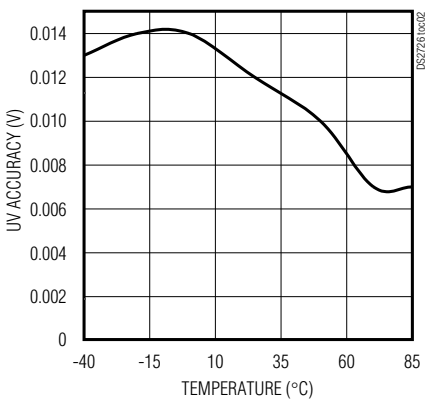
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

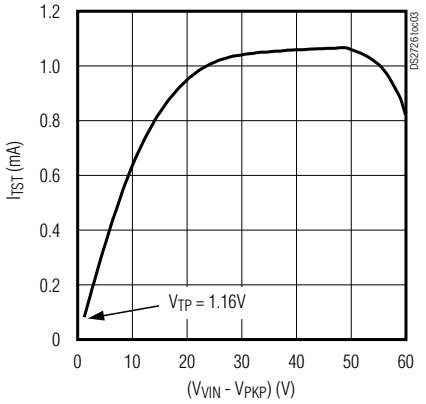
OV ACCURACY vs. TEMPERATURE



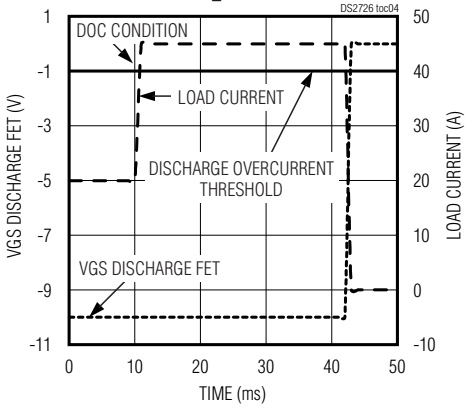
UV ACCURACY vs. TEMPERATURE



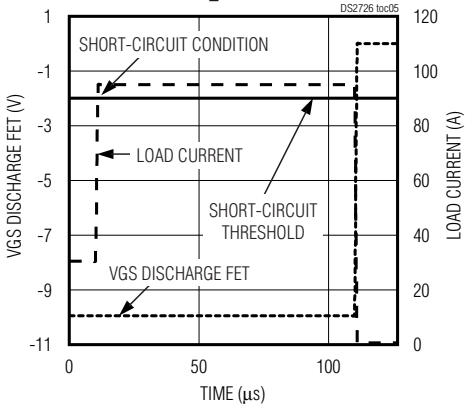
TEST CURRENT vs. (V_{VIN} - V_{PKP})



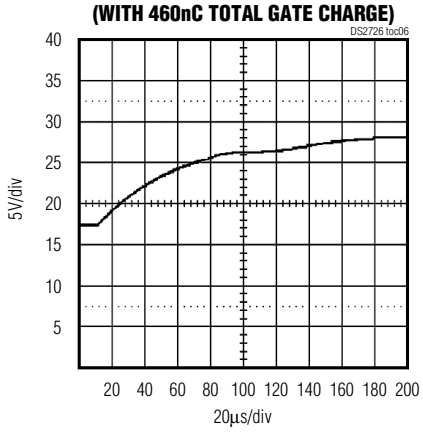
DISCHARGE OVERCURRENT DELAY
(CDOCD = 1000pF, R_{DOC} = 110kΩ
WITH R_{DS_ON} = 2.75kΩ)



SHORT-CIRCUIT DELAY
(CDOCD = 1000pF, RSC = 247.5kΩ
WITH R_{DS_ON} = 2.75MΩ)



FET TURN-OFF TIME
(WITH 460nC TOTAL GATE CHARGE)



5-Cell to 10-Cell Li+ Protector with Cell Balancing

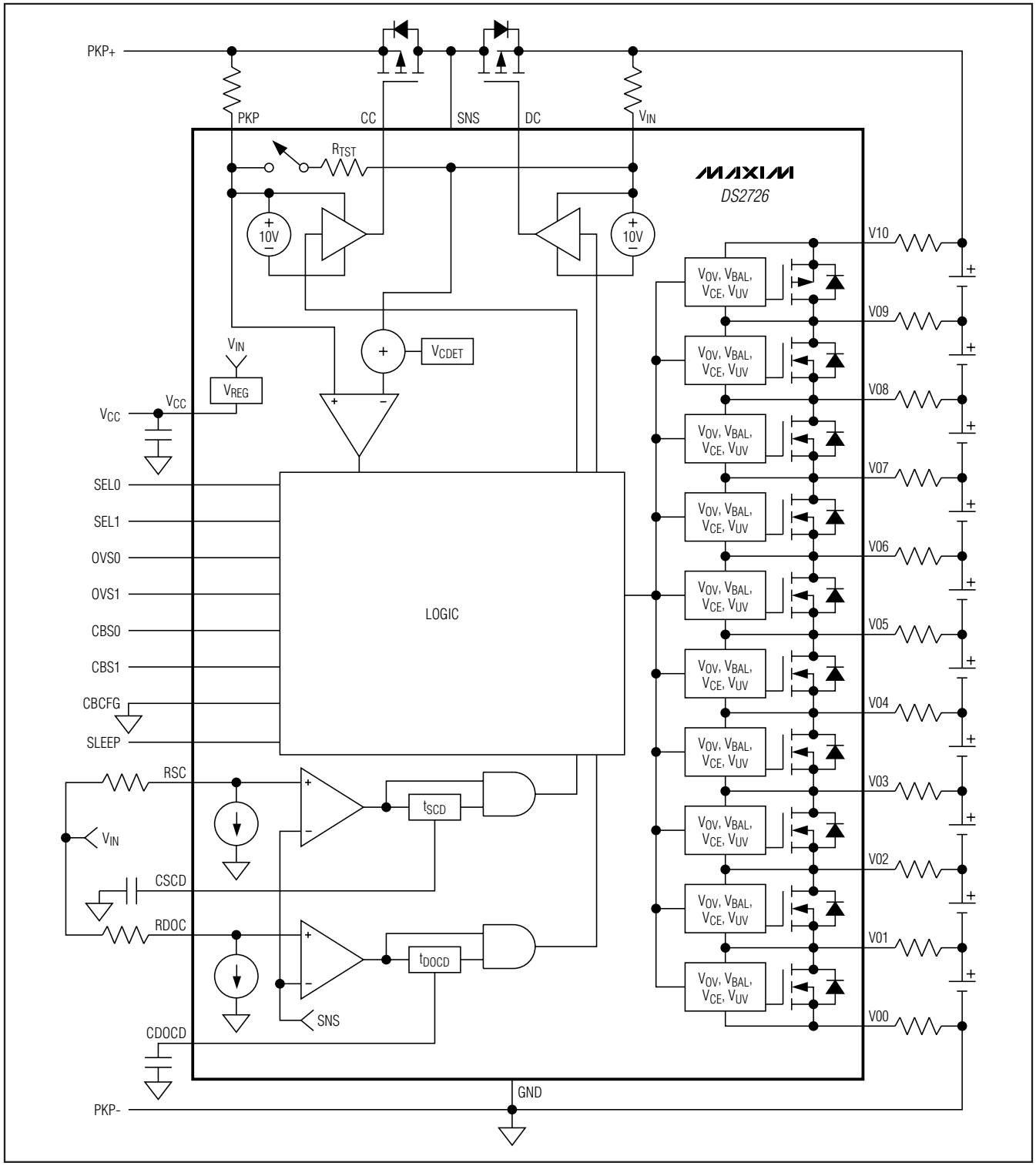


Figure 1. Block Diagram

Pin Description

PIN	NAME	FUNCTION
1	RSC	Short-Circuit Voltage Threshold. The resistor from this pin to the positive terminal of the cell stack selects the threshold voltage for a short-circuit condition in the discharge direction.
2	RDOC	Discharge Overcurrent Voltage Threshold. The resistor from this pin to the positive terminal of the cell stack selects the threshold voltage for an overcurrent condition in the discharge direction.
3	V_{CC}	Regulator Supply Output. V_{CC} supplies power to internal circuits and can be used to pull configuration pins to V_{IH}. It should be bypassed to GND with at least a 0.1µF ceramic capacitor.
4, 5	SEL0, SEL1	Select Number of Cells in the Battery Stack. This input is a three-level input. Connect to ground or V_{CC} for a logic-low or logic-high, respectively. Leave unconnected to achieve the midthreshold. See Table 2 for how to drive this pin for a particular number of cells.
6	CDOCD	Discharge Overcurrent Delay Time. Connect a capacitor from this pin to GND to select the amount of time for which a discharge overcurrent condition must persist before shutting off the DC FET.
7	SLEEP	Sleep-Mode Select Input. Driving this pin to a logic-low level forces the part into the lowest power state. The part exits Sleep Mode once a charge voltage is applied. When CBCFG is high, a logic-high on this pin enables cell balancing.
8	CSCD	Short-Circuit Current Delay Time. Connect a capacitor from this pin to GND to select the amount of time for which a short-circuit current condition must persist before shutting off the DC FET.
9	CBCFG	Charge-Balance Configuration Input. When this pin is at a logic-low, charge balancing is enabled if $V_{PKP} > V_{VIN} + V_{CDET}$. When this pin is at a logic-high, charge balancing is enabled if the SLEEP pin is at a logic-high.
10, 11	CBS0, CBS1	Select Cell-Balancing Voltage. This input is a three-level input. Connect to ground or V_{CC} for a logic-low or logic-high, respectively. Leave unconnected to achieve the midthreshold. See Table 4 for how to drive this pin for a particular cell-balancing voltage threshold.
12, 13	OVS0, OVS1	Select Overvoltage Threshold. This input is a three-level input. Connect to ground or V_{CC} for a logic-low or logic-high, respectively. Leave unconnected to achieve the midthreshold. See Table 3 for how to drive this pin for a particular overvoltage threshold.
14, 30	N.C.	No Connection. Not internally connected.
15	GND	Ground. Connect to the negative terminal of the lowest voltage cell.
16	V00	Negative Terminal Voltage Sense. Connect to the negative terminal of the 1st cell in the battery stack.
17	V01	Cell 01 Voltage Sense. Connect to the positive terminal of the 1st cell in the battery stack.
18	V02	Cell 02 Voltage Sense. Connect to the positive terminal of the 2nd cell in the battery stack.
19	V03	Cell 03 Voltage Sense. Connect to the positive terminal of the 3rd cell inf the battery stack.
20	V04	Cell 04 Voltage Sense. Connect to the positive terminal of the 4th cell in the battery stack.
21	V05	Cell 05 Voltage Sense. Connect to the positive terminal of the 5th cell in the battery stack.
22	V06	Cell 06 Voltage Sense. Connect to the positive terminal of the 6th cell in the battery stack.
23	V07	Cell 07 Voltage Sense. Connect to the positive terminal of the 7th cell in the battery stack.
24	V08	Cell 08 Voltage Sense. Connect to the positive terminal of the 8th cell in the battery stack.
25	V09	Cell 09 Voltage Sense. Connect to the positive terminal of the 9th cell in the battery stack.
26	V10	Cell 10 Voltage Sense. Connect to the positive terminal of the 10th cell in the battery stack.
27	V_{IN}	Connect to the Most Positive Cell Terminal
28	DC	Discharge Control Output. DC controls the gate of the discharge FET. Driven from V_{IN} to V_{OLDC} to turn on and turn off the discharge FET.

5-Cell to 10-Cell Li+ Protector with Cell Balancing

Pin Description (continued)

PIN	NAME	FUNCTION
29	SNS	Sense Input. Connect to the drains of the charge and discharge FETs. Used as a voltage reference for detecting short-circuit and discharge overcurrent conditions.
31	CC	Charge Control Output. CC controls the gate of the charge FET. Driven from PKP to V_{OLCC} to turn on and turn off the charge FET.
32	PKP	Pack Positive. The voltage on PKP is used to detect charger-attach and protection-release conditions.
—	EP	Exposed Pad. Connect to the negative terminal of the lowest voltage potential cell.

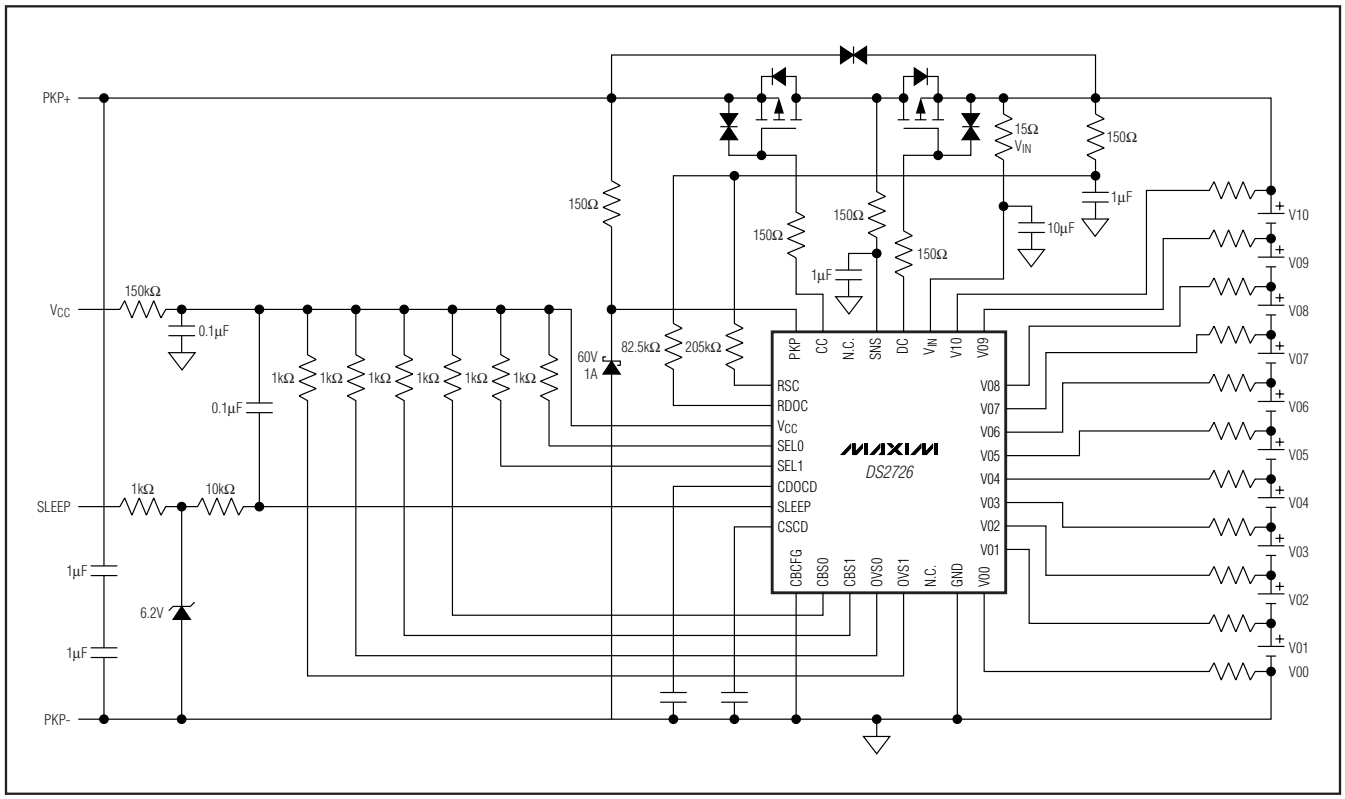


Figure 2. Typical Application Circuit

Detailed Description

The DS2726 provides the protection features for a 5-cell to 10-cell Li+ battery pack. The Li+ protection circuit allows for pin-configured selection of OV threshold and the cell-balancing threshold. DOC and SC thresholds and delays are component programmable.

Sleep Mode

Sleep Mode is a low-power state where the FETs are open and the IC is not monitoring voltages. During Wake Mode, the IC measures voltages and drives the FETs to the appropriate state.

Upon initial connection to cells, the DS2726 enters Sleep Mode. The IC also enters Sleep Mode if a UV condition is detected. Sleep Mode can be initiated any time by pulling the SLEEP pin low while a charger-detect condition does not exist. During Sleep Mode there is a pulldown current from PKP to GND.

V_{PKP} must be within V_{TP} of V_{VIN} ($V_{PKP} > V_{VIN} - V_{TP}$) to exit wake from Sleep Mode.

When a charger is detected and V_{CC} achieves regulation, the part measures all cells for undervoltage and overvoltage. Then the IC begins controlling the CC and DC FETs as shown in Table 1. Care should be taken to ensure that the SLEEP pin is not held low during a wake condition.

Charger Detect

The DS2726 has two different methods for detecting a charger connection. The methods are pin programmable at the CBCFG pin. If CBCFG is pulled to GND, then charge detection occurs when $V_{PKP} > V_{VIN} + V_{CDET}$. If CBCFG is pulled to V_{CC}, then charge detection occurs when the SLEEP pin is driven to a logic-high state.

Li+ Protection Circuitry

In Active Mode, the DS2726 constantly monitors V00–V10 to protect the battery from overvoltage and undervoltage. The voltage on the SNS pin is monitored and compared to the voltages on RDOC and RSC to protect against excessive discharge currents (discharge overcurrent and short circuit). Table 1 summarizes the conditions that activate the protection circuit, the response of the DS2726, and the thresholds that release it from a protection state.

Table 1. Li+ Protection Conditions and DS2726 Responses

CONDITION*	ACTIVATION			RELEASE THRESHOLD
	THRESHOLD	DELAY	RESPONSE	
Overvoltage (OV)	$V_{CELL} > V_{OV}$	t_{OVD}	CC Off	$V_{CELL} < V_{CE}$
Undervoltage (UV) (Note 15)	$V_{CELL} < V_{UV}$	t_{UVD}	CC Off, DC Off, Sleep Mode	CBCFG < V_{IL} and $V_{CELL} < V_{UV\_REL}$, then $V_{PKP} > V_{VIN} + V_{CDET}$ (Note 13)
				CBCFG < V_{IL} and $V_{CELL} > V_{UV\_REL}$, then $V_{PKP} > V_{VIN} - V_{TP}$
				CBCFG > V_{IH} then SLEEP > V_{IH} and $V_{PKP} > V_{VIN} - V_{TP}$
Discharge Overcurrent (DOC) (Note 15)	$V_{SNS} < V_{RDOC}$	t_{DOCD}	DC Off	$V_{PKP} > V_{VIN} - V_{TP}$ (Note 14)
Short Circuit (SC)	$V_{SNS} < V_{RSC}$	t_{SCD}	DC Off	$V_{PKP} > V_{VIN} - V_{TP}$ (Note 15)

**All voltages are with respect to GND. CC Off: $V_{CC} = V_{PKP}$, DC Off: $V_{DC} = V_{VIN}$.*

Note 13: *The DC FET remains off until $V_{CELL} > V_{UV\_REL}$.*

Note 14: *With test current I_{TST} flowing from V_{IN} to PKP.*

Note 15: *If a DOC condition persists indefinitely and a UV condition is reached, the IC does not enter Sleep Mode.*

5-Cell to 10-Cell Li+ Protector with Cell Balancing

Li+ Protection Conditions

Overvoltage, OV. If any cell voltage (V_{CELL}) exceeds the overvoltage threshold, V_{OV}, for a period longer than overvoltage delay, t_{OVD}, the DS2726 shuts off the external charge FET. When V_{CELL} falls below the charge-enable threshold V_{CE}, the DS2726 turns the charge FET on. The discharge FET remains enabled during the overvoltage event. Care should be taken while discharging during an OV condition because the current drawn by the load is going through the body diode of the CC FET.

Undervoltage, UV. If V_{CELL} drops below the undervoltage threshold, V_{UV}, for a period longer than undervoltage delay, t_{UVD}, the DS2726 shuts off the charge and discharge FETs and enters Sleep Mode. The device remains in Sleep Mode until a charger is detected, at which point the DS2726 wakes up and enables the CC FET. The DC FET remains disabled until every cell is above the V_{UV_REL} threshold. Care should be taken while charging during a UV event because the charge current is flowing through the body diode of the DC FET.

Discharge Overcurrent, DOC. If V_{SNS} is less than V_{RDOC} for a period longer than t_{DOCD}, the DS2726 shuts off the external discharge FET. The discharge current path is not reestablished until V_{PKP} rises above $V_{VIN} - V_{TP}$. The DS2726 provides a test current of value I_{TST} from the PKP pin to the V_{IN} pin to detect the removal of the offending low-impedance load. I_{TST} is not disabled if an undervoltage condition is reached.

Short Circuit, SC. If V_{SNS} is less than V_{RSC} for a period longer than short-circuit delay t_{SCD}, the DS2726 shuts off the external discharge FET. The discharge current path is not reestablished until V_{PKP} rises above $V_{VIN} - V_{TP}$. The DS2726 provides a test current of value I_{TST} from the PKP pin to the V_{IN} pin to detect the removal of the short. I_{TST} is disabled if an undervoltage condition is reached.

Summary. All the protection conditions described are logic ORed to affect the CC and DC outputs:

DC = (Undervoltage) or (Discharge Overcurrent) or (Short Circuit)

$\overline{CC}$ = (Overvoltage) or (Undervoltage and $\overline{\text{Charger Detect}}$)

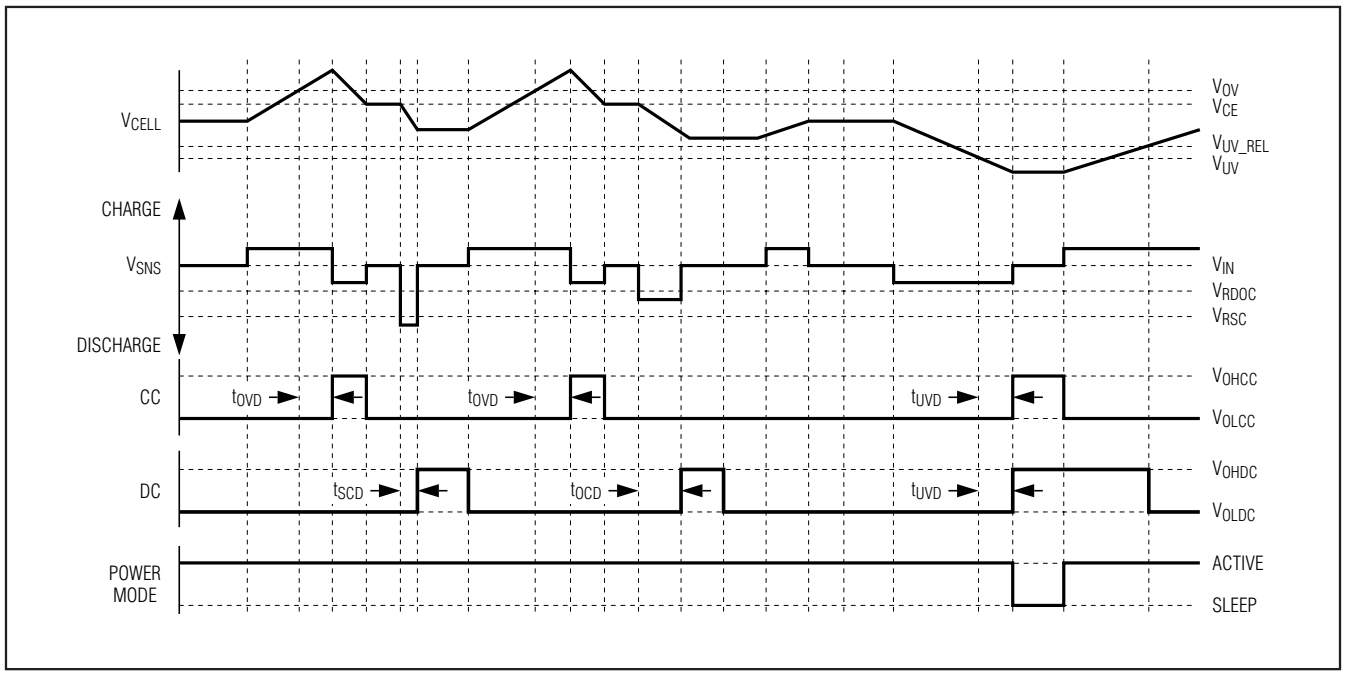


Figure 3. Li+ Protection Circuitry Example Waveforms

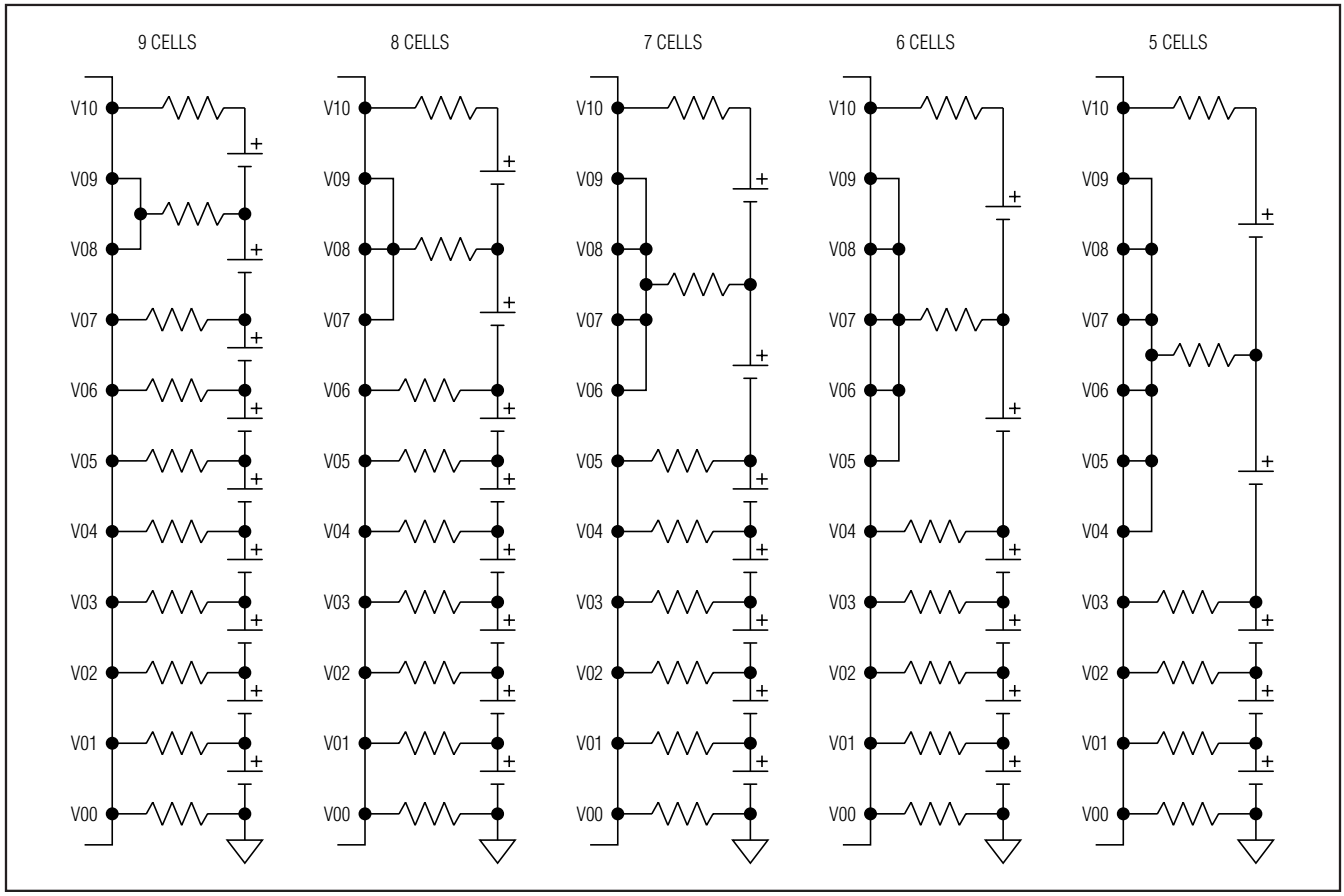


Figure 4. Cell Bypassing Connection

Configuration for Number of Cells

The DS2726 protects 5 to 10 Li+-based cells connected in series. The number of cells is configured using the SEL0 and SEL1 pins according to Table 2.

Pin V10 should always be connected to the positive terminal of the battery stack regardless of the number of cells in the stack. Cell connections that are not in use for battery stacks with fewer than 10 cells should be shorted to the cell connection below it. For example, a stack with 9 cells would have V9 shorted to V8 and V8 connected to the positive terminal of the 8th cell; a stack with 8 cells would have V9 shorted to V8 shorted to V7 and V7 connected to the positive terminal of the 7th cell, and so on (see Figure 4).

Cell Connection Order

Care must be taken when connecting cells to the DS2726 to avoid damaging the device. GND should be connected first, then V_{IN}. Next, V0 should be connected, then V1 and so on until V10 is connected last.

Table 2. Number of Cells Configuration

PIN	NUMBER OF SERIES-CONNECTED CELLS								
	5	6	7	8	9	10	10	10	10
SEL0	V_{IL}	V_{IM}	V_{IH}	V_{IL}	V_{IM}	V_{IH}	V_{IL}	V_{IM}	V_{IH}
SEL1	V_{IL}	V_{IL}	V_{IL}	V_{IM}	V_{IM}	V_{IM}	V_{IH}	V_{IH}	V_{IH}

Note: *The DC FET remains off until $V_{CELL} > V_{UV\_REL}$.*

5-Cell to 10-Cell Li+ Protector with Cell Balancing

Configuration of Overvoltage Threshold

The DS2726 allows the OV threshold to be set using the overvoltage select pins. The OV threshold is configured using the OVS0 and OVS1 pins according to Table 3.

Enabling Cell Balancing

For cell balancing to begin the DS2726 must detect a charger. The charge-balancing configuration pin (CBCFG) controls how the IC detects a charger. If CBCFG is pulled to GND, balancing is enabled when the charge-current comparator detects a charger. This detection occurs when $V_{PKP} > V_{VIN} + V_{CDET}$. If CBCFG is pulled to V_{CC}, cell balancing is enabled when the SLEEP pin is driven to a logic-high state. Note that cell balancing must be enabled and a valid cell-balancing voltage must exist for cell balancing to occur.

Configuration of Cell-Balancing Voltage Threshold

The DS2726 allows the cell-balancing threshold to be set using the cell-balance select pins. The threshold is configured using the CBS0 and CBS1 pins according to Table 4.

Setting the cell-balancing voltage threshold to zero disables the cell-balancing circuitry. The nominal cell-balancing voltage is never allowed a value below 3.75V. Setting the OVS0 and OVS1 pins low while the CBS0 and CBS1 pins are high results in a cell-balancing voltage (V_{BAL}) of 3.75V.

Nominal Cell-Balancing Voltage:

$V_{BAL} = V_{OV}$ – Cell-Balancing Voltage Threshold

Balancing begins when any cell's voltage is greater than V_{BAL}. When the balancing condition is met and cell balancing is enabled, the corresponding internal FET (from V_X to V_{X-1}) is enabled, shunting a portion of the charge current around the cell. The external resistors on V00–V10 should be chosen to limit the balancing current to a maximum of 200mA. This prevents damaging the internal cell-balancing FETs.

The DS2726 has three distinct states during balancing. A voltage measurement state of 5/32 t_{OCD} time periods is followed by a balancing state where even numbered cells are balanced for 123/32 t_{OCD} time periods. Another voltage measurement state of 5/32 t_{OCD} time periods then occurs. This is followed by a balancing state where odd numbered cells are balanced for 123/32 t_{OCD} time periods. This gives an average balancing current of approximately half the maximum balance current. Cell balancing terminates when all cell voltages are greater than V_{BAL}. See the *Measurement Sequence* section.

Table 3. OV Threshold Configuration

PIN	NOMINAL OV THRESHOLD (V)								
	4.10	4.15	4.20	4.25	4.30	4.35	4.40	4.45	4.50
OVS0	V_{IL}	V_{IM}	V_{IH}	V_{IL}	V_{IM}	V_{IH}	V_{IL}	V_{IM}	V_{IH}
OVS1	V_{IL}	V_{IL}	V_{IL}	V_{IM}	V_{IM}	V_{IM}	V_{IH}	V_{IH}	V_{IH}

Table 4. Cell-Balancing Threshold Configuration

PIN	CELL-BALANCING VOLTAGE THRESHOLD (OFFSET FROM V_{OV}) (V)								
	0.00	0.05	0.10	0.15	0.20	0.25	0.30	0.35	0.40
CBS0	V_{IL}	V_{IM}	V_{IH}	V_{IL}	V_{IM}	V_{IH}	V_{IL}	V_{IM}	V_{IH}
CBS1	V_{IL}	V_{IL}	V_{IL}	V_{IM}	V_{IM}	V_{IM}	V_{IH}	V_{IH}	V_{IH}

Setting the Short-Circuit Threshold and Delay Time

The DS2726 allows the selection of a short-circuit current threshold. This threshold is set using a resistor from the RSC pin to the positive terminal of the cell stack. The RSC pin sinks 1µA (nominal). The short-circuit comparator triggers when the voltage on the SNS pin is less than the voltage on the RSC pin. For example, assume a 500kΩ resistor is used on RSC, along with a DC FET with an R_{DS_ON} of 10mΩ. This corresponds to an RSC voltage of 500kΩ x 1µA = 0.5V. Because the FET is 10mΩ, the short-circuit threshold is 0.5V/10mΩ = 50A:

$$I_{SC} = \frac{1\mu A \times RSC}{R_{DS\_ON}}$$

The DS2726 allows for a delayed reaction to a short-circuit event. The short threshold must persist for the entire delay time before the DC FET begins to turn off (actual turn-off time varies based on the gate capacitance of the DC FET; see the DC pin drive capabilities in the *DC Electrical Characteristics* table for more details). The short-circuit delay time is set using a capacitor on the CSCD pin. The short-circuit delay time can be calculated by the equation:

$$t_{SCD} = C_{SCD} \times 500k\Omega$$

Be sure to select threshold and delay times that fall within the safe operating area of the FETs chosen for DC and CC.

Setting the Discharge Overcurrent Threshold and Delay Time

The DS2726 allows the selection of a discharge overcurrent threshold. This threshold is set using a resistor from the RDOC pin to the positive terminal of the cell stack. The RDOC pin sinks 1µA (nominal). The overcurrent circuit comparator triggers when the voltage on the SNS pin is less than the voltage on the RDOC pin. For example, assume a 200kΩ resistor is used on RDOC, along with a DC FET with an R_{DS_ON} of 10mΩ. This corresponds to a voltage on RDOC of 200kΩ x 1µA = 0.2V. Because the FET is 10mΩ, the discharge overcurrent threshold is 0.2V/10mΩ = 20A:

$$I_{DOC} = \frac{1\mu A \times R_{DOC}}{R_{DS\_ON}}$$

The DS2726 allows for a delayed reaction to a discharge overcurrent event. The discharge overcurrent threshold must persist for the entire delay time before the DC FET begins to turn off (actual turn-off time varies based on the gate capacitance of the DC FET; see DC pin drive capabilities in the *DC Electrical Characteristics* table for more details). The discharge overcurrent delay time is set using a capacitor on the CDOCD pin. The discharge overcurrent delay can be calculated by the equation:

$$t_{DOCD} = C_{DOCD} \times 32M\Omega$$

Be sure to select threshold and delay times that fall within the safe operating area for the FETs chosen for DC and CC.

If the voltage on the CDOCD pin is within approximately 1V of V_{CC} or GND, the condition is considered to be a fault, and the CC and DC outputs are disabled. This results in a delay before enabling the FETs when the part awakens from Sleep Mode. This delay occurs until the voltage on CDOCD reaches an acceptable level. This is a function of the capacitor on CDOCD. The CDOCD startup delay is in addition to a typical regulator startup of 100µs, and is given by the equation:

$$\text{STARTUP DELAY} \approx 100\mu s + C_{DOCD} \times 1.65M\Omega$$

Be sure to select threshold and delay times that fall within the safe operating area for the FETs chosen for DC and CC.

5-Cell to 10-Cell Li+ Protector with Cell Balancing

Measurement Sequence

The period with which the DS2726 measures voltages is a function of the discharge overcurrent delay time, t_{DOCD}. Figure 5 illustrates the measurement sequence.

One measurement period: 4 x t_{DOCD}

V_{UV}, V_{UV_REL}, V_{CE}, V_{OV}, and V_{BAL} are measured for all cells: 5 x $t_{DOCD}/32$

Chip performs balancing on even cells: 123 x $t_{DOCD}/32$

One measurement period: 4 x t_{DOCD}

V_{UV}, V_{UV_REL}, V_{CE}, V_{OV}, and V_{BAL} are measured for all cells: 5 x $t_{DOCD}/32$

Chip performs balancing on odd cells: 123 x $t_{DOCD}/32$

One cell-balancing period: 8 x t_{DOCD}

Overvoltage and Undervoltage Delay Time

Cell voltages are measured simultaneously and then sequentially compared to each of the five thresholds V_{UV}, V_{UV_REL}, V_{CE}, V_{OV}, and V_{BAL}. This sequence is repeated every four t_{DOCD} intervals. Overvoltage and undervoltage conditions are time qualified and therefore not recognized immediately. If an overvoltage condition exists on any cell for 32 intervals consecutively (t_{OVD} = 4 x 32 x t_{DOCD} = 128 x t_{DOCD}), an overvoltage condition is recognized, and the CC FET is turned off. If an undervoltage condition exists on any cell for 32 intervals consecutively (t_{UVD} = 4 x 32 x t_{DOCD} = 128 x t_{DOCD}) an undervoltage condition is recognized, the CC and DC FETs are turned off, and Sleep Mode is entered.

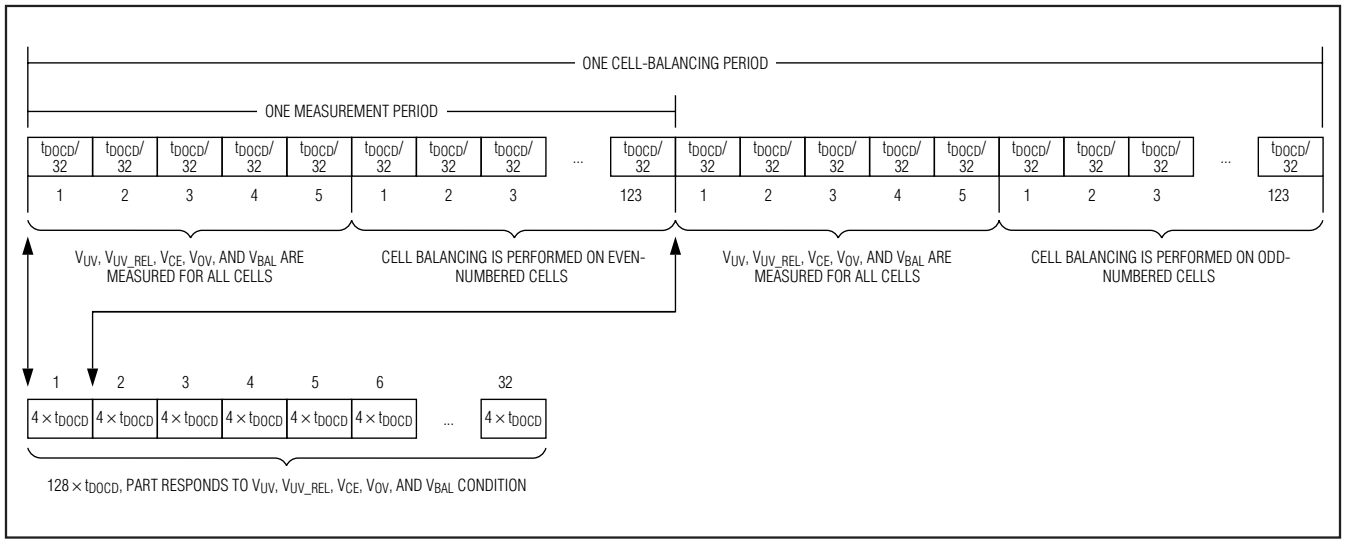
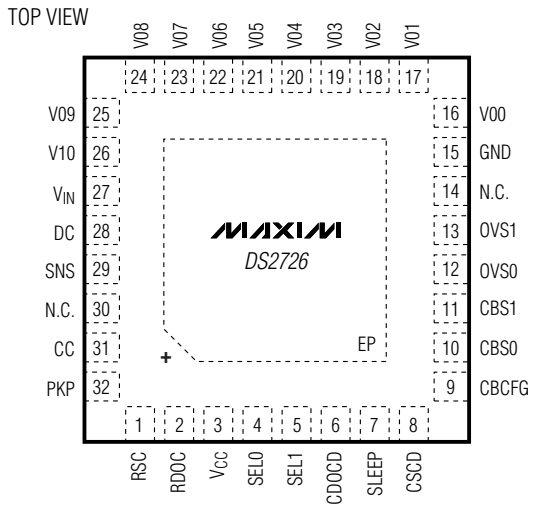


Figure 5. Cell Balancing and Measurement Periods

5-Cell to 10-Cell Li+ Protector with Cell Balancing

Pin Configuration



TQFN
(7mm × 7mm)

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
32 TQFN-EP	T3277+2	21-0144	90-0125

5-Cell to 10-Cell Li+ Protector with Cell Balancing

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/08	Initial release.	—
1	9/08	Deleted the "±50mV Overvoltage Accuracy" from the *Features* section, added the *Cell Connection Order* section, corrected wording mistake in the *Configuration of Cell-Balancing Voltage Threshold* section involving minimum cell-balancing voltage configuration.	1, 11, 12
2	1/09	Corrected PFET drawings in schematics, added the PKP, CC, DC pins to the Human Body Model (HBM) ESD Limit in the *Absolute Maximum Ratings*.	1, 2, 6, 8
3	8/10	Changed the operating temperature range from -40°C to +85°C to -20°C to +85°C in the *Absolute Maximum Ratings*.	2