

ELECTRICAL SPECIFICATIONS:

1.0 TURNS RATIO (P8-P6-P7) : (J1-J2)

(P2-P3-P1) : (J3-J6)

2.0 INDUCTANCE (P7-P8)

: 1CT : 1± 3%

1.0 PINS WITHOUT ELECTRICAL CONNECTION ARE OMITTED.

: 1CT : 1 ± 3%

: 350uH MIN. @ 0.1V , 100KHz, 8mA DC Bias

350uH MIN. @ 0.1V, 100KHz, 8mA DC Bias

(P1-P2)

3.0 LEAKAGE INDUCTANCE P8-P7 (WITH J1 AND J2 SHORT)

: 0.3 MAX. @ 1MHz

P2-P1 (WITH J3 AND J6 SHORT)

: 0.3 MAX. @ 1MHz

4.0 INTERWINDING CAPACITANCE (P8,P6,P7) TO (J1,J2)

(P3,P2,P1) TO (J6,J3)

: 25pf MAX @ 1MHz

: 25pf MAX, @ 1MHZ

5.0 DC RESISTANCE (J1-J2) (P1-P2)

: 1.2 ohms Max.

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of 4 SI-40239 REV.02

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6.0 RETURN LOSS:

60MHz TO 80MHz 1MHz TO 30MHz

12dB MIN, 18dB MIN.

7.0 VOLTAGE WITHSTAND

(J3, J6) TO (P1, P2)

(J1, J2) T0 (P8,P7)

8.0 INSERTION LOSS

100KHz TO 100MHz

1500 1500 <AC

9.0 RISE TIME:

DUTPUT VOLTAGE = 1 V peak

PULSE WIDTH= 112nS

1.1 dB TYP

3.0 nS MAX

10.0 CROSS TALK:

1MHz TO 100MHz

35 dB TYP

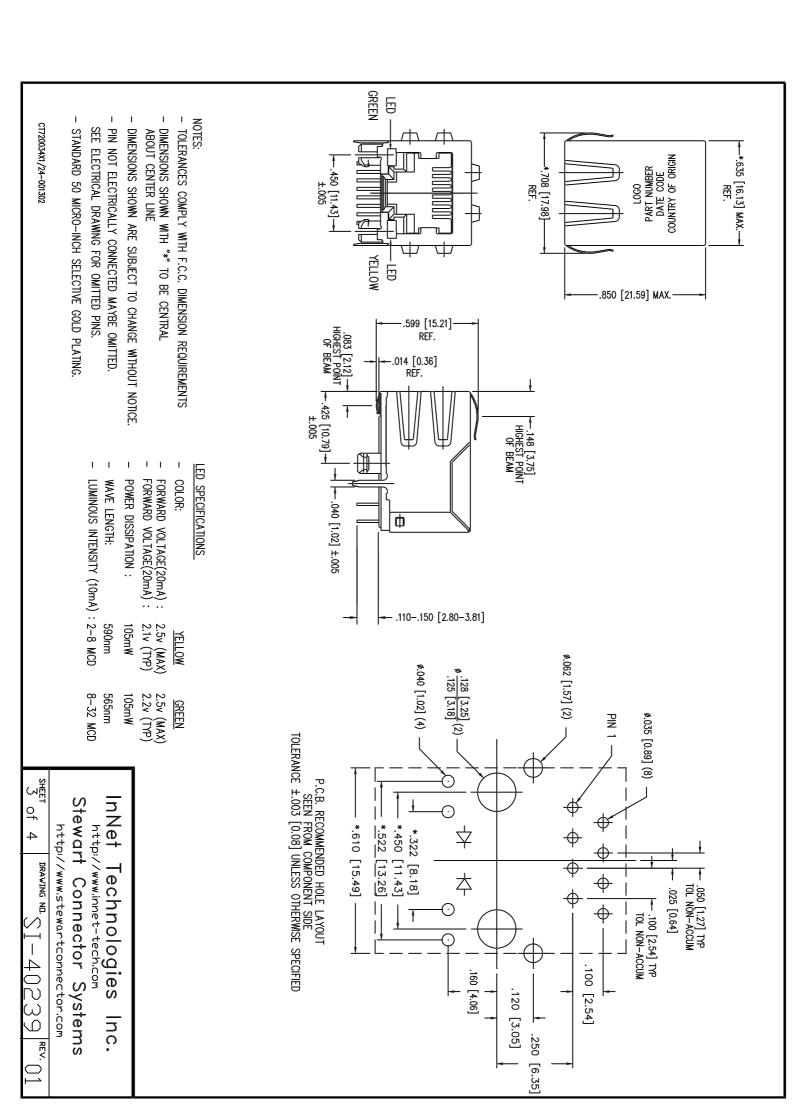
11.0 COMMON TO COMMON MODE ATTENUATION: 1MHz TO 100MHz

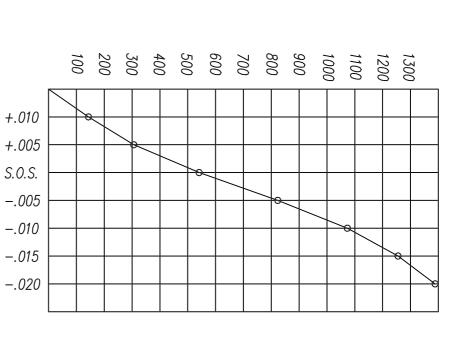
35dB TYP

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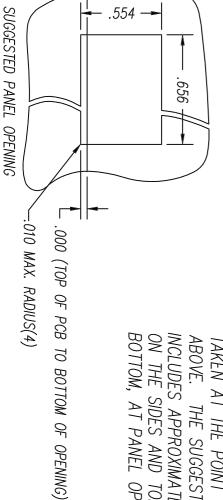
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SHEET 2 of 4









.080 WITH PANEL ₩ .275 MAX **₩** ф

POINT OF CONTACT

BOTTOM, AT PANEL OPENING. INCLUDES APPROXIMATELY .020 CLEARANCE ON THE SIDES AND TOP AND .013 ON THE ABOVE. ON THE GRAPH ARE GENERAL AVERAGES ASSEMBLY TOLERANCES. FORCE VALUES OF LOWER MATING FORCES OR TIGHTER CARRY SOME CONSEQUENCES IN THE FORM ADJUSTED IN EITHER DIRECTION BUT MAY REASONABLE JACK / PANEL CLEARANCES CAPABILITY. TAKEN AT THE POINT OF CONTACT SHOWN YET MAINTAIN RELIABLE GROUNDING TO GIVE THE USER THE ABILITY TO HAVE THE SUGGESTED PANEL OPENING IS INTENDED THE SUGGESTED PANEL OPENING THESE VARIABLES CAN BE

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SHEET 4 of 4

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DRAWING NO. SI-40239 REV. 01