



Pin Definition:
 1. Gate
 2. Drain
 3. Source

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (m Ω)	I_D (A)
55	8 @ $V_{GS} = 10V$	62

General Description

The TSM100N06 N-Channel Power MOSFET utilized advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well know for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance contribute to its wide acceptance throughout the industry.

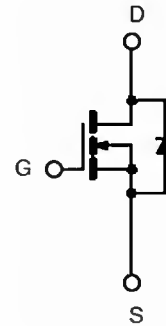
Features

- Advanced Process Technology
- Low $R_{DS(ON)}$ 8m Ω (Max.)
- Dynamic dv/dt Rating
- Fast Switching

Ordering Information

Part No.	Package	Packing
TSM110N06CZ C0	TO-220	50pcs / Tube

Block Diagram



N-Channel MOSFET

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

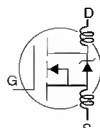
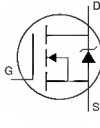
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V_{DS}	55	V	
Gate-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current	I_D	110	A	
Pulsed Drain Current *	I_{DM}	390	A	
Avalanche Current (Repetitive) (Note 1)	I_{AR}	62	A	
Repetitive Avalanche Energy (Note 1)	E_{AR}	20	mJ	
Maximum Power Dissipation	P_D	$T_c = 25^\circ C$	175	W
		Derate above 25°C	1.17	W/°C
Peak Diode Recovery dv/dt (Note 3)	dv/dt	5	V/nS	
Operating Junction Temperature	T_J	150	°C	
Storage Temperature Range	T_{STG}	-55 to +150	°C	

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	$R_{\theta_{JC}}$	0.85	°C/W
Thermal Resistance - Junction to Ambient	$R_{\theta_{JA}}$	62.5	°C/W

Notes: Surface mounted on FR4 board $t \leq 10sec$

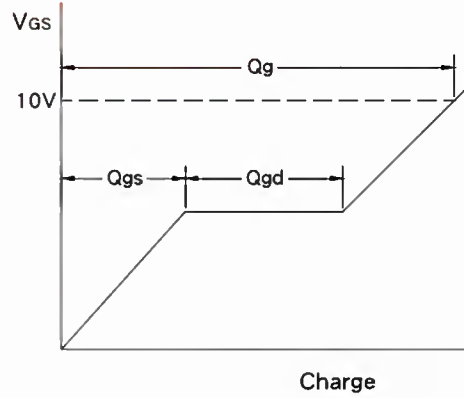
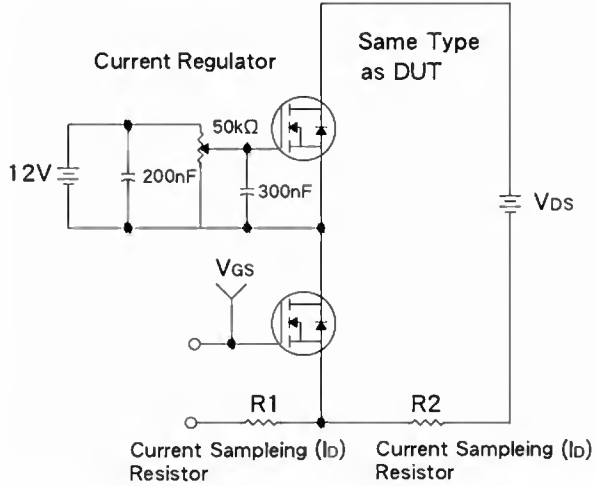
Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	55	--	--	V	
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 62A$	$R_{DS(ON)}$	--	6.5	8	mΩ	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2.0	--	4.0	V	
Zero Gate Voltage Drain Current	$V_{DS} = 55V, V_{GS} = 0V$	I_{DSS}	--	--	25	μA	
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	±100	nA	
Forward Transconductance	$V_{DS} = 25V, I_D = 62A$	g_{fs}	--	44	--	S	
Dynamic^b							
Total Gate Charge	$V_{DS} = 44V, I_D = 62A,$ $V_{GS} = 10V$	Q_g	--	87.8	--	nC	
Gate-Source Charge		Q_{gs}	--	22.8	--		
Gate-Drain Charge		Q_{gd}	--	28.2	--		
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0MHz$	C_{iss}	--	4590	--	pF	
Output Capacitance		C_{oss}	--	327	--		
Reverse Transfer Capacitance		C_{rss}	--	200	--		
Internal Drain Inductance	Between lead, 6mm (0.25in.) from package and center of die contact		L_D	--	4.5	--	nH
Internal Source Inductance			L_S	--	7.5	--	
Switching^c							
Turn-On Delay Time	$V_{GS} = 28V, I_D = 62A,$ $V_{DD} = 10V, R_G = 4.5\Omega$	$t_{d(on)}$	--	32.4	--	nS	
Turn-On Rise Time		t_r	--	18.3	--		
Turn-Off Delay Time		$t_{d(off)}$	--	104	--		
Turn-Off Fall Time		t_f	--	18.2	--		
Drain-Source Diode Characteristics and Maximum Rating							
Maximum Continuous Drain-Source Diode Forward Current	MOSFET symbol showing the integral reverse P-N junction diode		I_S	--	--	110	A
Maximum Pulsed Drain-Source Diode Forward Current			I_{SM}	--	--	390	A
Diode Forward Voltage	$I_S = 62A, V_{GS} = 0V$	V_{SD}	--	--	1.3	V	
Reverse Recovery Time	$V_{GS} = 0V, I_S = 62A,$ $di_f/dt = 100A/\mu S$	T_{rr}	--	110	--	nS	
Reverse Recovery Charge		Q_{rr}	--	450	--	μC	

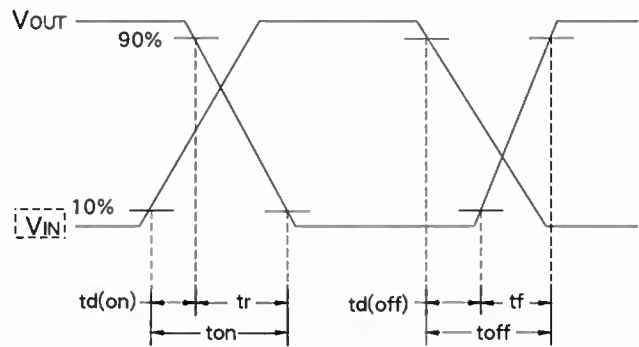
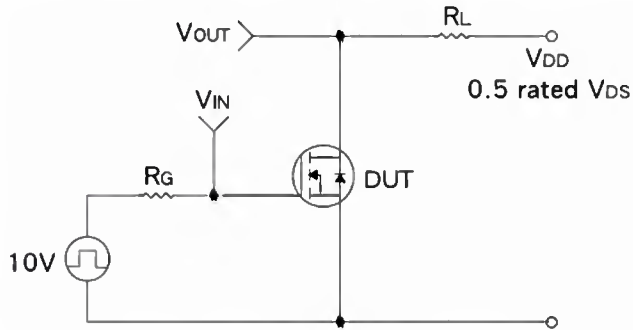
Notes:

1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature
2. Starting $T_J = 25^\circ C, I_{AS} = 62A, L = 138\mu H, R_G = 25\Omega$
3. $I_{SD} \leq 62A, di/dt \leq 207A/\mu S, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ C$
4. Pulse test: pulse width $\leq 400\mu S$, duty cycle $\leq 2\%$
5. Essentially Independent of Operating Temperature
6. For design reference only, not subject to production testing.
7. Switching time is essentially independent of operating temperature.

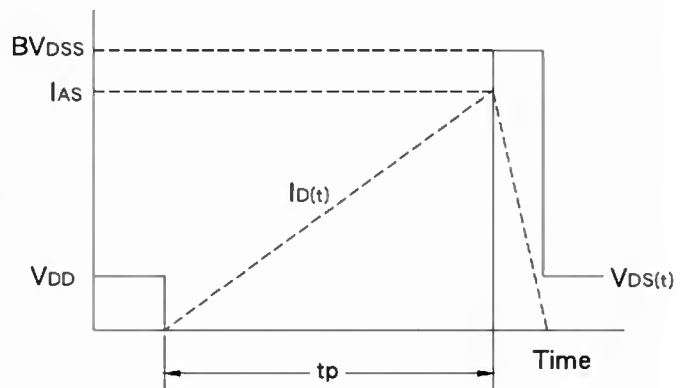
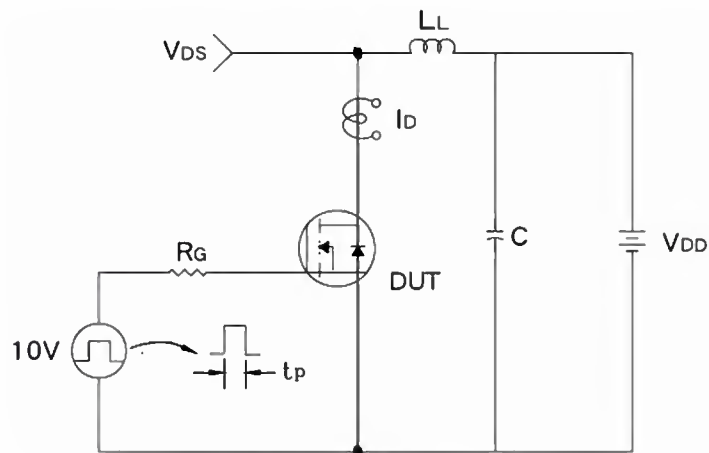
Gate Charge Test Circuit & Waveform



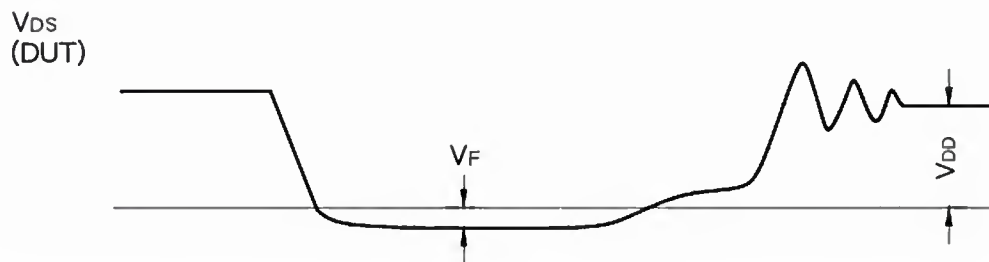
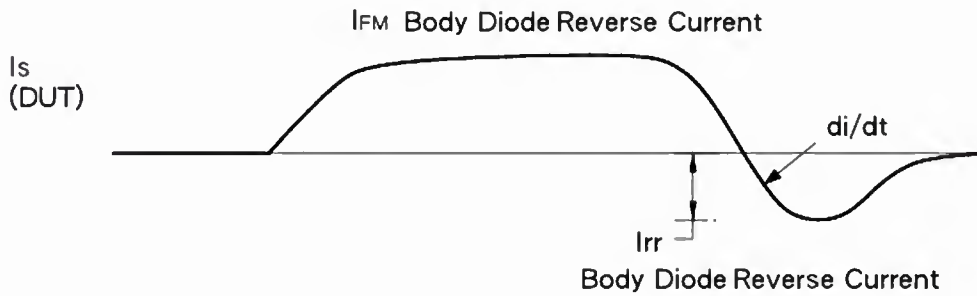
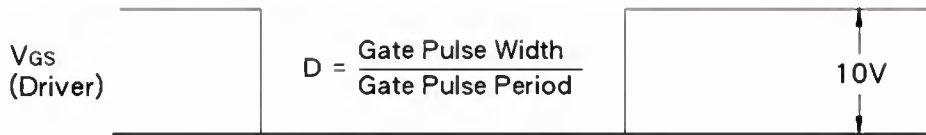
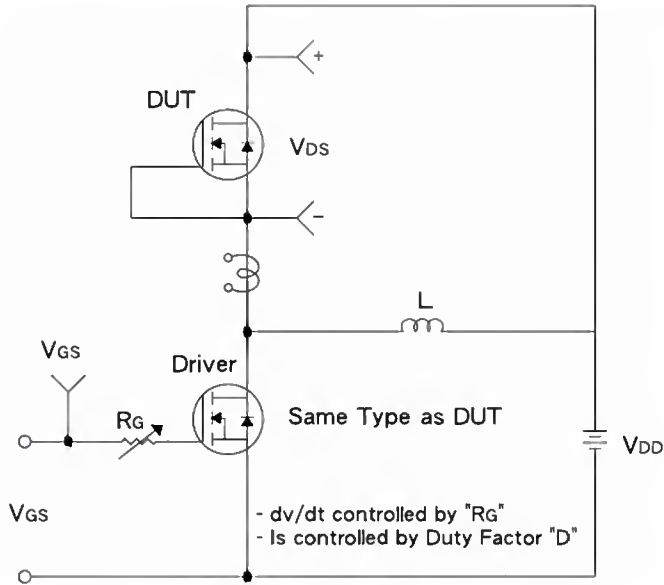
Resistive Switching Test Circuit & Waveform



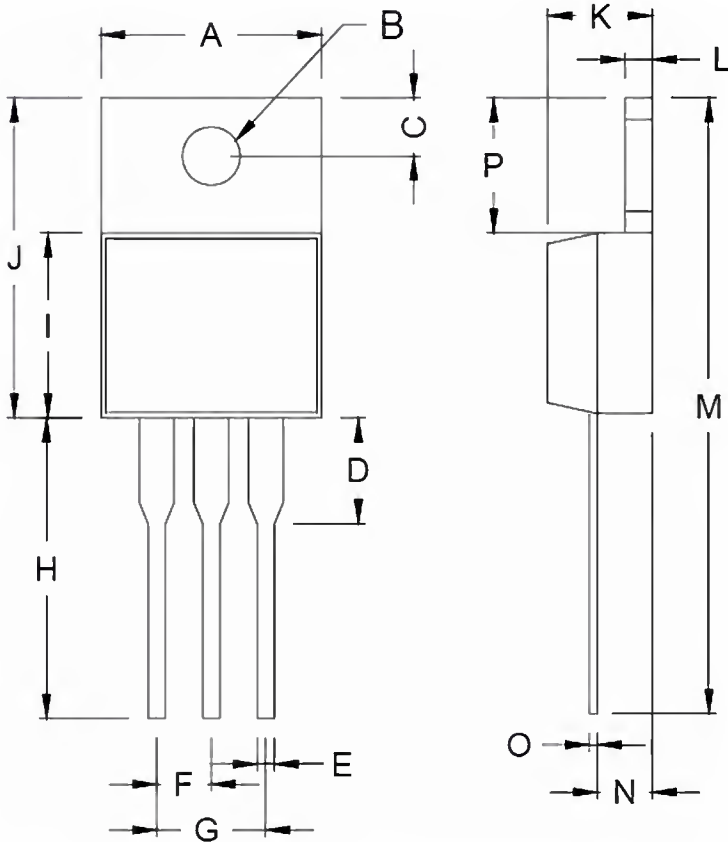
EAS Test Circuit & Waveform



Diode Reverse Recovery Time Test Circuit & Waveform

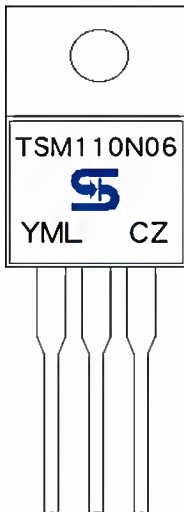


TO-220 Mechanical Drawing



TO-220 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.000	10.500	0.394	0.413
B	3.740	3.910	0.147	0.154
C	2.440	2.940	0.096	0.116
D	-	6.350	-	0.250
E	0.381	1.106	0.015	0.040
F	2.345	2.715	0.092	0.058
G	4.690	5.430	0.092	0.107
H	12.700	14.732	0.500	0.581
J	14.224	16.510	0.560	0.650
K	3.556	4.826	0.140	0.190
L	0.508	1.397	0.020	0.055
M	27.700	29.620	1.060	1.230
N	2.032	2.921	0.080	0.115
O	0.255	0.610	0.010	0.024
P	5.842	6.858	0.230	0.270

Marking Diagram



- Y** = Year Code
- M** = Month Code
(A=Jan, B=Feb, C=Mar, D=Apl, E=May, F=Jun, G=Jul, H=Aug, I=Sep, J=Oct, K=Nov, L=Dec)
- L** = Lot Code

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