REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Make the changes to case outline X in figure 1. Editorial changes throughout. - tvn	99-04-15	Monica L. Poelking

REV																				
SHEET																				
REV	A	A	A	A	A	A														
SHEET	15	16	17	18	19	20														

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Thomas M. Hess	**DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thomas M. Hess	
	APPROVED BY Monica L. Poelking	MICROCIRCUIT, DIGITAL, MULTICHIP MICROCIRCUIT, DUAL MICROPROCESSOR WITH STATIC RAM, SILICON
	DRAWING APPROVAL DATE 97-02-12	
	REVISION LEVEL **A**	SIZE **A** CAGE CODE **67268** **5962-96789** SHEET 1 OF 20

DSCC FORM 2233
APR 97

5962-E210-99

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

5962	-	96789	01	Q	X	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)
_____ Drawing number _____/						

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Memory	Operating frequency	Circuit function
01	320MCM42A	128K	40 MHz	Dual Digital Signal Processor Multichip Module
02	320MCM42A	256K	40 MHz	Dual Digital Signal Processor Multichip Module
03	320MCM42A	128K	50 MHz	Dual Digital Signal Processor Multichip Module
04	320MCM42A	256K	50 MHz	Dual Digital Signal Processor Multichip Module

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	408	Ceramic quad flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	-0.3 V dc to +7.0 V dc 2/
Voltage range on any pin (V_{IN})	-0.3 V dc to +7.0 V dc
Output voltage range (V_{OUT})	-0.3 V dc to +7.0 V dc
Storage temperature range (T_{STG})	-65 C to +150 C
Maximum allowed junction temperature (T_J)	125 C
Maximum solder temperature (10s duration)	260 C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.75 V V_{CC} +5.25 V
High level input voltage range (V_{IH}): 3/	
CLKIN, COMM	+2.6 V V_{IH} V_{CC} + 0.3 V
$\overline{\text{CSTRBx}}$, $\overline{\text{CRDYx}}$, $\overline{\text{CREQx}}$, $\overline{\text{CACKx}}$	+2.2 V V_{IH} V_{CC} + 0.3 V
All other pins	+2.0 V V_{IH} V_{CC} + 0.3 V
Low level input voltage range (V_{IL})	-0.3 V_{IL} 0.8 V 3/
High level output current (I_{OH})	-300 A
Low level output current (I_{OL})	2 mA
Case operating temperature range (T_C)	-55 C to 125 C
Maximum operating free-air temperature (T_J)	+125 C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ All voltage values are with respect to V_{SS}.

3/ Maximum V_{IH} levels and minimum V_{IL} levels are characterized but not tested.

4/ Values will be added when they become available.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 and figure 1 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Boundary scan codes. The boundary scan codes shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number H (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Element evaluation.

4.2.1 Microcircuit dice. Microcircuit dice shall be produced on a QML certified line and probed at wafer level according to the manufacturers QM plan.

4.2.2 Capacitors. Capacitor element evaluation shall be performed according to the manufacturer's QM plan.

4.2.3 Package evaluation. Packages shall be electrically tested by the package manufacturer. Element evaluation shall be performed according to the manufacturer's QM plan.

4.3 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. Constant acceleration shall be in accordance with MIL-PRF-38535 except the peak level shall be at test condition A (5000 g's). External ambient pressure shall not exceed 45 psi during screening.

4.3.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125 C, minimum.

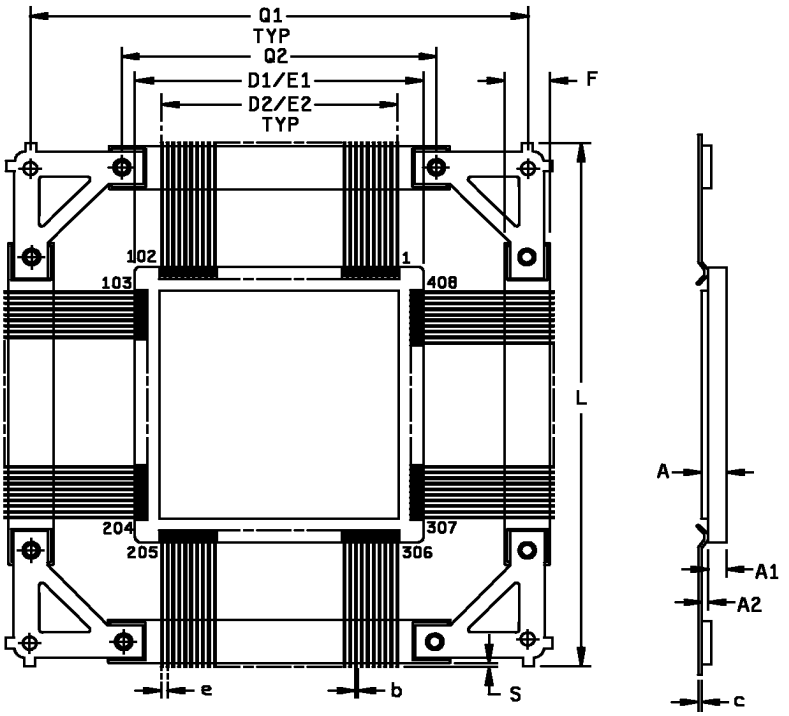
b. Interim and final electrical test parameters shall be as specified in table II herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Test conditions -55 C T_C +125 C +4.75 V V_{CC} +5.25 V unless otherwise specified	Device types	Group A subgroups	Limits		Unit
					Min	Max	
DC Electricals							
High-level output voltage 1/	V_{OH}	V_{CC} = MIN, I_{OH} = MAX	All	1, 2, 3	2.4		V
Low-level output voltage 1/	V_{OL}	V_{CC} = MIN, I_{OL} = MAX	All	1, 2, 3		0.6	V
Three-state current 1/ 2/	I_Z	V_I = V_{SS} to V_{CC}	All	1, 2, 3	-20	20	A
Input current 1/	I_I	V_I = V_{SS} to V_{CC}	All	1, 2, 3	-10	10	A
Input current, COMM signal 1/ 2/ 3/	I_{I2}	V_I = V_{SS} to V_{CC}	All	1, 2, 3	-20	20	A
Input current, internal pullup 1/ 2/ 4/	I_{IPU}	V_I = V_{SS} to V_{CC}	All	1, 2, 3	-400	30	A
Input current, dual internal pullup 1/ 2/ 5/	I_{IP2}	V_I = V_{SS} to V_{CC}	All	1, 2, 3	-800	60	A
Input current, dual internal pulldown 1/ 2/ 6/	I_{IP3}	V_I = V_{SS} to V_{CC}	All	1, 2, 3	-40	800	A
Input current, CLKIN_COMM 1/ 2/	I_{IC}	V_I = V_{SS} to V_{CC}	All	1, 2, 3	-60	60	A
Supply current 1/	I_{CC}	V_{CC} = MAX	01, 03	4		1.1	A
			02, 04			1.5	
Input capacitance	C_I	See 4.5.1c	All	4		7/	pF
Output capacitance	C_O	See 4.5.1c	All	4		7/	pF
Functional testing		See 4.5.1b	All	7, 8			
AC testing		8/	All	9, 10, 11			

1/ These parameters are guaranteed but not tested.
2/ Electrical characteristics are calculated algebraically from SMD 5962-94669 limits.
3/ Includes signals EMU0_COMM, EMU1_COMM, and $\overline{\text{RESET\_COMM}}$.
4/ Applies to TDI_C40_#1.
5/ Includes signals TCK_COMM, TMS_COMM.
6/ Applies to signal $\overline{\text{TRST\_COMM}}$.
7/ An additional 45 pF shall be added to the limits specified in smd 5962-94669 for this parameter limit.
8/ Electrical parameters for the microprocessor die shall be per SMD 5962-94669. Electrical parameters for the SRAM die shall be per 5962-89598 with the following exceptions: I_{CC2} max = 40 mA. Data retention test is not performed on the modules SRAM's. The placement of die into the module will not add more than 1 ns to the propagations delay limits. This limit will be guaranteed, but not tested.

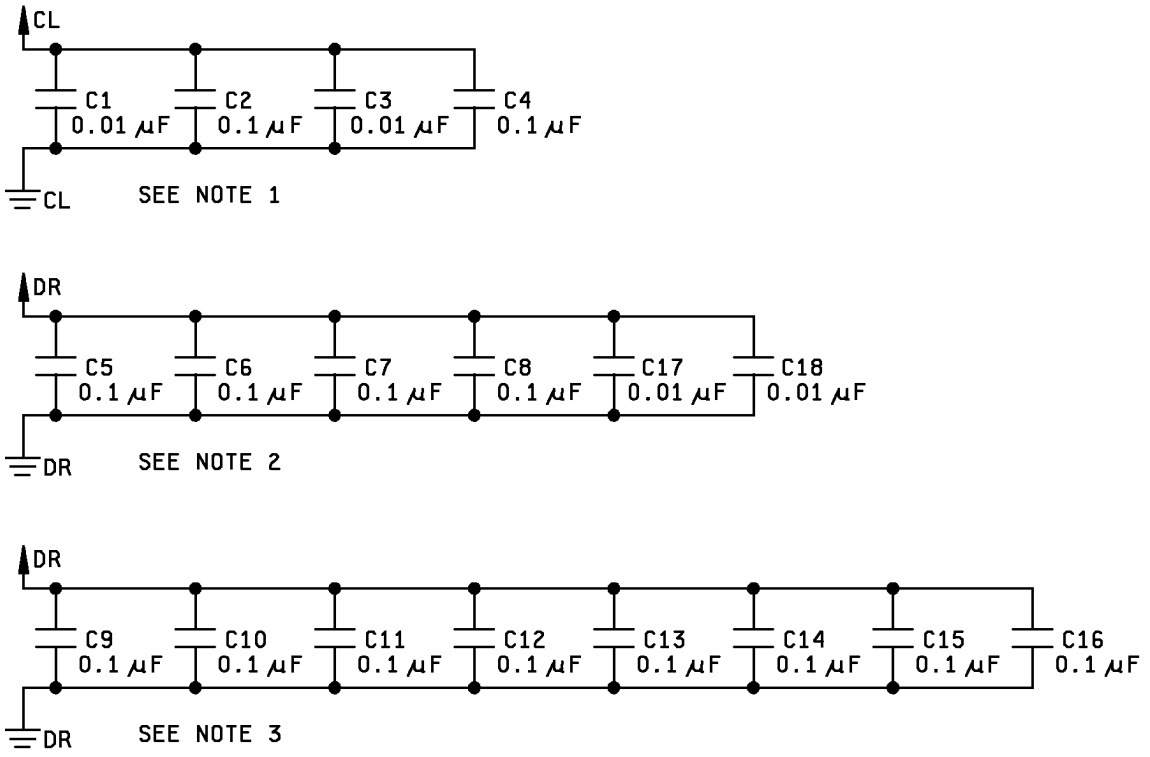
Case outline X



NOTE: The lid is gounded (connected to V_{SS} _DR).

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	3.56	4.45	.140	.175
A1	1.78	2.41	.070	.095
A2	0.15	0.30	.006	.012
b	0.18	0.30	.007	.012
c	0.13	0.23	.005	.009
D1/E1	66.70	67.92	2.626	2.674
D2/E2	64.13 TYP		2.525 TYP	
e	0.65 BSC		.025 BSC	
F	4.45	5.72	.175	.225
L	102.87		4.050	
Q1	97.79 TYP		3.850 TYP	
Q2	71.37	71.73	2.810	2.820
S		0.51		.020

FIGURE 1. Case outline.



NOTES:

1. Capacitors are physically located near the microprocessor die.
2. Capacitors are physically located near the microprocessor die.
3. Capacitors are physically located near the SRAM die.

FIGURE 1. Case outline – Continued.

Case outline X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	ROMEN C40_#1	36	A23_C40_#1	71	D25_C40_#2
2	IIOF0_C40_#1	37	A22_C40_#1	72	D24_C40_#2
3	IIOF1_C40_#1	38	A21_C40_#1	73	D23_C40_#2
4	IIOF2_C40_#1	39	A20_C40_#1	74	D22_C40_#2
5	IIOF3_C40_#1	40	A19_C40_#1	75	D21_C40_#2
6	$\overline{\text{NMI\_C40\_\#1}}$	41	A18_C40_#1	76	D20_C40_#2
7	V_{CC}_DR	42	A17_C40_#1	77	D19_C40_#2
8	V_{SS}_CL	43	V_{CC}_DR	78	D18_C40_#2
9	TCLK0_C40_#1	44	V_{SS}_CL	79	D17_C40_#2
10	TCLK1_C40_#1	45	V_{SS}_DR	80	D16_C40_#2
11	H3_C40_#1	46	A16_C40_#1	81	V_{SS}_CL
12	H1_C40_#1	47	A15_C40_#1	82	V_{SS}_CL
13	V_{SS}_CL	48	A14_C40_#1	83	V_{CC}_DR
14	$\overline{\text{IACK\_C40\_\#1}}$	49	A13_C40_#1	84	V_{SS}_DR
15	CLKIN_COMM	50	A12_C40_#1	85	D15_C40_#2
16	V_{CC}_DR	51	A11_C40_#1	86	D14_C40_#2
17	V_{CC}_CL	52	A10_C40_#1	87	D13_C40_#2
18	V_{CC}_DR	53	A9_C40_#1	88	D12_C40_#2
19	V_{SS}_CL	54	A8_C40_#1	89	D11_C40_#2
20	V_{SS}_DR	55	A7_C40_#1	90	D10_C40_#2
21	V_{CC}_DR	56	A6_C40_#1	91	D9_C40_#2
22	V_{CC}_DR	57	A5_C40_#1	92	D8_C40_#2
23	V_{CC}_CL	58	A4_C40_#1	93	D7_C40_#2
24	V_{SS}_CL	59	V_{CC}_DR	94	D6_C40_#2
25	V_{SS}_DR	60	A3_C40_#1	95	D5_C40_#2
26	V_{SS}_CL	61	A2_C40_#1	96	V_{CC}_DR
27	V_{CC}_DR	62	A1_C40_#1	97	D4_C40_#2
28	A30_C40_#1	63	A0_C40_#1	98	D3_C40_#2
29	A29_C40_#1	64	D31_C40_#2	99	D2_C40_#2
30	A28_C40_#1	65	D30_C40_#2	100	D1_C40_#2
31	V_{CC}_DR	66	D29_C40_#2	101	$\overline{\text{D0\_C40\_\#2}}$
32	A27_C40_#1	67	D28_C40_#2	102	$\overline{\text{CE1\_C40\_\#2}}$
33	A26_C40_#1	68	D27_C40_#2	103	$\overline{\text{RDY1\_C40\_\#2}}$
34	A25_C40_#1	69	D26_C40_#2	104	V_{SS}_DR
35	A24_C40_#1	70	V_{CC}_DR	105	V_{SS}_CL

FIGURE 2. Terminal connections.

Case outline X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
106	$\overline{\text{LOCK\_C40\_\#2}}$	141	$\overline{\text{CREQ4\_C40\_\#2}}$	176	$\overline{\text{CRDY1\_C40\_\#2}}$
107	V_{CC}_CL	142	V_{CC}_DR	177	$\overline{\text{CSTRB1\_C40\_\#2}}$
108	V_{SS}_CL	143	C5D7_C40_#2	178	$\overline{\text{CACK1\_C40\_\#2}}$
109	$\overline{\text{CE0\_C40\_\#2}}$	144	C5D6_C40_#2	179	$\overline{\text{CREQ1\_C40\_\#2}}$
110	$\overline{\text{RDY0\_C40\_\#2}}$	145	C5D5_C40_#2	180	$\overline{\text{CRDY0\_C40\_\#2}}$
111	$\overline{\text{DE\_C40\_\#2}}$	146	C5D4_C40_#2	181	$\overline{\text{CSTRB0\_C40\_\#2}}$
112	TCK_COMM	147	C5D3_C40_#2	182	$\overline{\text{CACK0\_C40\_\#2}}$
113	TDO_C40_#2	148	C5D2_C40_#2	183	$\overline{\text{CREQ0\_C40\_\#2}}$
114	TMS_COMM	149	C5D1_C40_#2	184	V_{SS}_DR
115	$\overline{\text{TRST\_COMM}}$	150	C5D0_C40_#2	185	V_{SS}_CL
116	EMU0_COMM	151	V_{CC}_DR	186	V_{SS}_DR
117	EMU1_COMM	152	C4D7_C40_#2	187	V_{CC}_DR
118	PAGE1_C40_#2	153	C4D6_C40_#2	188	C1D7_C40_#2
119	R/$\overline{\text{W}}$1_C40_#2	154	C4D5_C40_#2	189	C1D6_C40_#2
120	$\overline{\text{STRB1\_C40\_\#2}}$	155	C4D4_C40_#2	190	C1D5_C40_#2
121	STAT0_C40_#2	156	C4D3_C40_#2	191	C1D4_C40_#2
122	STAT1_C40_#2	157	C4D2_C40_#2	192	C1D3_C49_#2
123	V_{SS}_CL	158	C4D1_C40_#2	193	C1D2_C40_#2
124	STAT2_C40_#2	159	C4D0_C40_#2	194	C1D1_C40_#2
125	STAT3_C40_#2	160	V_{CC}_DR	195	C1D0_C40_#2
126	PAGE0_C40_#2	161	V_{CC}_DR	196	V_{CC}_DR
127	R/$\overline{\text{W}}$0_C40_#2	162	V_{SS}_CL	197	C0D7_C40_#2
128	$\overline{\text{STRB0\_C40\_\#2}}$	163	C2D7_C40_#2	198	C0D6_C40_#2
129	$\overline{\text{AE\_C40\_\#2}}$	164	C2D6_C40_#2	199	C0D5_C40_#2
130	RESETLOC1_C40_#2	165	C2D5_C40_#2	200	C0D4_C40_#2
131	V_{CC}_DR	166	C2D4_C40_#2	201	C0D3_C40_#2
132	RESETLOC0_C40_#2	167	C2D3_C40_#2	202	C0D2_C40_#2
133	$\overline{\text{RESET\_COMM}}$	168	C2D2_C40_#2	203	C0D1_C40_#2
134	$\overline{\text{CRDY5\_C40\_\#2}}$	169	C2D1_C40_#2	204	C0D0_C40_#2
135	$\overline{\text{CSTRB5\_C40\_\#2}}$	170	C2D0_C40_#2	205	ROMEN_C40_#2
136	$\overline{\text{CACK5\_C40\_\#2}}$	171	$\overline{\text{CRDY2\_C40\_\#2}}$	206	IIOF0_C40_#2
137	$\overline{\text{CREQ5\_C40\_\#2}}$	172	$\overline{\text{CSTRB2\_C40\_\#2}}$	207	IIOF1_C40_#2
138	$\overline{\text{CRDY4\_C40\_\#2}}$	173	$\overline{\text{CACK2\_C40\_\#2}}$	208	IIOF2_C40_#2
139	$\overline{\text{CSTRB4\_C40\_\#2}}$	174	$\overline{\text{CREQ2\_C40\_\#2}}$	209	IIOF3_C40_#2
140	$\overline{\text{CACK4\_C40\_\#2}}$	175	V_{CC}_DR	210	$\overline{\text{NMI\_C40\_\#2}}$

FIGURE 2. Terminal connections - Continued.

Case outline X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
211	V_{CC}_DR	246	V_{CC}_DR	281	D18_C40_#1
212	V_{SS}_CL	247	V_{SS}_CL	282	D17_C40_#1
213	TCLK0_C40_#2	248	V_{SS}_DR	283	D16_C40_#1
214	TCLK1_C40_#2	249	A16_C40_#2	284	V_{SS}_CL
215	H3_C40_#2	250	A15_C40_#2	285	V_{SS}_CL
216	H1_C40_#2	251	A14_C40_#2	286	V_{CC}_DR
217	V_{SS}_CL	252	A13_C40_#2	287	V_{SS}_DR
218	$\overline{\text{IACK}}$_C40_#2	253	A12_C40_#2	288	D15_C40_#1
219	V_{CC}_DR	254	A11_C40_#2	289	D14_C40_#1
220	V_{CC}_DR	255	A10_C40_#2	290	D13_C40_#1
221	V_{CC}_DR	256	A9_C40_#2	291	D12_C40_#1
222	V_{SS}_CL	257	A8_C40_#2	292	D11_C40_#1
223	V_{SS}_DR	258	A7_C40_#2	293	D10_C40_#1
224	V_{CC}_DR	259	A6_C40_#2	294	D9_C40_#1
225	V_{CC}_DR	260	A5_C40_#2	295	D8_C40_#1
226	V_{CC}_CL	261	A4_C40_#2	296	D7_C40_#1
227	V_{SS}_CL	262	V_{CC}_DR	297	D6_C40_#1
228	V_{SS}_DR	263	A3_C40_#2	298	D5_C40_#1
229	V_{SS}_CL	264	A2_C40_#2	299	V_{CC}_DR
230	V_{CC}_DR	265	A1_C40_#2	300	D4_C40_#1
231	A30_C40_#2	266	A0_C40_32	301	D3_C40_#1
232	A29_C40_#2	267	D31_C40_#1	302	D2_C40_#1
233	A28_C40_#2	268	D30_C40_#1	303	D1_C40_#1
234	V_{CC}_DR	269	D29_C40_#1	304	D0_C40_#1
235	A27_C40_#2	270	D28_C40_#1	305	$\overline{\text{CE1}}$_C40_#1
236	A26_C40_#2	271	D27_C40_#1	306	$\overline{\text{RDY1}}$_C40_#1
237	A25_C40_#2	272	D26_C40_#1	307	V_{SS}_DR
238	A24_C40_#2	273	V_{CC}_DR	308	V_{SS}_CL
239	A23_C40_#2	274	D25_C40_#1	309	$\overline{\text{LOCK}}$_C40_#1
240	A22_C40_#2	275	D24_C40_#1	310	V_{CC}_CL
241	A21_C40_#2	276	D23_C40_#1	311	V_{SS}_CL
242	A20_C40_#2	277	D22_C40_#1	312	$\overline{\text{CE0}}$_C40_#1
243	A19_C40_#2	278	D21_C40_#1	313	$\overline{\text{RDY0}}$_C40_#1
244	A18_C40_#2	279	D20_C40_#1	314	$\overline{\text{DE}}$_C40_#1
245	A17_C40_#2	280	D19_C40_#1	315	TDI_C40_#1

FIGURE 2. Terminal connections - Continued.

Case outline X					
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
316	PAGE1_C40_#1	347	C5D1_C40_#1	378	V_{SS}_DR
317	R/$\overline{W}$ 1_C40_#1	348	C5D0_C40_#1	379	V_{CC}_DR
318	$\overline{\text{STRB1\_C40\_\#1}}$	349	V_{CC}_DR	380	$\overline{\text{CRDY3\_C40\_\#1}}$
319	STAT0_C40_#1	350	C4D7_C40_#1	381	$\overline{\text{CSTRB3\_C40\_\#1}}$
320	STAT1_C40_#1	351	C4D6_C40_#1	382	$\overline{\text{CACK3\_C40\_\#1}}$
321	V_{SS}_CL	352	C4D5_C40_#1	383	$\overline{\text{CREQ3\_C40\_\#1}}$
322	STAT2_C40_#1	353	C4D4_C40_#1	384	V_{CC}_CL
323	STAT3_C40_#1	354	C4D3_C40_#1	385	V_{SS}_CL
324	PAGE0_C40_#1	355	C4D2_C40_#1	386	$\overline{\text{CRDY2\_C40\_\#1}}$
325	R/$\overline{W}$ 0_C40_#1	356	C4D1_C40_#1	387	$\overline{\text{CSTRB2\_C40\_\#1}}$
326	$\overline{\text{STRB0\_C40\_\#1}}$	357	C4D0_ C40_#1	388	$\overline{\text{CACK2\_C40\_\#1}}$
327	$\overline{\text{AE\_C40\_\#1}}$	358	V_{SS}_DR	389	$\overline{\text{CREQ2\_C40\_\#1}}$
328	RESETLOC1_C40_#1	359	V_{CC}_DR	390	V_{CC}_DR
329	V_{CC}_DR	360	C3D7_C40_#1	391	$\overline{\text{CRDY1\_C40\_\#1}}$
330	RESETLOC0_C40_#1	361	C3D6_C40_#1	392	$\overline{\text{CSTRB1\_C40\_\#1}}$
331	$\overline{\text{CRDY5\_C40\_\#1}}$	362	C3D5_C40_#1	393	$\overline{\text{CACK1\_C40\_\#1}}$
332	$\overline{\text{CSTRB5\_C40\_\#1}}$	363	C3D4_C40_#1	394	$\overline{\text{CREQ1\_C40\_\#1}}$
333	$\overline{\text{CACK5\_C40\_\#1}}$	364	C3D3_C40_#1	395	V_{SS}_DR
334	$\overline{\text{CREQ5\_C40\_\#1}}$	365	C3D2_C40_#1	396	V_{SS}_CL
335	$\overline{\text{CRDY4\_C40\_\#1}}$	366	C3D1_C40_#1	397	V_{SS}_DR
336	$\overline{\text{CSTRB4\_C40\_\#1}}$	367	C3D0_C40_#1	398	V_{CC}_DR
337	$\overline{\text{CACK4\_C40\_\#1}}$	368	V_{CC}_DR	399	C1D7_C40_#1
338	$\overline{\text{CREQ4\_C40\_\#1}}$	369	V_{SS}_CL	400	C1D6_C40_#1
339	V_{SS}_DR	370	C2D7_C40_#1	401	C1D5_C40_#1
340	V_{CC}_DR	371	C2D6_C40_#1	402	C1D4_C40_#1
341	C5D7_C40_#1	372	C2D5_C40_#1	403	C1D3_C40_#1
342	C5D6_C40_#1	373	C2D4_C40_#1	404	C1D2_C40_#1
343	C5D5_C40_#1	374	C2D3_C40_#1	405	C1D1_C40_#1
344	C5D4_C40_#1	375	C2D2_C40_#1	406	C1D0_C40_#1
345	C5D3_C40_#1	376	C2D1_C40_#1	407	V_{CC}_DR
346	C5D2_C40_#1	377	C2D0_C40_#1	408	V_{SS}_DR

FIGURE 2. Terminal connections - Continued.

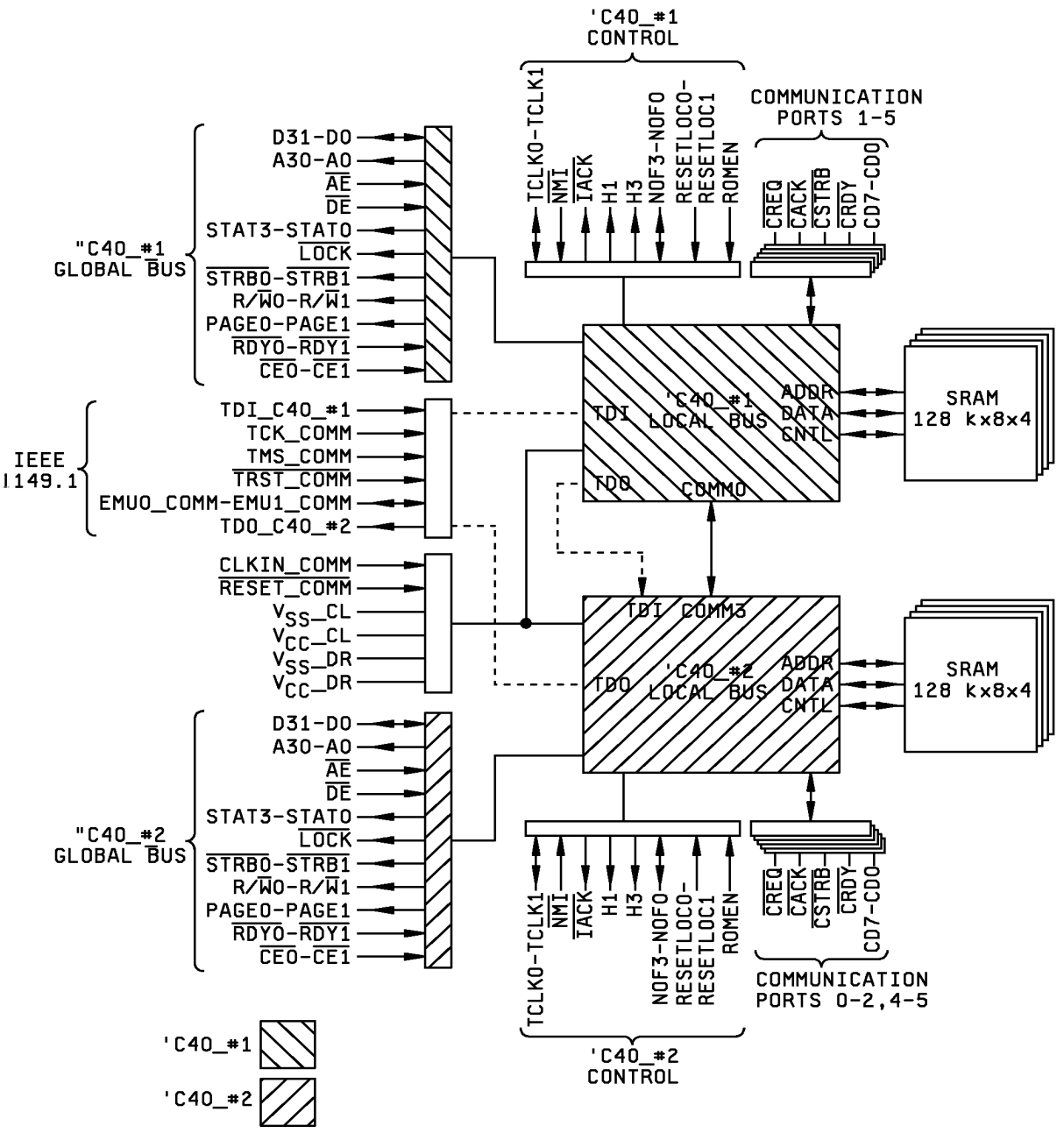
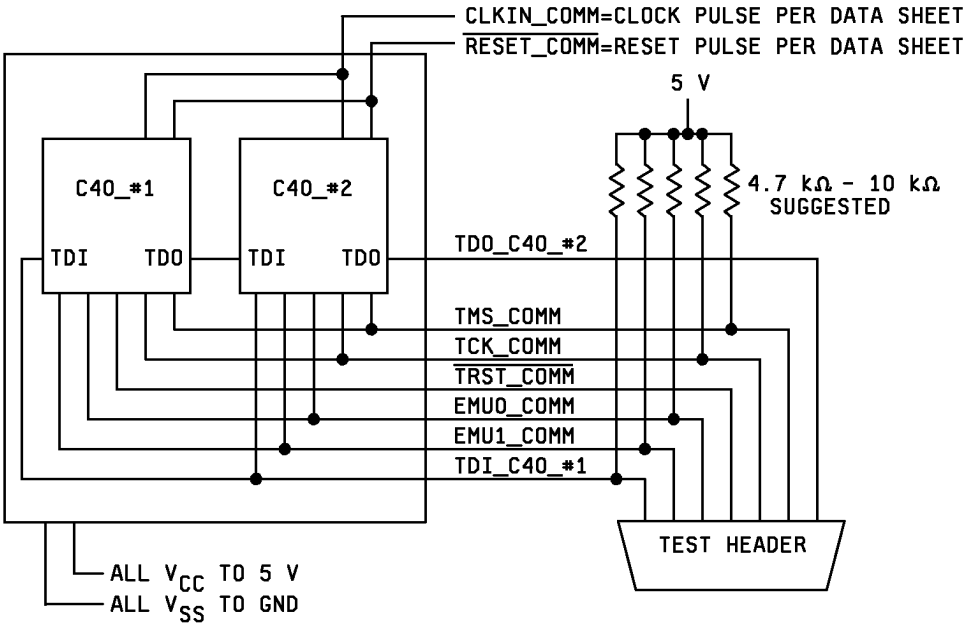


FIGURE 3. Block diagram.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-96789
		REVISION LEVEL A	SHEET 13

DSCC FORM 2234
APR 97



Instruction code	Instruction name
00000000	EXTEST
11111111	BYPASS
00000010	SAMPLE
00000110	HIGHZ
00000011	PRIVATE1
00100000	PRIVATE2
00100001	PRIVATE3
00100010	PRIVATE4
00100011	PRIVATE5
00100100	PRIVATE6
00100101	PRIVATE7
00100110	PRIVATE8
00100111	PRIVATE9
00101000	PRIVATE10
00101001	PRIVATE11

FIGURE 4. Boundary scan instruction codes.

4.3.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.4 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.5.1 through 4.5.4).

4.5 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.5.1 through 4.5.4).

4.5.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_I and C_O measurements) shall be measured only for initial test and after process or design changes which may affect input capacitance. A minimum sample size of 5 devices with zero rejects shall be required

4.5.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.5.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125 C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.5.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.5.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.3)	---	---	1
Final electrical parameters (see 4.3)	1, 2, 3, 4, 7, 8 1/	1, 2, 3, 7, 8 1/	1, 2, 3, 7, 8 2/
Group A test requirements (see 4.5)	1, 2, 3, 4, 7, 8	1, 2, 3, 4, 7, 8	1, 2, 3, 4, 7, 8
Group C end-point electrical parameters (see 4.5)	2, 8A	2, 8A	2, 7, 8
Group D end-point electrical parameters (see 4.5)	2, 8A	2, 8A	2, 7, 8
Group E end-point electrical parameters (see 4.5)	2, 8	2, 8	2, 7, 8

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.5.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25 C 5 C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and table III herein.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

TABLE III. Pin descriptions.

Signal	Pins	Type 1/	Description
Global bus external interface (80 pins)			
D31-D0	32	I/O/Z	32-bit data port of the global external interface
$\overline{DE}$	1	I	Data bus enable signal for the global external interface
A30-A0	31	O/Z	31-bit address port of the global external interface
$\overline{AE}$	1	I	Address bus enable signal for the global bus interface
STAT3-STAT0	4	O	Status signals for the global bus interface
$\overline{LOCK}$	1	O	Lock signal for the global bus interface
$\overline{STRB0}$ 2/	1	O/Z	Access strobe 0 for the global bus interface
R/$\overline{W}$ 0 2/	1	O/Z	Read/write signal for $\overline{STRB0}$ accesses
PAGE0 2/	1	O/Z	Page signal for $\overline{STRB0}$ accesses
$\overline{RDY0}$ 2/	1	I	Ready signal for $\overline{STRB0}$ accesses
$\overline{CE0}$ 2/	1	I	Control enable for the $\overline{STRB0}$, PAGE0, and R/$\overline{W}$ 0 signals
$\overline{STRB1}$ 2/	1	O/Z	Access strobe 1 for the global bus interface
R/$\overline{W}$ 1 2/	1	O/Z	Read/write signal for $\overline{STRB1}$ accesses
PAGE1 2/	1	O/Z	Page signal for $\overline{STRB1}$ accesses
$\overline{RDY1}$ 2/	1	I	Ready signal for $\overline{STRB1}$ accesses
$\overline{CE1}$ 2/	1	I	Control enable for the $\overline{STRB1}$, PAGE1, and R/$\overline{W}$ 1 signals

See footnotes at end of table.

TABLE III. Pin descriptions - Continued.

Signal	Pins	Type 1/	Description
Local bus external interface (80 pins)			
LD31-LD0	32	I/O/Z	32-bit data port of the local external interface
$\overline{\text{LDE}}$	1	I	Data bus enable signal for the local external interface
LA30-LA0	31	O/Z	31-bit address port of the local external interface
$\overline{\text{LAE}}$	1	I	Address bus enable signal for the local bus interface
LSTAT3-LSTAT0	4	O	Status signals for the local bus interface
$\overline{\text{LLOCK}}$	1	O	Lock signal for the local bus interface
$\overline{\text{LSTRB0}}$ 2/	1	O/Z	Access strobe 0 for the local bus interface
LR/$\overline{\text{W}}$ 0	1	O/Z	Read/write signal for $\overline{\text{LSTRB0}}$ accesses
LPAGE0	1	O/Z	Page signal for $\overline{\text{LSTRB0}}$ accesses
$\overline{\text{LRDY0}}$	1	I	Ready signal for $\overline{\text{LSTRB0}}$ accesses
$\overline{\text{LCE0}}$	1	I	Control enable for the $\overline{\text{LSTRB0}}$, LPAGE0, and LR/$\overline{\text{W}}$ 0 signals
$\overline{\text{LSTRB1}}$ 2/	1	O/Z	Access strobe 1 for the local bus interface
LR/$\overline{\text{W}}$ 1	1	O/Z	Read/write signal for $\overline{\text{LSTRB1}}$ accesses
LPAGE1	1	O/Z	Page signal for $\overline{\text{LSTRB1}}$ accesses
$\overline{\text{LRDY1}}$	1	I	Ready signal for $\overline{\text{LSTRB1}}$ accesses
$\overline{\text{LCE1}}$	1	I	Control enable for the $\overline{\text{LSTRB1}}$, LPAGE1, and LR/$\overline{\text{W}}$ 1 signals
Communication port 0 interface (12 pins)			
C0D7-C0D0	8	I/O	Communication port 0 data bus
$\overline{\text{CREQ0}}$	1	I/O	Communication port 0 token request signal
$\overline{\text{CACK0}}$	1	I/O	Communication port 0 token request acknowledge signal
$\overline{\text{CSTRB0}}$	1	I/O	Communication port 0 data strobe signal
$\overline{\text{CRDY0}}$	1	I/O	Communication port 0 data ready signal
Communication port 1 interface (12 Pins)			
C1D7-C1D0	8	I/O	Communication port 1 data bus
$\overline{\text{CREQ1}}$	1	I/O	Communication port 1 token request signal
$\overline{\text{CACK1}}$	1	I/O	Communication port 1 token request acknowledge signal
$\overline{\text{CSTRB1}}$	1	I/O	Communication port 1 data strobe signal
$\overline{\text{CRDY1}}$	1	I/O	Communication port 1 data ready signal

See footnotes at end of table.

TABLE III. Pin descriptions - Continued.

Signal	Pins	Type 1/	Description
Communication port 2 interface (12 Pins)			
C2D7-C2D0	8	I/O	Communication port 2 data bus
$\overline{\text{CREQ2}}$	1	I/O	Communication port 2 token request signal
$\overline{\text{CACK2}}$	1	I/O	Communication port 2 token request acknowledge signal
$\overline{\text{CSTRB2}}$	1	I/O	Communication port 2 data strobe signal
$\overline{\text{CRDY2}}$	1	I/O	Communication port 2 data ready signal
Communication port 3 interface (12 pins)			
C3D7-C3D0	8	I/O	Communication port 3 data bus
$\overline{\text{CREQ3}}$	1	I/O	Communication port 3 token request signal
$\overline{\text{CACK3}}$	1	I/O	Communication port 3 token request acknowledge signal
$\overline{\text{CSTRB3}}$	1	I/O	Communication port 3 data strobe signal
$\overline{\text{CRDY3}}$	1	I/O	Communication port 3 data ready signal
Communication port 4 interface (12 Pins)			
C4D7-C4D0	8	I/O	Communication port 4 data bus
$\overline{\text{CREQ4}}$	1	I/O	Communication port 4 token request signal
$\overline{\text{CACK4}}$	1	I/O	Communication port 4 token request acknowledge signal
$\overline{\text{CSTRB4}}$	1	I/O	Communication port 4 data strobe signal
$\overline{\text{CRDY4}}$	1	I/O	Communication port 4 data ready signal
Communication port 5 interface (12 Pins)			
C5D7-C5D0	8	I/O	Communication port 5 data bus
$\overline{\text{CREQ5}}$	1	I/O	Communication port 5 token request signal
$\overline{\text{CACK5}}$	1	I/O	Communication port 5 token request acknowledge signal
$\overline{\text{CSTRB5}}$	1	I/O	Communication port 5 data strobe signal
$\overline{\text{CRDY5}}$	1	I/O	Communication port 5 data ready signal
Clock (4 Pins)			
X1	1	O	Crystal pin
X2/CLKIN	1	I	Crystal/oscillator pin
H1	1	O	H1 clock
H3	1	O	H3 clock

See footnotes at end of table.

TABLE III. Pin descriptions - Continued.

Signal	Pins	Type 1/	Description
Interrupts, I/O flags, RESET, timer (12 pins)			
IIOF3-IIOF0	4	I/O	Interrupt and I/O flags
$\overline{NMI}$	1	I	Nonmaskable interrupt. It is sensitive to a low-going edge.
$\overline{IACK}$	1	O	Interrupt acknowledge
$\overline{RESET}$	1	I	Reset signal
RESETLOC1 - RESETLOC0	2	I	Reset-vector location pins
ROMEN	1	I	On-chip ROM enable (0 = disable, 1 = enable)
TCLK0	1	I/O	Timer 0 pin
TCLK1	1	I/O	Timer 1 pin
Power (70 pins)			
CV_{SS}	15	I	Ground pins
DV_{SS}	15	I	Ground pins
IV_{SS}	6	I	Ground pins
DV_{DD}	13	I	+5-V DC supply pins
$GADV_{DD}$	3	I	+5-V DC supply pins
$GDDV_{DD}$	3	I	+5-V DC supply pins
$LADV_{DD}$	3	I	+5-V DC supply pins
$LDDV_{DD}$	3	I	+5-V DC supply pins
SUBS	1	I	Substrate pin (tie to ground)
V_{DDL}	4	I	+5-V DC supply pins
V_{SSL}	4	I	Ground pins
Emulation (7 pins)			
TCK	1	I	JTAG test port clock
TDO	1	O/Z	JTAG test port data out
TDI	1	I	JTAG test port data in
TMS	1	I	JTAG test port mode select
TRST	1	I	JTAG test port reset
EMU0	1	I/O	Emulation pin 0
EMU1	1	I/O	Emulation pin 1

1/ I = Input; O = Ouput; Z = High impedance.

2/ $\overline{STRB0}$ and $\overline{STRB1}$ and associated signals (R/$\overline{W}$ 1, R/$\overline{W}$ 0, PAGE0, PAGE1, etc.) are effective over the address ranges defined by the STRB ACTIVE bits.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99-04-15

Approved sources of supply for SMD 5962-96789 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and/or QML-38535 during the next revision. MIL-HDBK-103 and/or QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and/or QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9678901QXC	01295	SMJ320MCM42DHFNM40
5962-9678902QXC	01295	SMJ320MCM42CHFNM40
5962-9678903QXC	01295	SMJ320MCM42DHFNM50
5962-9678904QXC	01295	SMJ320MCM42CHFNM50

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Incorporated 13500 North Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448

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