74ALVCH16373

Low-Voltage 16-Bit Transparent Latch with Bus Hold 1.8/2.5/3.3 V
(3–State, Non–Inverting)

The 74ALVCH16373 is an advanced performance, non–inverting 16–bit transparent latch. It is designed for very high–speed, very low–power operation in 1.8 V, 2.5 V or 3.3 V systems. The VCXH16373 is byte controlled, with each byte functioning identically, but independently. Each byte has separate Output Enable and Latch Enable inputs. These control pins can be tied together for full 16–bit operation.

The 74ALVCH16373 contains 16 D–type latches with 3–state 3.6 V–tolerant outputs. When the Latch Enable (LEn) inputs are HIGH, data on the Dn inputs enters the latches. In this condition, the latches are transparent, (a latch output will change state each time its D input changes). When LE is LOW, the latch stores the information that was present on the D inputs a setup time preceding the HIGH–to–LOW transition of LE. The 3–state outputs are controlled by the Output Enable ($\overline{\text{OEn}}$) inputs. When $\overline{\text{OE}}$ is LOW, the outputs are enabled. When $\overline{\text{OE}}$ is HIGH, the standard outputs are in the high impedance state, but this does not interfere with new data entering into the latches. The data inputs include active bushold circuitry, eliminating the need for external pull–up resistors to hold unused or floating inputs at a valid logic state.

- Designed for Low Voltage Operation: $V_{CC} = 1.65 - 3.6$ V
- 3.6 V Tolerant Inputs and Outputs
- High Speed Operation: 3.0 ns max for 3.0 to 3.6 V
  3.9 ns max for 2.3 to 2.7 V
  6.8 ns max for 1.65 to 1.95 V
- Static Drive: ±24 mA Drive at 3.0 V
  ±18 mA Drive at 2.3 V
  ±6 mA Drive at 1.65 V
- Supports Live Insertion and Withdrawal
- Includes Active Bushold to Hold Unused or Floating Inputs at a Valid Logic State
- I_{OFF} Specification Guarantees High Impedance When $V_{CC} = 0$ V†
- Near Zero Static Supply Current in All Three Logic States (20 μA) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds ±250 mA @ 125°C
- ESD Performance: Human Body Model >2000 V;
  Machine Model >200 V
- Second Source to Industry Standard 74ALVCH16373

†To ensure the outputs activate in the 3–state condition, the output enable pins should be connected to V_{CC} through a pull–up resistor. The value of the resistor is determined by the current sinking capability of the output connected to the $\overline{\text{OE}}$ pin.

MARKING DIAGRAM

TSSOP–48
DT SUFFIX
CASE 1201

48

74ALVCH16373DT
AWLYYWW

1
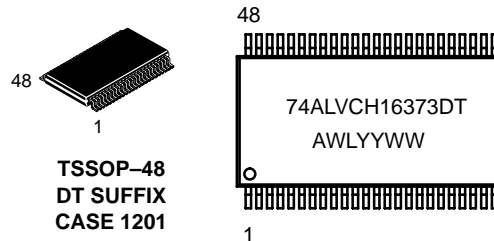
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

PIN NAMES

Pins	Function
$\overline{\text{OEn}}$	Output Enable Inputs
LEn	Latch Enable Inputs
D0–D15	Inputs
O0–O15	Outputs

ORDERING INFORMATION

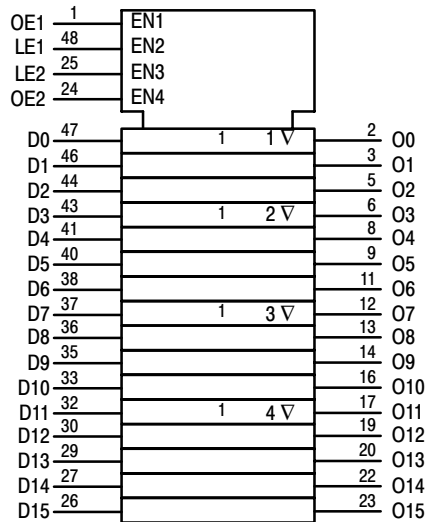| Device	Package	Shipping
74ALVCH16373DT	TSSOP	39 Units/Rail
74ALVCH16373DTR	TSSOP	2500/Tape & Reel

74ALVCH16373
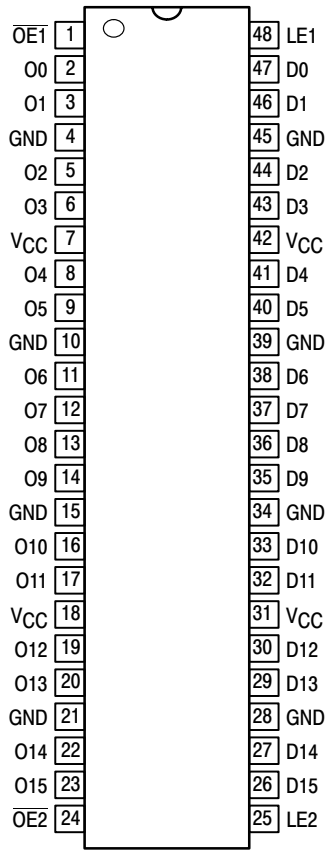
Figure 1. 48–Lead Pinout
(Top View)
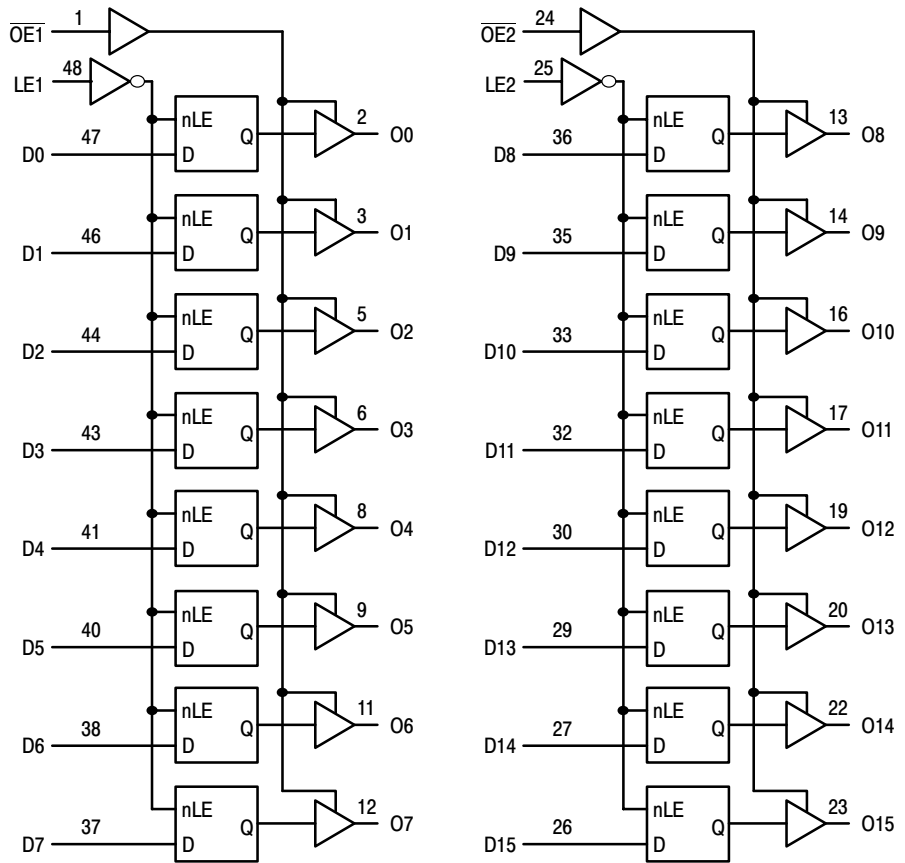
Figure 2. Logic Diagram

Figure 3. IEC Logic Diagram

Inputs			Outputs	Inputs			Outputs
LE1	$\overline{OE1}$	D0:7	O0:7	LE2	$\overline{OE2}$	D8:15	O8:15
X	H	X	Z	X	H	X	Z
H	L	L	L	H	L	L	L
H	L	H	H	H	L	H	H
L	L	X	O0	L	L	X	O0

H = High Voltage Level; L = Low Voltage Level; Z = High Impedance State; X = High or Low Voltage Level and Transitions Are Acceptable, for I_{CC} reasons, DO NOT FLOAT Inputs. O0 = No Change.

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MAXIMUM RATINGS (Note 1)

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		-0.5 to $+4.6$	V
V_I	DC Input Voltage		-0.5 to $+4.6$	V
V_O	DC Output Voltage		-0.5 to $+4.6$	V
I_{IK}	DC Input Diode Current	$V_I < GND$	-50	mA
I_{OK}	DC Output Diode Current	$V_O < GND$	-50	mA
I_O	DC Output Sink Current		± 50	mA
I_{CC}	DC Supply Current per Supply Pin		± 100	mA
I_{GND}	DC Ground Current per Ground Pin		± 100	mA
T_{STG}	Storage Temperature Range		-65 to $+150$	$^\circ$C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	$^\circ$C
T_J	Junction Temperature Under Bias		$+150$	$^\circ$C
θ_{JA}	Thermal Resistance (Note 2)		90	$^\circ$C/W
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 30% – 35%	UL–94–VO (0.125 in)	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	>2000 >200 N/A	V
$I_{LATCH-UP}$	Latch–Up Performance	Above V_{CC} and Below GND at 85°C (Note 6)	± 250	mA

Maximum Ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum–rated conditions is not implied. Functional operation should be restricted to the Recommended Operating Conditions.
1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm–by–1 inch, 2–ounce copper trace with no air flow.
3. Tested to EIA/JESD22–A114–A.
4. Tested to EIA/JESD22–A115–A.
5. Tested to JESD22–C101–A.
6. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	Operating Data Retention Only	2.3 1.5	3.6 3.6	V
V_I	Input Voltage	(Note 7)	0	3.6	V
V_O	Output Voltage	(HIGH or LOW State)	0	3.6	V
T_A	Operating Free–Air Temperature		-40	$+85$	$^\circ$C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate	$V_{CC} = 2.5$ V $\pm$ 0.2 V $V_{CC} = 3.0$ V $\pm$ 0.3 V $V_{CC} = 5.0$ V $\pm$ 0.5 V	0 0 0	20 10 5	ns/V

7. Unused inputs may not be left open. All inputs must be tied to a high–logic voltage level or a low–logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	$T_A = -40°C$ to $+85°C$ Min	Max	Unit
V_{IH}	HIGH Level Input Voltage (Note 8)	1.65 V $\leq$ V_{CC} < 2.3 V	0.65 × V_{CC}		V
		2.3 V $\leq$ V_{CC} $\leq$ 2.7 V	1.7		
		2.7 V < V_{CC} $\leq$ 3.6 V	2.0		
V_{IL}	LOW Level Input Voltage (Note 8)	1.65 V $\leq$ V_{CC} < 2.3 V		0.35 × V_{CC}	V
		2.3 V $\leq$ V_{CC} $\leq$ 2.7 V		0.7	
		2.7 V < V_{CC} $\leq$ 3.6 V		0.8	
V_{OH}	HIGH Level Output Voltage	1.65 V $\leq$ V_{CC} $\leq$ 3.6 V; I_{OH} = −100 μA	V_{CC} − 0.2		V
		V_{CC} = 1.65 V; I_{OH} = −4 mA	1.20		
		V_{CC} = 2.3 V; I_{OH} = −6 mA	2.0		
		V_{CC} = 2.3 V; I_{OH} = −12 mA	1.7		
		V_{CC} = 2.7 V; I_{OH} = −12 mA	2.2		
		V_{CC} = 3.0 V; I_{OH} = −12 mA	2.4		
		V_{CC} = 3.0 V; I_{OH} = −24 mA	2.0		
V_{OL}	LOW Level Output Voltage	1.65 V $\leq$ V_{CC} $\leq$ 3.6 V; I_{OL} = 100 μA		0.2	V
		V_{CC} = 1.65 V; I_{OL} = 4 mA		0.45	
		V_{CC} = 2.3 V; I_{OL} = 6 mA		0.4	
		V_{CC} = 2.3 V; I_{OL} = 12 mA		0.7	
		V_{CC} = 2.7 V; I_{OL} = 12 mA		0.4	
		V_{CC} = 3.0 V; I_{OL} = 24 mA		0.55	
V_{OL}	LOW Level Output Voltage	V_{CC} = 3.6 V; V_I = 0 to 3.6 V		±500	μA
I_I	Input Leakage Current	1.65 V $\leq$ V_{CC} $\leq$ 3.6 V; 0 V $\leq$ V_I $\leq$ 3.6 V		±5.0	μA
$I_{I(HOLD)}$	Minimum Bus–hold Input Current	V_{CC} = 3.0 V, V_{IN} = 0.8 V	75		μA
		V_{CC} = 3.0 V, V_{IN} = 2.0 V	−75		
		V_{CC} = 2.3 V, V_{IN} = 0.7 V	45		
		V_{CC} = 2.3 V, V_{IN} = 1.7 V	−45		
		V_{CC} = 1.65 V, V_{IN} = 0.58 V	25		
		V_{CC} = 1.65 V, V_{IN} = 1.07 V	−25		
I_{OZ}	3–State Output Current	1.65 V $\leq$ V_{CC} $\leq$ 3.6 V; 0 V $\leq$ V_O $\leq$ 3.6 V; V_I = V_{IH} or V_{IL}		±10	μA
I_{OFF}	Power–Off Leakage Current	V_{CC} = 0 V; V_I or V_O = 3.6 V		10	μA
I_{CC}	Quiescent Supply Current (Note 9)	1.65 V $\leq$ V_{CC} $\leq$ 3.6 V; V_I = GND or V_{CC}		40	μA
		1.65 V $\leq$ V_{CC} $\leq$ 3.6 V; 3.6 V $\leq$ V_I, V_O $\leq$ 3.6 V		±40	
ΔI_{CC}	Increase in I_{CC} per Input	2.7 V < V_{CC} $\leq$ 3.6 V; V_{IH} = V_{CC} − 0.6 V		750	μA

8. These values of V_I are used to test DC electrical characteristics only.
9. Outputs disabled or 3–state only.

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AC CHARACTERISTICS (Note 10; $t_R = t_F = 2.0$ ns; $C_L = 30$ pF; $R_L = 500\ \Omega$)

Symbol	Parameter	Waveform	Limits						Unit
			$T_A = -40°C$ to $+85°C$						
			$V_{CC} = 3.0$ V t o 3.6 V		$V_{CC} = 2.3$ V to 2.7 V		$V_{CC} = 1.65$ V to 1.95 V		
			Min	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Dn to On	1	0.5 0.5	3.0 3.0	0.5 0.5	3.4 3.4	0.5 0.5	6.8 6.8	ns
t_{PLH} t_{PHL}	Propagation Delay LE to On	1	0.5 0.5	3.0 3.0	0.5 0.5	3.9 3.9	0.5 0.5	7.8 7.8	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	2	0.5 0.5	3.5 3.5	0.5 0.5	4.6 4.6	0.5 0.5	9.2 9.2	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	2	0.5 0.5	3.5 3.5	0.5 0.5	3.8 3.8	0.5 0.5	6.8 6.8	ns
t_S	Setup Time, High or Low Dn to LE	3	1.5		1.5		2.5		ns
t_h	Hold Time, High or Low Dn to LE	3	1.0		1.0		1.0		ns
t_W	LE Pulse Width, High	3	1.5		1.5		4.0		ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 11)			0.5 0.5		0.5 0.5		0.75 0.75	ns

10. For $C_L = 50$ pF, add approximately 300 ps to the AC maximum specification.
11. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Unit
C_{IN}	Input Capacitance	Note 12	6	pF
C_{OUT}	Output Capacitance	Note 12	7	pF
C_{PD}	Power Dissipation Capacitance	Note 12, 10 MHz	20	pF

12. $V_{CC} = 1.8$, 2.5 or 3.3 V; $V_I = 0V$ or V_{CC}.
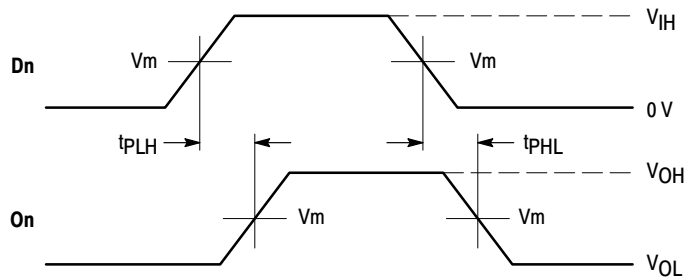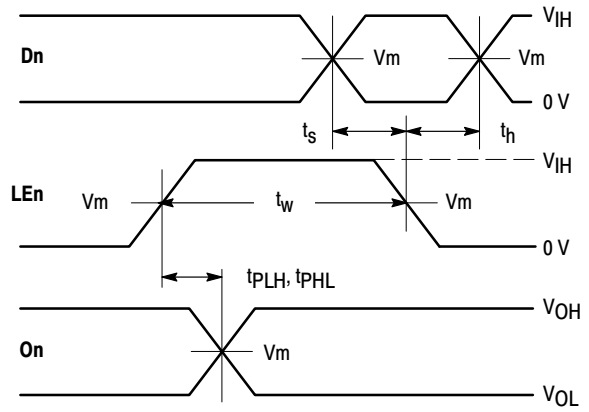

WAVEFORM 1 – PROPAGATION DELAYS
$t_R = t_F = 2.0$ ns, 10% to 90%; f = 1MHz; $t_W = 500$ ns
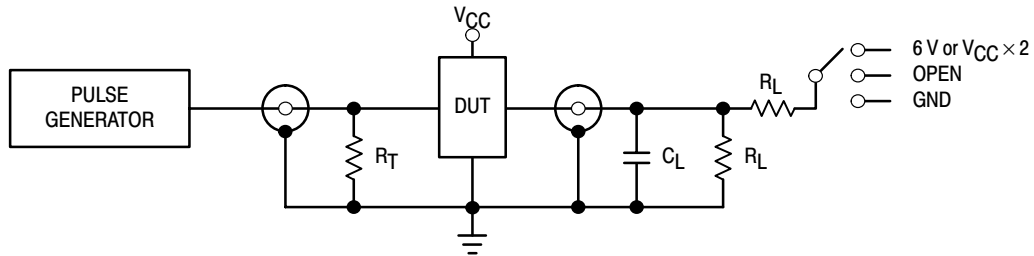
Figure 4. AC Waveforms

74ALVCH16373
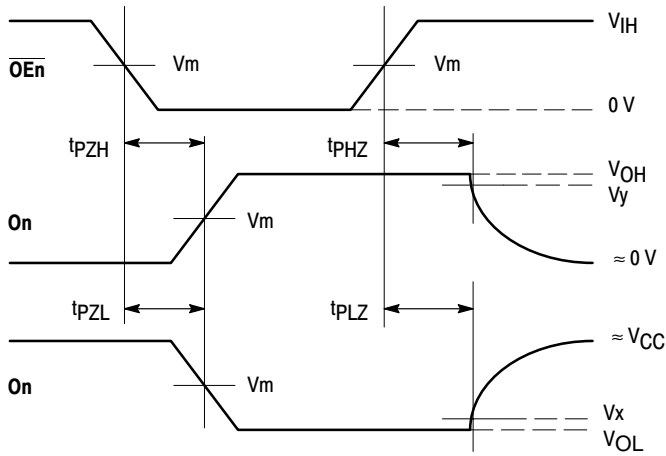
WAVEFORM 2 – OUTPUT ENABLE AND DISABLE TIMES
$t_R = t_F = 2.0$ ns, 10% to 90%; f = 1 MHz; $t_W = 500$ ns

WAVEFORM 3 – LE to On PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn to LE SETUP AND HOLD TIMES
$t_R = t_F = 2.0$ ns, 10% to 90%; f = 1 MHz; $t_W = 500$ ns except when noted

Figure 5. AC Waveforms

Symbol	V_{CC}		
	3.3 V $\pm$0.3 V	**2.5 V $\pm$0.2 V**	**1.8 V $\pm$0.15 V**
V_{IH}	2.7 V	V_{CC}	V_{CC}
V_m	1.5 V	$V_{CC}/2$	$V_{CC}/2$
V_x	$V_{OL} + 0.3$ V	$V_{OL} + 0.15$ V	$V_{OL} + 0.15$ V
V_y	$V_{OH} - 0.3$ V	$V_{OH} - 0.15$ V	$V_{OH} - 0.15$ V

| TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6 V at $V_{CC} = 3.3 \pm0.3$ V; $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm0.2$ V; 1.8 V ±0.15 V
t_{PZH}, t_{PHZ}	GND

$C_L = 50$ pF for $V_{CC} = 3.0 \pm 0.3$ V
$R_L = 500 \ \Omega$ or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50 Ω)

Figure 6. Test Circuit

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AC CHARACTERISTICS (t_R = t_F = 2.0 ns; C_L = 50 pF; R_L = 500 Ω)

Symbol	Parameter	Waveform	Limits				Unit
			T_A = −40°C to +85°C				
			V_{CC} = 3.0 V to 3.6 V		V_{CC} = 2.7 V		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay Dn to On	4	1.0 1.0	3.6 3.6		4.3 4.3	ns
t_{PLH} t_{PHL}	Propagation Delay LE to On	4	1.0 1.0	3.9 3.9		4.6 4.6	ns
t_{PZH} t_{PZL}	Output Enable Time to High and Low Level	5	1.0 1.0	4.7 4.7		5.7 5.7	ns
t_{PHZ} t_{PLZ}	Output Disable Time From High and Low Level	5	1.0 1.0	4.1 4.1		4.5 4.5	ns
t_{OSHL} t_{OSLH}	Output–to–Output Skew (Note 13)			0.5 0.5		0.5 0.5	ns

13. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW (t_{OSHL}) or LOW–to–HIGH (t_{OSLH}); parameter guaranteed by design.

TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6 V at V_{CC} = 3.3 ±0.3 V; V_{CC}× 2 at V_{CC} = 2.5 ±0.2 V; 1.8 V ±0.15 V
t_{PZH}, t_{PHZ}	GND

C_L = 50 pF or equivalent (Includes jig and probe capacitance)
R_L = 500 Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50 Ω)

Figure 7. Test Circuit

74ALVCH16373
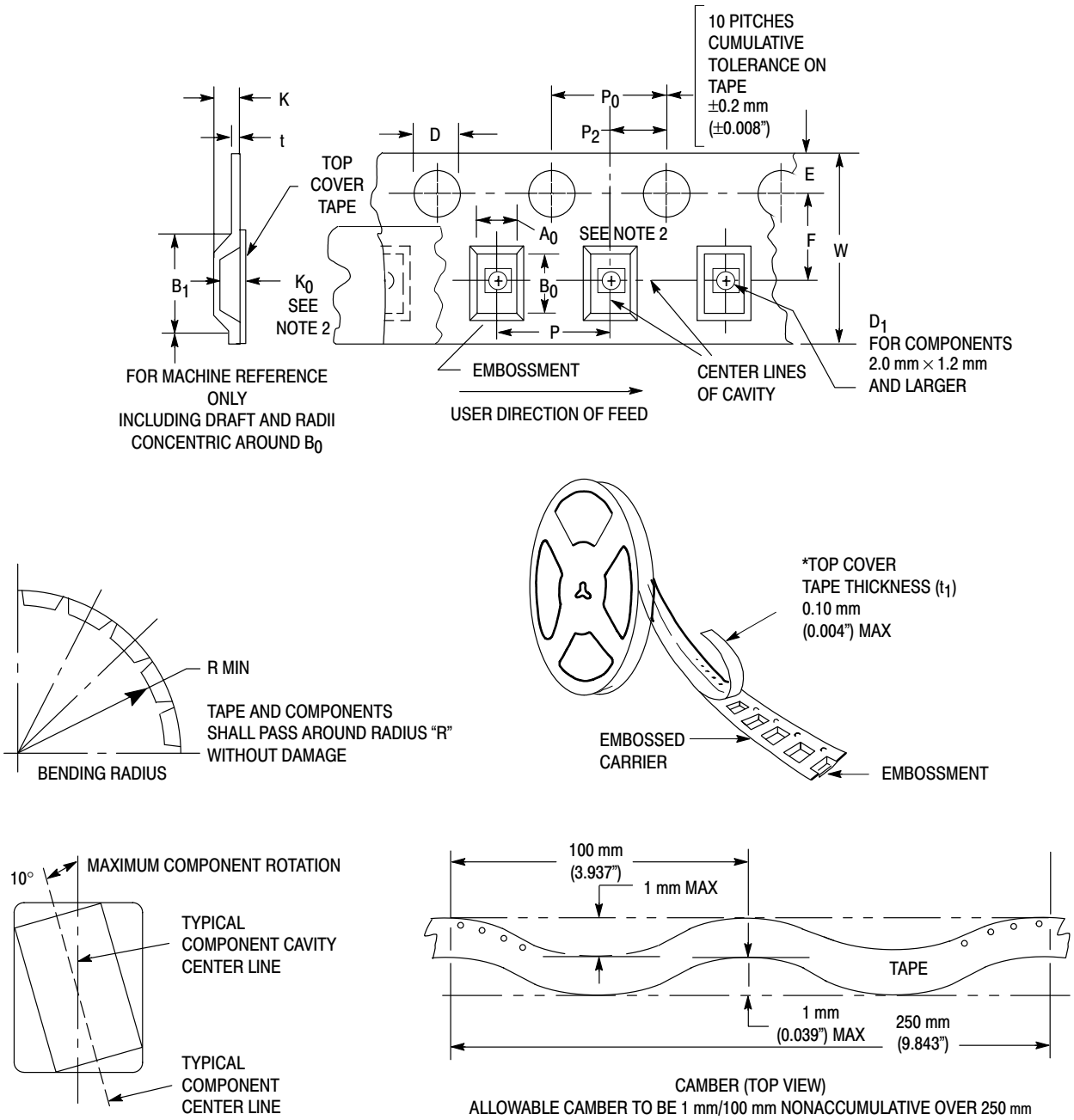
Figure 8. Carrier Tape Specifications

EMBOSSED CARRIER DIMENSIONS (See Notes 14 and 15)

Tape Size	B$_1$ Max	D	D$_1$	E	F	K	P	P$_0$	P$_2$	R	T	W
24mm	20.1mm (0.791")	1.5 + 0.1mm −0.0 (0.059 +0.004" −0.0)	1.5mm Min (0.060")	1.75 ±0.1 mm (0.069 ±0.004")	11.5 ±0.10 mm (0.453 ±0.004")	11.9 mm Max (0.468")	16.0 ±0.1 mm (0.63 ±0.004")	4.0 ±0.1 mm (0.157 ±0.004")	2.0 ±0.1 mm (0.079 ±0.004")	30 mm (1.18")	0.6 mm (0.024")	24.3 mm (0.957")

14. Metric Dimensions Govern–English are in parentheses for reference only.

15. A$_0$, B$_0$, and K$_0$ are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity.
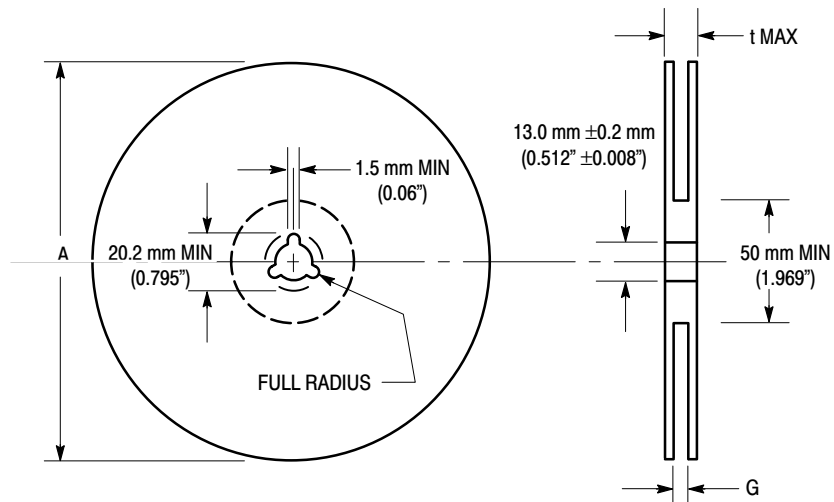
Figure 9. Reel Dimensions

REEL DIMENSIONS

Tape Size	A Max	G	t Max
24 mm	360 mm (14.173")	24.4 mm + 2.0 mm, −0.0 (0.961" + 0.078", −0.00)	30.4 mm (1.197")
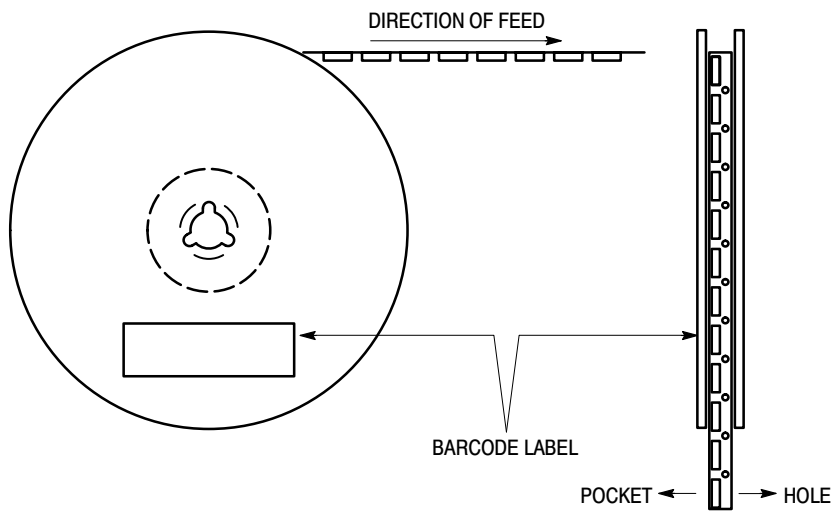
Figure 10. Reel Winding Direction

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TAPE TRAILER
(Connected to Reel Hub)
NO COMPONENTS
160 mm MIN

COMPONENTS

TAPE LEADER
NO COMPONENTS
400 mm MIN

CAVITY
TAPE

TOP TAPE

DIRECTION OF FEED
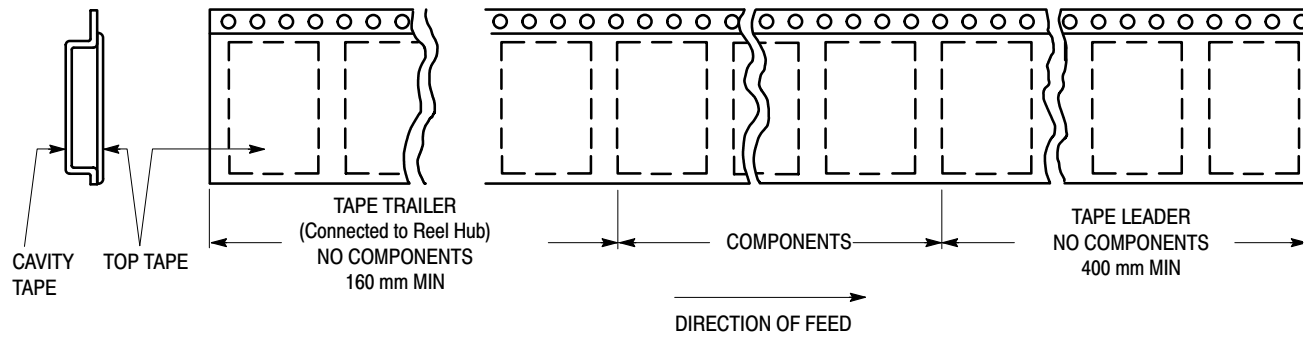
Figure 11. Tape Ends for Finished Goods

User Direction of Feed
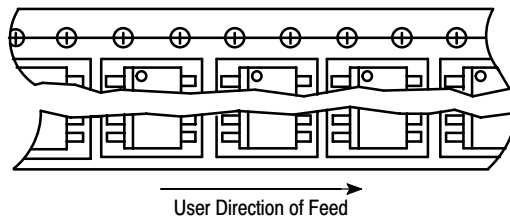
Figure 12. Reel Configuration

K

F

L

48 Leads

G
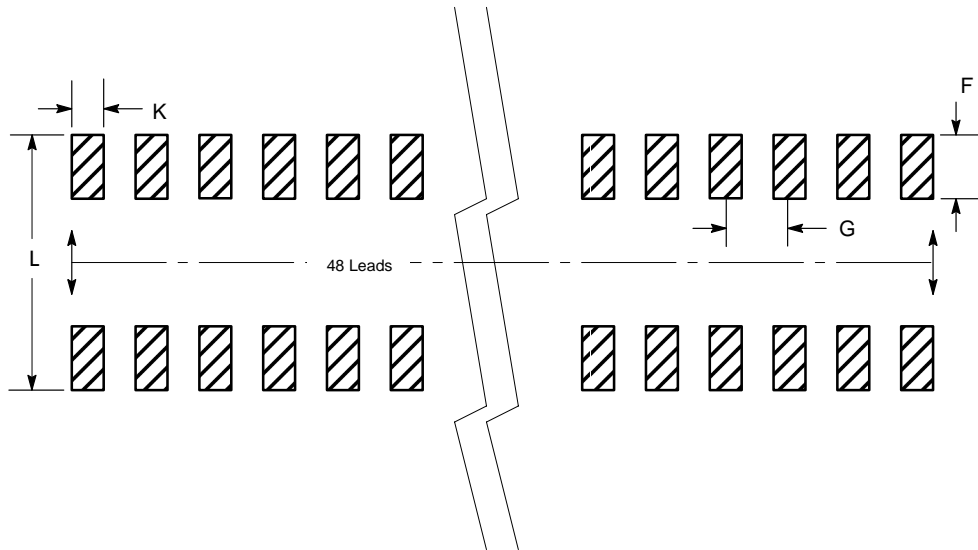
Figure 13. Package Footprint

PACKAGE DIMENSIONS

TSSOP
DT SUFFIX
CASE 1201–01
ISSUE A
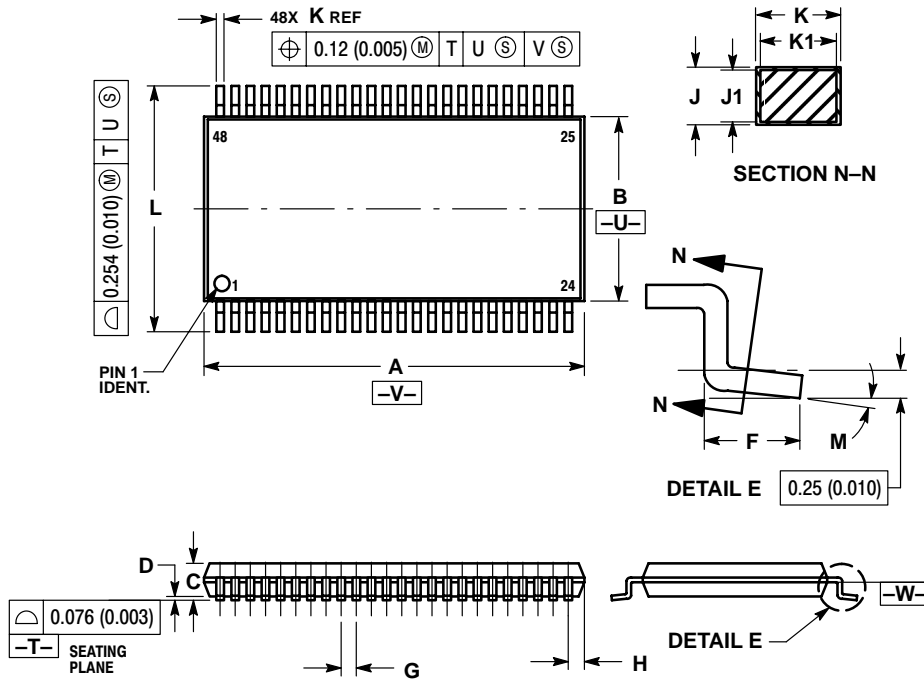
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.40	12.60	0.488	0.496
B	6.00	6.20	0.236	0.244
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.50 BSC		0.0197 BSC	
H	0.37	---	0.015	---
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.17	0.27	0.007	0.011
K1	0.17	0.23	0.007	0.009
L	7.95	8.25	0.313	0.325
M	0 °	8 °	0 °	8 °

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