



UTD351

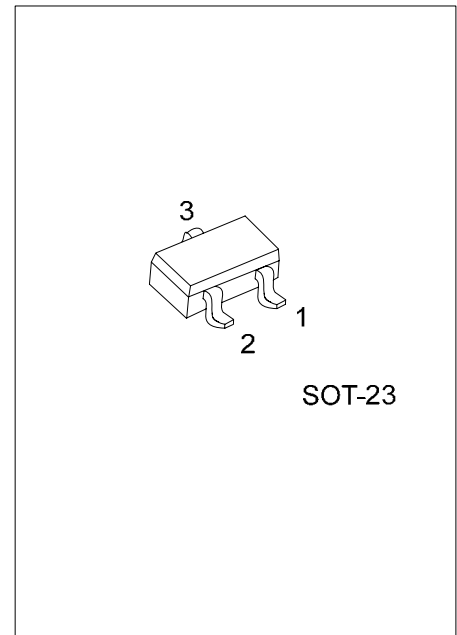
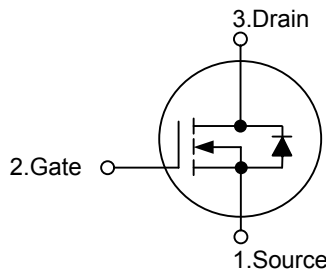
Power MOSFET

N-CHANNEL ENHANCEMENT MODE

■ DESCRIPTION

As N-Channel Logic Level MOSFET, **UTD351** has been optimized for battery power management applications. And it's produced using UTC's Trench process.

■ SYMBOL



SOT-23

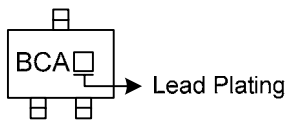
*Pb-free plating product number: UTD351L

■ ORDERING INFORMATION

Ordering Number		Package	Pin Assignment			Packing
Normal	Lead Free Plating		1	2	3	
UTD351-AE3-R	UTD351L-AE3-R	SOT-23	S	G	D	Tape Reel

<p>UTD351L-AE3-R</p> <p>(1)Packing Type</p> <p>(2)Package Type</p> <p>(3)Lead Plating</p>	<p>(1) R: Tape Reel</p> <p>(2) AE3: SOT-23</p> <p>(3) L: Lead Free Plating, Blank: Pb/Sn</p>
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■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_A = 25$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DSS}	30	V
Gate-Source Voltage	V_{GSS}	± 20	
Continuous Drain Current (Note 3)	I_D	1.4	A
Pulsed Drain Current	I_{DM}	10	
Power Dissipation	P_D	0.5	W
Junction Temperature	T_J	+150	$^{\circ}C$
Storage Temperature	T_{STG}	-55 ~ +150	$^{\circ}C$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL DATA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Junction-to-Ambient (Note 3)	θ_{JA}		250		$^{\circ}C/W$
Junction-to-Case	θ_{JC}		75		$^{\circ}C/W$

■ ELECTRICAL CHARACTERISTICS ($T_A = 25^{\circ}C$, unless otherwise specified)

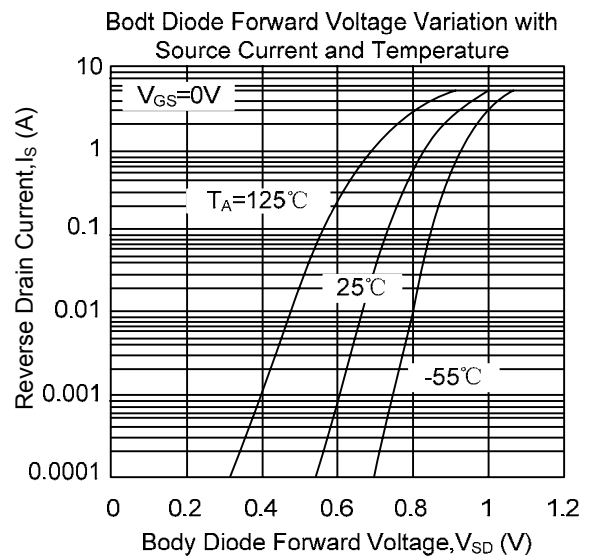
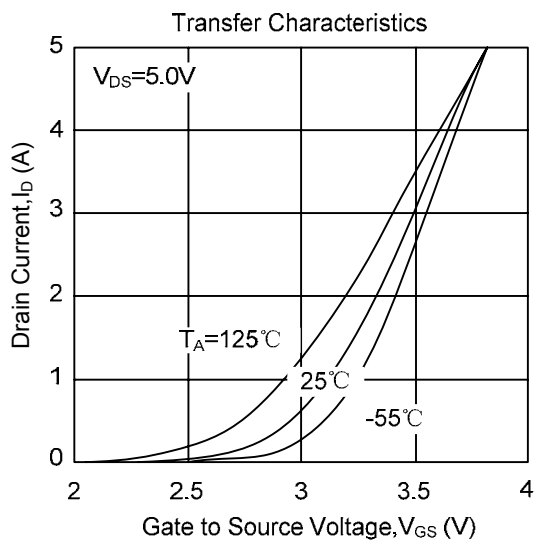
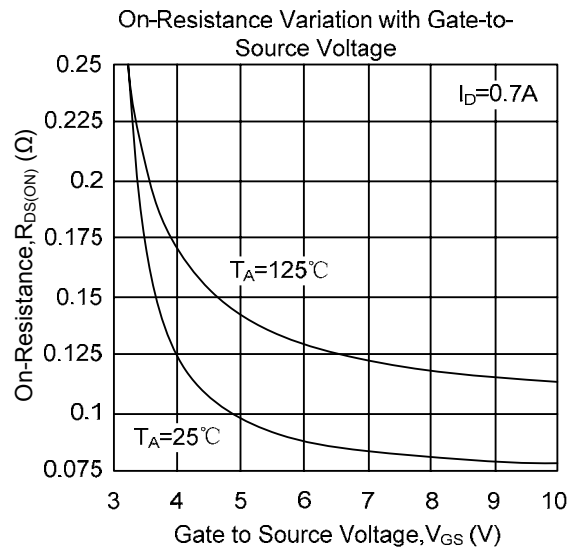
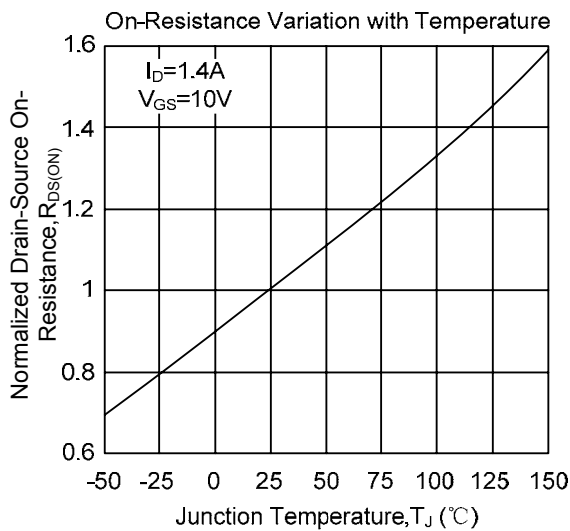
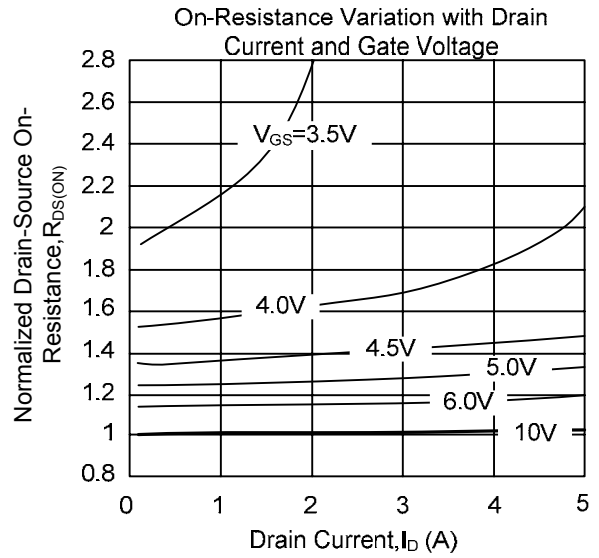
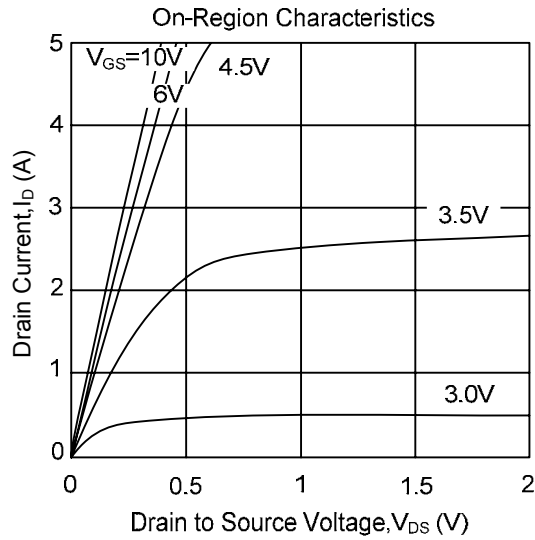
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0 V, I_D = 250 \mu A$	30			V
Drain-Source Leakage Current	I_{DSS}	$V_{DS} = 24 V, V_{GS} = 0 V$			1	μA
Gate-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20 V, V_{DS} = 0 V$			± 100	nA
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	$I_D = 250 \mu A$, Referenced to $25^{\circ}C$		26		mV/
ON CHARACTERISTICS (Note2)						
Gate-Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.8	2.1	3	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	$V_{GS} = 10 V, I_D = 1.4 A$		92	160	m Ω
		$V_{GS} = 4.5 V, I_D = 1.2 A$		120	250	
DYNAMIC PARAMETERS						
Input Capacitance	C_{ISS}	$V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz$		145		pF
Output Capacitance	C_{OSS}			35		
Reverse Transfer Capacitance	C_{RSS}			15		
SWITCHING PARAMETERS (Note2)						
Turn-ON Delay Time	$t_{D(ON)}$	$V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V,$ $R_{GEN} = 6 \Omega$		3	6	ns
Turn-ON Rise Time	t_R			8	16	
Turn-OFF Delay Time	$t_{D(OFF)}$			16	29	
Turn-OFF Fall-Time	t_F			2	4	
Total Gate Charge	Q_G	$V_{DS} = 15 V, V_{GS} = 4.5 V, I_D = 1.4 A$		1.3	1.8	nC
Gate-Source Charge	Q_{GS}			0.5		
Gate-Drain Charge	Q_{GD}			0.5		
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Continuous Drain-Source Diode Forward Current	I_S				0.42	A
Drain-Source Diode Forward Voltage	V_{SD}	$V_{GS} = 0 V, I_S = 0.42 A$ (Note 2)		0.8	1.2	V
Reverse Recovery Time	t_{RR}	$I_F = 1.4 A, dI_F/dt = 100 A/\mu s$		11		ns
Reverse Recovery Charge	Q_{RR}				4	

Notes: 1. Pulse width limited by $T_{J(MAX)}$

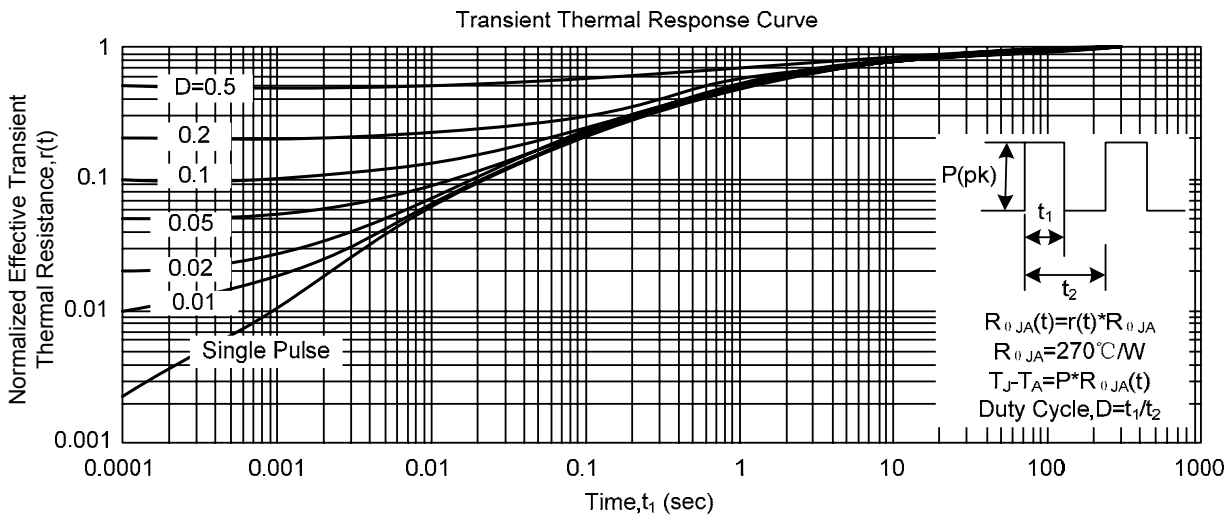
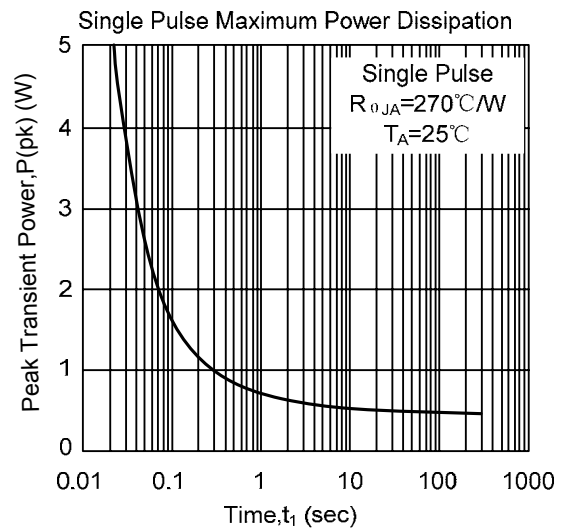
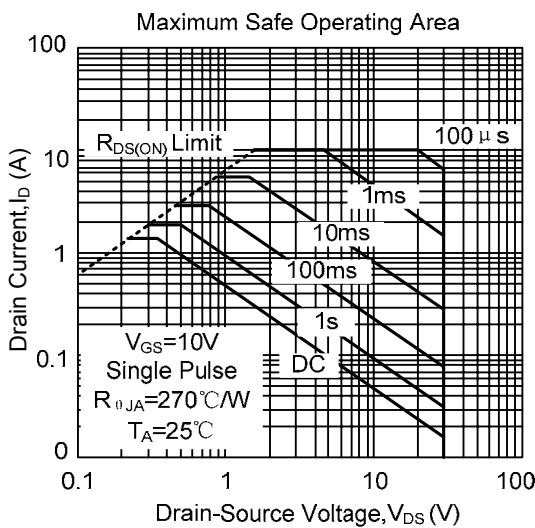
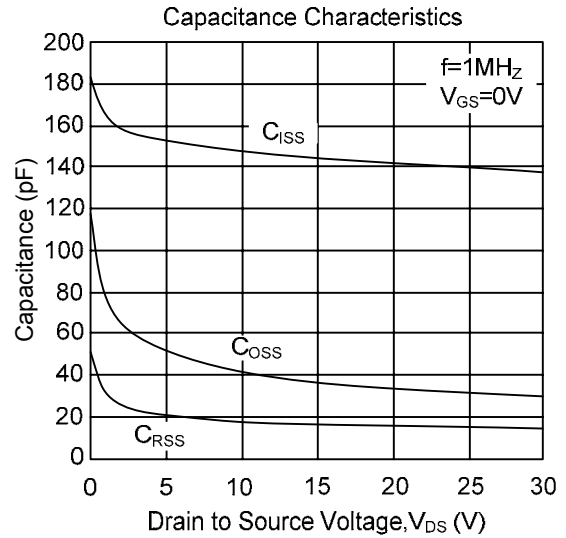
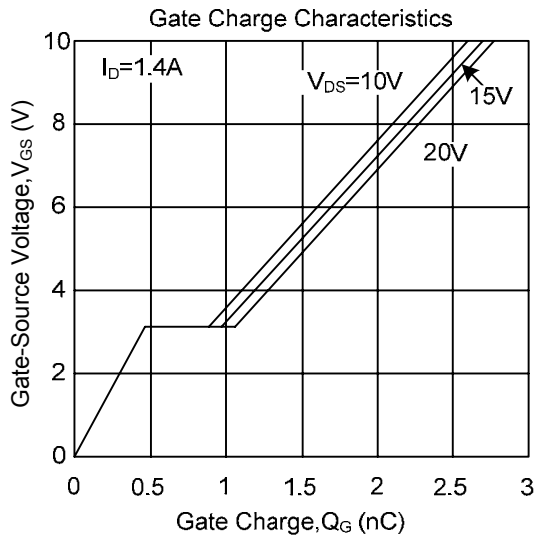
2. Pulse width $\leq 300 \mu s$, duty cycle $\leq 2\%$.

3. Surface mounted on 1 in^2 copper pad of FR4 board; 250 /W when mounted on min.

TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS(Cont.)



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