Video Genlock PLL

General Description

The **AV9173** provides the analog circuit blocks required for implementing a video genlock dot (pixel) clock generator. It contains a phase detector, charge pump, loop filter, and voltage-controlled oscillator (VCO). By grouping these critical analog blocks into one IC and utilizing external digital functions, performance and design flexibility are optimized as are development time and system cost.

When used with an external clock divider, the **AV9173** forms a Phase-Locked Loop configured as a frequency synthesizer. The **AV9173** is designed to accept video horizontal synchronization (h-sync) pulses and produce a video dot clock. A separated, negative-going sync input reference pulse is required at pin2 (IN).

The **AV9173** is also suited for other clock recovery applications in such areas as data communications.

Features

- Phase-detector/VCO circuit block
- Ideal for genlock system
- Reference clock range 25 kHz to 1 MHz
- Output clock range 1.25 to 50 MHz
- On-chip loop filter
- Single 5 volt power supply
- Low power CMOS technology
- Small 8-pin DIP or SOP package

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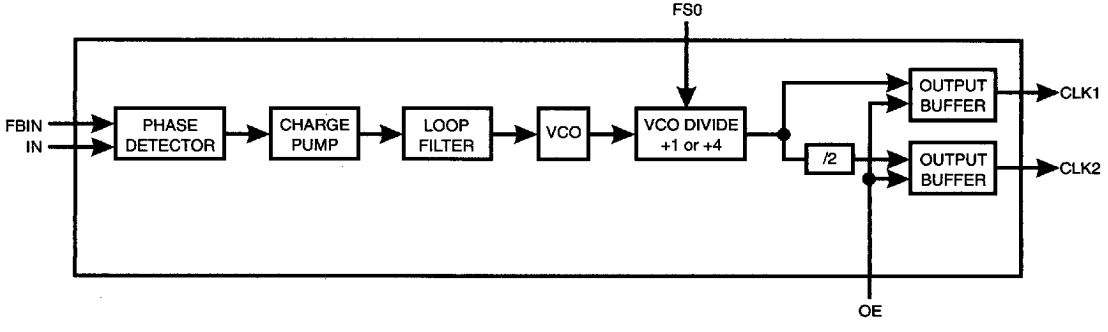
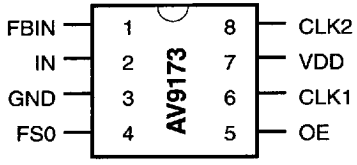
Block Diagram



Pin Configuration



8-Pin DIP or SOP
K-3, K-6

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	FBIN	Input	Feedback Input
2	IN	Input	Input for reference sync pulse
3	GND	-	Ground
4	FS0	Input	Frequency Select 0 input
5	OE	Input	Output Enable
6	CLK1	Output	Clock output 1
7	VDD	-	Power supply (+5V)
8	CLK2	Output	Clock output 2 (Divided-by-2 from Clock 1)

Using the AV9173

Most video sources, such as video cameras, are asynchronous, free-running devices. To digitize video or synchronize one video source to another free-running reference video source, a video "genlock" (generator lock) circuit is required. The **AV9173** integrates the analog blocks which make the task much easier.

In the complete video genlock circuit, the primary function of the **AV9173** is to provide the analog circuitry required to generate the video dot clock within a PLL. This application is illustrated in Figure 1. The input reference signal for this circuit is the horizontal synchronization (h-sync) signal. If a composite video reference source is being used, the h-sync pulses must be separated from the composite signal. A video sync separator circuit, such as the national Semiconductor LM1881, can be used for this purpose.

The clock feedback divider shown in Figure 1 is a digital divider used within the PLL to multiply the reference frequency. Its divide ratio establishes how many video dot clock cycles occur per h-sync pulse. For example, if 880 pixel clocks are desired per h-sync pulse, then the divider ratio is set to 880. Hence, together the h-sync frequency and external divider ratio establish the dot clock frequency:

$f_{OUT} = f_{IN} \bullet N$ where N is external divide ratio

Both **AV9173** input pins IN and FBIN respond only to negative-going clock edges of the input signal. The h-sync signal must be constant frequency in the 25 kHz to 1 MHz range and stable (low clock jitter) for creation of a stable output clock.

The output hook-up of the **AV9173** is dictated by the desired dot clock frequency. The primary consideration is the internal VCO which operates over a frequency range of 10 MHz to 50 MHz. Because of the selectable VCO output divider and the additional divider on output CLK2, four distinct output frequency ranges can be achieved. The following table lists these ranges and the corresponding device configuration.

FS0 State	Output Used	Frequency Range
0	CLK1	10 - 50 MHz
0	CLK2	5 - 25 MHz
1	CLK1	2.5 - 12.5 MHz
1	CLK2	1.25 - 6.25 MHz

Note that both outputs, CLK1 nd CLK2, are available during operation even though only one is fed back via the external clock divider.

Pin 5, OE, tristates both CLK1 and CLK2 upon logic low input. This feature can be used to revert dot clock control to the system clock when not in genlock mode (hence, when in genlock mode the system dot clock must be tristated).

When unused, inputs FS0 and OE must be tied to either GND (logic low) or VDD (logic high).

For further discussion of VCO/PLL operation as it applies to the **AV9173**, please refer to the AV9170 application note. The AV9170 is a similar device with fixed feedback dividers for skew control applications.

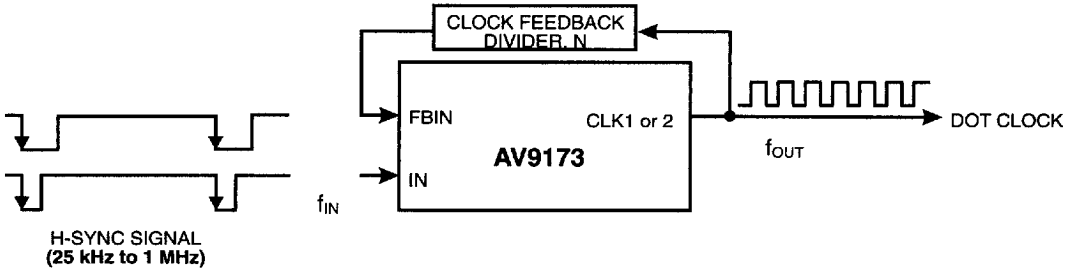


Figure 1: Typical Application of AV9173 in a Video Genlock System

Absolute Maximum Ratings

VDD referenced to GND 7V
Operating temperature under bias ..... 0°C to +70°C
Storage temperature ..... -65°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation ..... 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics

V_{DD} =+5V± 5%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	V_{DD}=5V	-	-	0.8	V
Input High Voltage	V_{IH}	V_{DD}=5V	2.0	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-5	-	-	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5	-	5	µA
Output Low Voltage	V_{OL}	I_{OL}=8mA	-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-1mA, V_{DD}=5.0V	V_{DD}-.4V	-	-	V
Output High Voltage	V_{OH}	I_{OH}=-4mA, V_{DD}=5.0V	V_{DD}-.8V	-	-	V
Output High Voltage	V_{OH}	I_{OH}=-8mA	2.4	-	-	V
Supply Current	I_{DD}	Unloaded, 50 MHz	-	20	50	mA
AC Characteristics						
Input Clock Rise Time	$ICLK_r$	Note 1	-	-	10	ns
Input Clock Fall Time	$ICLK_f$	Note 1	-	-	10	ns
Output Rise Time, 0.8 to 2.0V	t_r	15 pf load	-	1	2	ns
Rise time, 20% to 80%V_{DD}	t_r	15 pf load	-	2	4	ns
Output Fall time, 2.0 to 0.8V	t_f	15 pf load	-	1	2	ns
Fall time, 80% to 20% V_{DD}	t_f	15 pf load	-	2	4	ns
Output Duty Cycle	d_t	15 pf load. Note 1	40	48/52	60	%
Cycle-to-cycle jitter, 1 sigma	T_{1s}		-	120	300	ps
Cycle-to-cycle jitter, absolute	T_{abs}		-500	±250	500	ps
Line-to-line jitter, absolute	TL_{abs}	Note 2		-±4	-	ns
Input Frequency, IN or FBIN	f_i		25	-	1000	kHz
VCO clock speed	f_{VCO}		10	-	50	MHz

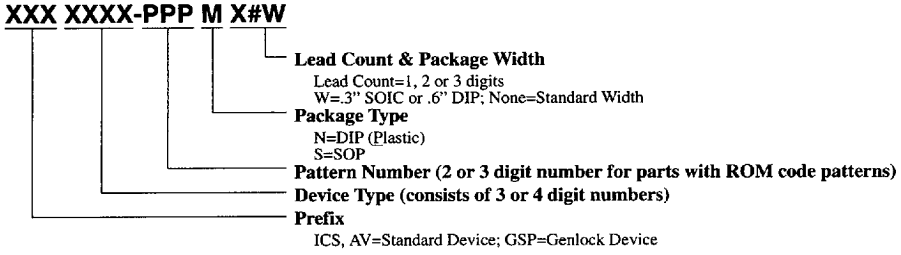
NOTES:

1. Duty cycle measured at 1.4V.
2. Input Reference Frequency = 25 kHz, Output Frequency = 25 MHz.

Ordering Information

AV9173-01N8 or AV9173-01S8

Example:



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