Multiple Power Supply Tracking Controller with Power Good Timeout

FEATURES

- **Flexible Power Supply Tracking Up and Down**
- **Power Supply Sequencing**
- **Supply Stability Is Not Affected**
- **Controls Three Supplies Without Series FETs**
- **Controls an Optional Fourth Supply with a Series FET**
- **Electronic Circuit Breaker**
- **Remote Sense Switch Compensates for Voltage Drop Across a Series FET**
- Supply Shutdown Outputs
- $\overline{\text{FAULT}}$ Output
- Adjustable Power Good Timeout
- Available in Narrow 24-Lead SSOP and Tiny 24-Lead QFN Packages

APPLICATIONS

- V_{CORE} and $V_{I/O}$ Supply Tracking
- Microprocessor, DSP and FPGA Supplies
- Servers
- Communication Systems

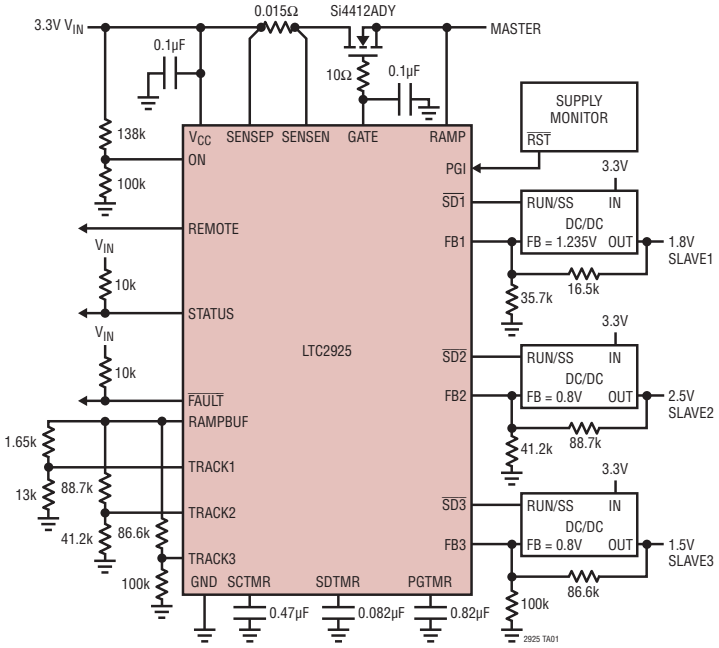
DESCRIPTION

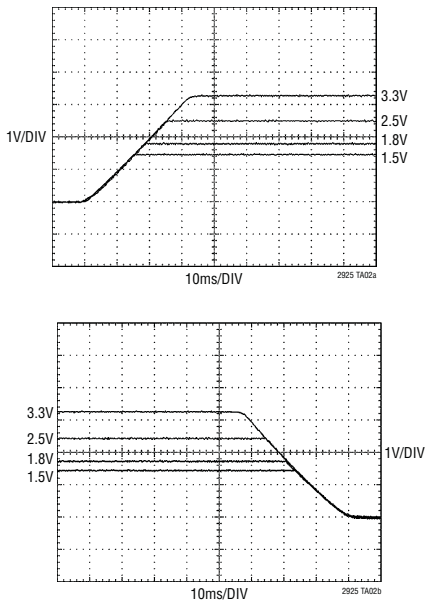
The LTC®2925 provides a simple solution to power supply tracking and sequencing requirements. By selecting a few resistors, the supplies can be configured to ramp-up and ramp-down together or with voltage offsets, time delays or different ramp rates.

The LTC2925 controls the outputs of three independent supplies without inserting any pass element losses. For systems that require a fourth supply, or when a supply does not allow direct access to its feedback resistors, one supply can be controlled with a series FET. When the FET is used, an internal remote sense switch compensates for the voltage drop across the FET and current sense resistor, and an electronic circuit breaker provides protection from short-circuit conditions.

The LTC2925 also includes a power good timeout feature that turns off the supplies if an external supply monitor fails to indicate that the supplies have entered regulation within an adjustable timeout period.

TYPICAL APPLICATION

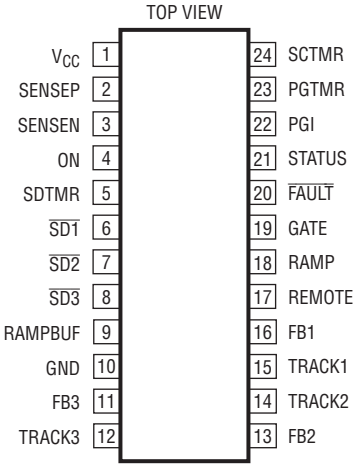




ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

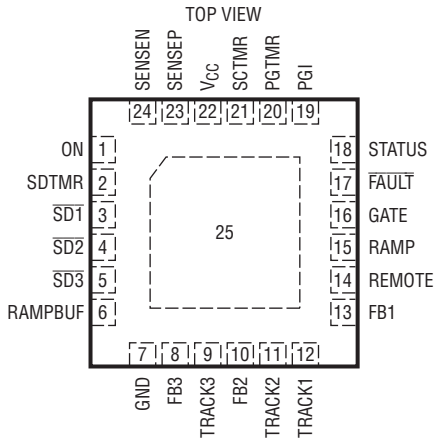
Supply Voltage (V_{CC}) ..... –0.3V to 10V
Input Voltages
ON, PGI, SENSEP, SENSEN ..... –0.3V to 10V
TRACK1, TRACK2, TRACK3 ..... –0.3V to V_{CC} + 0.3V
SCTMR, SDTMR, PGTMR ..... –0.3V to V_{CC} + 0.3V
Output Voltages
$\overline{FAULT}$, SD1, SD2, SD3,
FB1, FB2, FB3, STATUS ..... –0.3V to 10V
RAMPBUF, REMOTE ..... –0.3V to V_{CC} + 0.3V
RAMP ..... –0.3V to V_{CC} + 1V
GATE (Note 3) ..... –0.3V to 11.5V
Average Current
TRACK1, TRACK2, TRACK3 ..... 5mA
FB1, FB2, FB3 ..... 5mA
Operating Temperature Range
LTC2925C ..... 0°C to 70°C
LTC2925I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
MS Package ..... 300°C

PIN CONFIGURATION



GN PACKAGE
24-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 85°C/W



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
EXPOSED PAD (PIN 25) INTERNALLY CONNECTED
TO GND (PCB CONNECTION OPTIONAL)

T_{JMAX} = 125°C, θ_{JA} = 37°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2925CGN#PBF	LTC2925CGN#TRPBF	LTC2925CGN	24-Lead Plastic SSOP	0°C to 70°C
LTC2925IGN#PBF	LTC2925IGN#TRPBF	LTC2925IGN	24-Lead Plastic SSOP	–40°C to 85°C
LTC2925CUF#PBF	LTC2925CUF#TRPBF	2925	24-Lead (4mm × 4mm) Plastic QFN	0°C to 70°C
LTC2925IUF#PBF	LTC2925IUF#TRPBF	2925	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC2925CGN	LTC2925CGN#TR	LTC2925CGN	24-Lead Plastic SSOP	0°C to 70°C
LTC2925IGN	LTC2925IGN#TR	LTC2925IGN	24-Lead Plastic SSOP	–40°C to 85°C
LTC2925CUF	LTC2925CUF#TR	2925	24-Lead (4mm × 4mm) Plastic QFN	0°C to 70°C
LTC2925IUF	LTC2925IUF #TR	2925	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Input Supply Range		●	2.9		5.5	V
I_{CC}	Input Supply Current	I_{FBx} = 0, I_{TRACKx} = 0, $I_{RAMPBUF}$ = 0	●		1.5	3	mA
		I_{FBx} = –1mA, I_{TRACKx} = –1mA, $I_{RAMPBUF}$ = –3mA	●		10.5	15	mA
$V_{CC(UVL)}$	Input Supply Undervoltage Lockout	V_{CC} Rising	●	2.3	2.5	2.7	V
$\Delta V_{CC(UVL, HYST)}$	Input Supply Undervoltage Lockout Hysteresis				25		mV
ΔV_{GATE}	External N-Channel Gate Drive ($V_{GATE} – V_{CC}$)	I_{GATE} = –1µA	●	5	5.5	6	V
I_{GATE}	GATE Pin Current	Gate On, V_{GATE} = 0V, No Faults	●	–7	–10	–13	µA
		Gate Off, V_{GATE} = 5V, No Faults	●	7	10	13	µA
		Gate Off, V_{GATE} = 5V, Short-Circuit or Power Good Timeout	●	5	20	50	mA
$V_{ON(TH)}$	ON Pin Threshold Voltage	V_{ON} Rising	●	1.214	1.232	1.250	V
$\Delta V_{ON(HYST)}$	ON Pin Hysteresis		●	30	75	150	mV
$V_{ON(FC)}$	ON Pin Fault Clear Threshold Voltage		●	0.3	0.4	0.5	V
$I_{ON(IN)}$	ON Pin Input Current	V_{ON} = 1.2V, V_{CC} = 5.5V	●		0	±100	nA
$\Delta V_{RS-SENSE(TH)}$	Sense Resistor Overcurrent Voltage Threshold ($V_{SENSEP} – V_{SENSEN}$)	1V < V_{SENSEP} < V_{CC} 0V < V_{SENSEP} < 1V	● ●	40 30	50 50	60 70	mV mV
I_{SENSEN}	SENSEN Pin Input Current	0V < V_{SENSEN} < V_{CC}	●	–1	5	10	µA
I_{SENSEP}	SENSEP Pin Input Current	0V < V_{SENSEP} < V_{CC}	●	–1	5	10	µA
V_{OS}	Ramp Buffer Offset ($V_{RAMPBUF} – V_{RAMP}$)	$V_{RAMPBUF}$ = V_{CC}/2, $I_{RAMPBUF}$ = 0A	●	–30	0	30	mV
$V_{\overline{FAULT}(OL)}$	$\overline{FAULT}$ Output Low Voltage	$I_{\overline{FAULT}}$ = 3mA	●		0.2	0.4	V
$V_{\overline{SDx}(OL)}$	$\overline{SDx}$ Output Low Voltage	$I_{\overline{SDx}}$ = 1mA, V_{CC} = 2.3	●		0.2	0.4	V
$V_{STATUS(OL)}$	STATUS Output Low Voltage	I_{STATUS} = 3mA	●		0.2	0.4	V
I_{RAMP}	RAMP Pin Input Current	0V < RAMP < V_{CC}, V_{CC} = 5.5V	●		0	±1	µA
$V_{RAMPBUF(OL)}$	RAMPBUF Low Voltage	$I_{RAMPBUF}$ = 3mA	●		90	150	mV
$V_{RAMPBUF(OH)}$	RAMPBUF High Voltage ($V_{CC} – V_{RAMPBUF}$)	$I_{RAMPBUF}$ = –3mA	●		100	200	mV
$I_{ERROR(\%)}$	I_{FBx} to I_{TRACKx} Current Mismatch $I_{ERROR(\%)} = (I_{FBx} – I_{TRACKx})/I_{TRACKx}$	I_{TRACKx} = –10µA I_{TRACKx} = –1mA	● ●		0 0	±5 ±5	% %
V_{TRACKx}	TRACK Pin Voltage	I_{TRACKx} = –10µA I_{TRACKx} = –1mA	● ●	0.78 0.78	0.8 0.8	0.82 0.82	V V
$I_{FB(LEAK)}$	I_{FB} Leakage Current	V_{FB} = 1.5V, V_{CC} = 5.5V	●			±10	nA
$V_{FB(CLAMP)}$	V_{FB} Clamp Voltage	1µA < I_{FB} < 1mA	●	1.6	2.1	2.5	V
R_{REMOTE}	REMOTE Feedback Switch Resistance	2V < V_{REMOTE} < V_{CC}	●		15	30	Ω
$I_{SCTMR(UP)}$	Short-Circuit Timer Pull-Up Current	V_{SCTMR} = 1V	●	–35	–50	–65	µA
$I_{SCTMR(DN)}$	Short-Circuit Timer Pull-Down Current	V_{SCTMR} = 1V	●	1	2	3	µA
$V_{SCTMR(TH)}$	Short-Circuit Timer Threshold Voltage		●	1.1	1.23	1.4	V
$I_{SDTMR(UP)}$	Shutdown Timer Pull-Up Current	V_{SDTMR} = 1V	●	–7	–10	–13	µA
$V_{SDTMR(TH)}$	Shutdown Timer Threshold Voltage		●	1.1	1.23	1.4	V
$I_{PGI(UP)}$	Power Good Input Pull-Up Current	V_{PGI} = 0V	●	–5	–10	–15	µA
$V_{PGI(TH)}$	Power Good Input Threshold Voltage		●	0.8		1.4	V
$I_{PGTMR(UP)}$	Power Good Timer Pull-Up Current	V_{PGTMR} = 1V	●	–8	–10	–14	µA
$V_{PGTMR(TH)}$	Power Good Timer Threshold Voltage		●	1.1	1.23	1.4	V

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

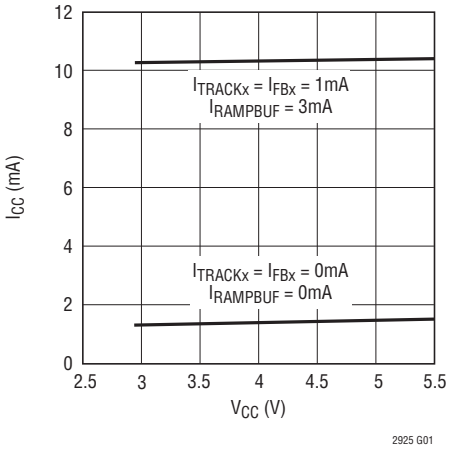
Note 2: All currents into the device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: The GATE pin is internally limited to a minimum of 11.5V. Driving this pin to voltages beyond the clamp may damage the part.

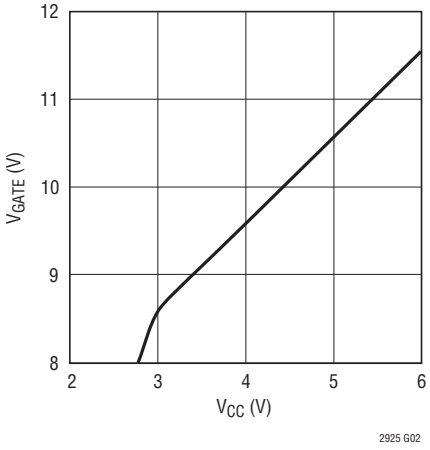
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C

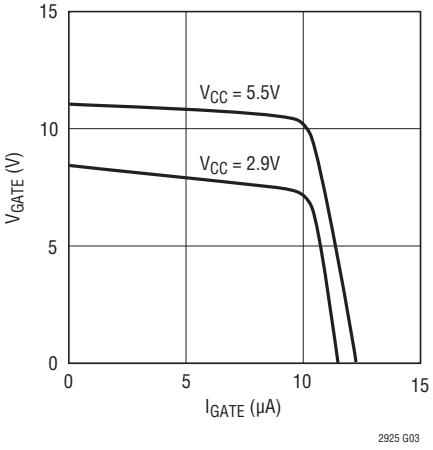
I_{CC} vs V_{CC}



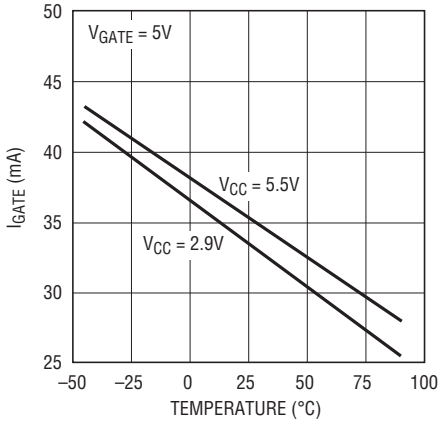
V_{GATE} vs V_{CC}



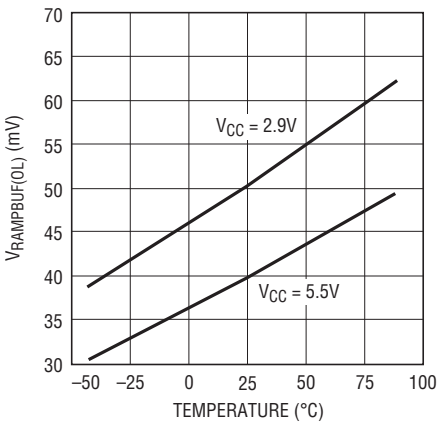
V_{GATE} vs I_{GATE}



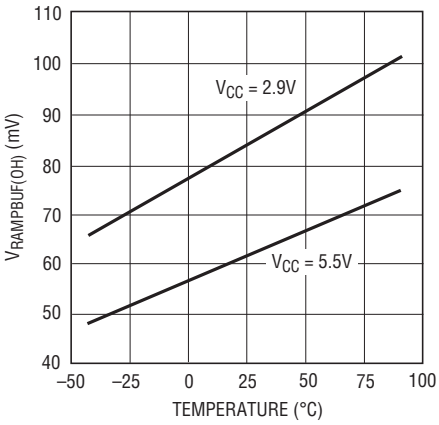
I_{GATE} Fast Pull-Down vs Temperature



$V_{RAMPBUF(OL)}$ vs Temperature



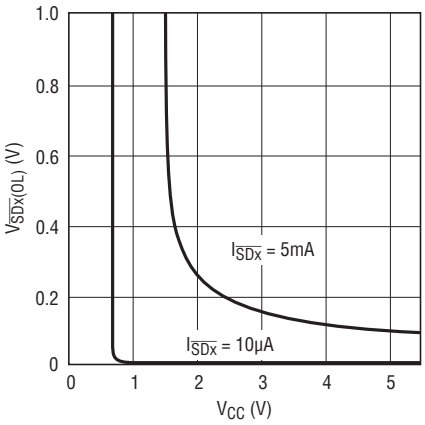
$V_{RAMPBUF(OH)}$ vs Temperature



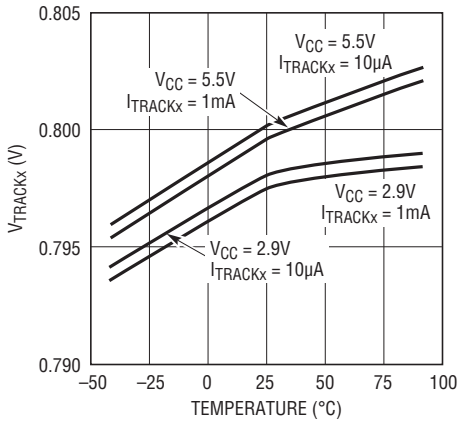
TYPICAL PERFORMANCE CHARACTERISTICS

Specifications are at T_A = 25°C

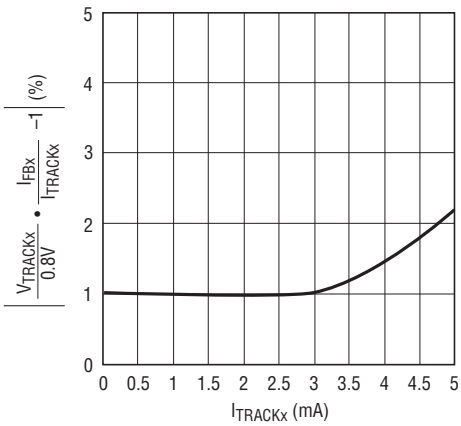
$V_{\overline{SDx}(OL)}$ vs V_{CC}



V_{TRACK} vs Temperature



Tracking Cell Error vs I_{TRACKx}



PIN FUNCTIONS

GN/UF Packages

V_{CC} (Pin 1/Pin 22): Positive Supply Input. The operating supply input range is 2.9V to 5.5V. An undervoltage lockout circuit resets the part when the supply is below 2.5V. V_{CC} should be bypassed to GND with a 0.1µF capacitor.

SENSEP (Pin 2/Pin 23): Circuit Breaker Positive Sense Input. SENSEP and SENSEN measure the voltage across the sense resistor and trigger the circuit breaker function when the current exceeds the level programmed by the sense resistor for longer than a short-circuit timer cycle (see SCTMR). If unused, tie SENSEN and SENSEP to V_{CC}.

SENSEN (Pin 3/Pin 24): Circuit Breaker Negative Sense Input. SENSEN connects to the low side of the current sense resistor. SENSEP and SENSEN monitor the current through the external FET by measuring the voltage across the sense resistor. The circuit breaker turns off the FET when the sense voltage exceeds 50mV for longer than a short circuit timer cycle (see SCTMR). If the short-circuit timer times out, the GATE pin will be pulled low immediately to protect the FET. If unused, tie SENSEN and SENSEP to V_{CC}.

ON (Pin 4/Pin 1): On Control Input. The ON pin has a threshold of 1.23V with 75mV of hysteresis. An active high will cause 10µA to flow from the GATE pin, ramping up the supplies. An active low pulls 10µA from the GATE pin, ramping the supplies down. Pulling the ON pin below 0.4V resets the electronic circuit breaker in the LTC2925. If a resistive divider connected to V_{CC} drives the ON pin, the supplies will automatically start up when V_{CC} is fully powered.

SDTMR (Pin 5/Pin 2): Shutdown Timer. A capacitor from SDTMR to GND sets the delay time between the ON pin transitioning high (which releases the $\overline{SDx}$ pins) and the supplies beginning to ramp-up. Float SDTMR when it is unused.

$\overline{SD1}$, $\overline{SD2}$, $\overline{SD3}$ (Pins 6, 7, 8/Pins 3, 4, 5): Outputs for Slave Supply Shutdowns. The $\overline{SDx}$ pins are open-drain outputs that hold the shutdown (RUN/SS) pins of the slave supplies low until the ON pin is pulled above 1.23V. The $\overline{SDx}$ pins will be pulled low again when RAMP <100mV and ON <1.23V. If a slave supply is capable of operating with an input supply that is lower than the LTC2925's minimum operating voltage of 2.9V, the $\overline{SDx}$ pins can be used to hold off the slave supplies. Each $\overline{SDx}$ pin is capable of sinking greater than 1mA with supplies as low as 2.3V.

RAMPBUF (Pin 9/Pin 6): Ramp Buffer Output. Provides a low impedance buffered version of the signal on the RAMP pin. This buffered output drives the resistive dividers that connect to the TRACKx pins. Limit the capacitance at the RAMPBUF pin to less than 100pF.

GND (Pin 10/Pins 7, 25): Circuit Ground.

TRACK1, TRACK2, TRACK3 (Pins 15, 14, 12/Pins 12, 11, 9): Tracking Control Input Pin. A resistive divider between RAMPBUF, TRACKx and GND determines the tracking

PIN FUNCTIONS GN/UF Packages

profile of OUTx (see Applications Information). TRACKx pulls up to 0.8V and the current supplied at TRACKx is mirrored at FBx. The TRACKx pin is capable of supplying at least 1mA when V_{CC} = 2.9V. It may be capable of supplying up to 30mA when the supply is at 5.5V, so care should be taken not to short this pin for extended periods. Limit the capacitance at the TRACKx pin to less than 25pF. Float the TRACKx pins if unused.

FB1, FB2, FB3 (Pins 16, 13, 11/Pins 13, 10, 8): Feedback Control Output. FBx connects to the feedback node of slave supplies. Tracking is achieved by mirroring the current from TRACKx into FBx. If the appropriate resistive divider connects RAMPBUF and TRACKx, the FBx current will force OUTx to track RAMP. The LTC2925 is capable of controlling slave supplies with feedback voltages between 0V and 1.6V. To prevent damage to the slave supply, the FBx pin will not force the slave's feedback node above 2.5V. In addition, it will not actively sink current from this node even when the LTC2925 is unpowered. Float the FBx pins if unused.

REMOTE (Pin 17/Pin 14): Remote Sense Switch. A 15Ω switch connects REMOTE to RAMP when the GATE is fully enhanced (GATE > RAMP + 4.9V). Otherwise, it presents a high impedance. When the slave supplies track the master supply, REMOTE can be used to compensate for the voltage drop across the external sense resistor and N-channel FET. A resistor between the output and the sense nodes of the master supply provides feedback before the external FET is fully enhanced. If an external FET is not used, float REMOTE.

RAMP (Pin 18/Pin15): Ramp Buffer Input. When the RAMP pin is connected to the source of the external N-channel FET, the slave supplies track the FET's source as it ramps up and down. Alternatively, when no external FET is used, the RAMP pin can be tied directly to the GATE pin. In this configuration, the supplies track the capacitor on the GATE pin as it is charged and discharged by the 10µA current source controlled by the ON pin. When the GATE is fully enhanced (GATE > RAMP + 4.9V) the open-drain STATUS pin goes high impedance and the remote sense switch connects the RAMP pin to the REMOTE pin.

GATE (Pin 19/Pin 16): Gate Drive for External N-Channel FET. When the ON pin is high, an internal 10µA current source charges the gate of the external N-channel MOSFET. A capacitor connected from GATE to GND sets the ramp rate. It is a good practice to add a 10Ω resistor between this capacitor and the FET's gate to prevent high frequency FET oscillations. An internal charge pump guarantees that GATE will pull up to 5V above V_{CC} ensuring that logic-level N-channel FETs are fully enhanced. When the ON pin is pulled low, the GATE pin is pulled to GND with a 10µA current source. Under a short-circuit condition, the electronic circuit breaker in the LTC2925 pulls the GATE low immediately with 20mA. Tie GATE to GND if unused.

$\overline{\text{FAULT}}$ (Pin 20/Pin 17): Circuit Breaker and Power Good Timer Fault Output. $\overline{\text{FAULT}}$ is an open-drain output that pulls low when the electronic circuit breaker is activated or a power good timeout fault is detected. $\overline{\text{FAULT}}$ is reset by pulling ON below 0.4V. To allow retry, tie $\overline{\text{FAULT}}$ to ON.

STATUS (Pin 21/Pin 18): Power Good Status Indicator. The STATUS pin is an open-drain output that pulls low until GATE has been fully charged at which time all supplies will have reached their final operating voltage.

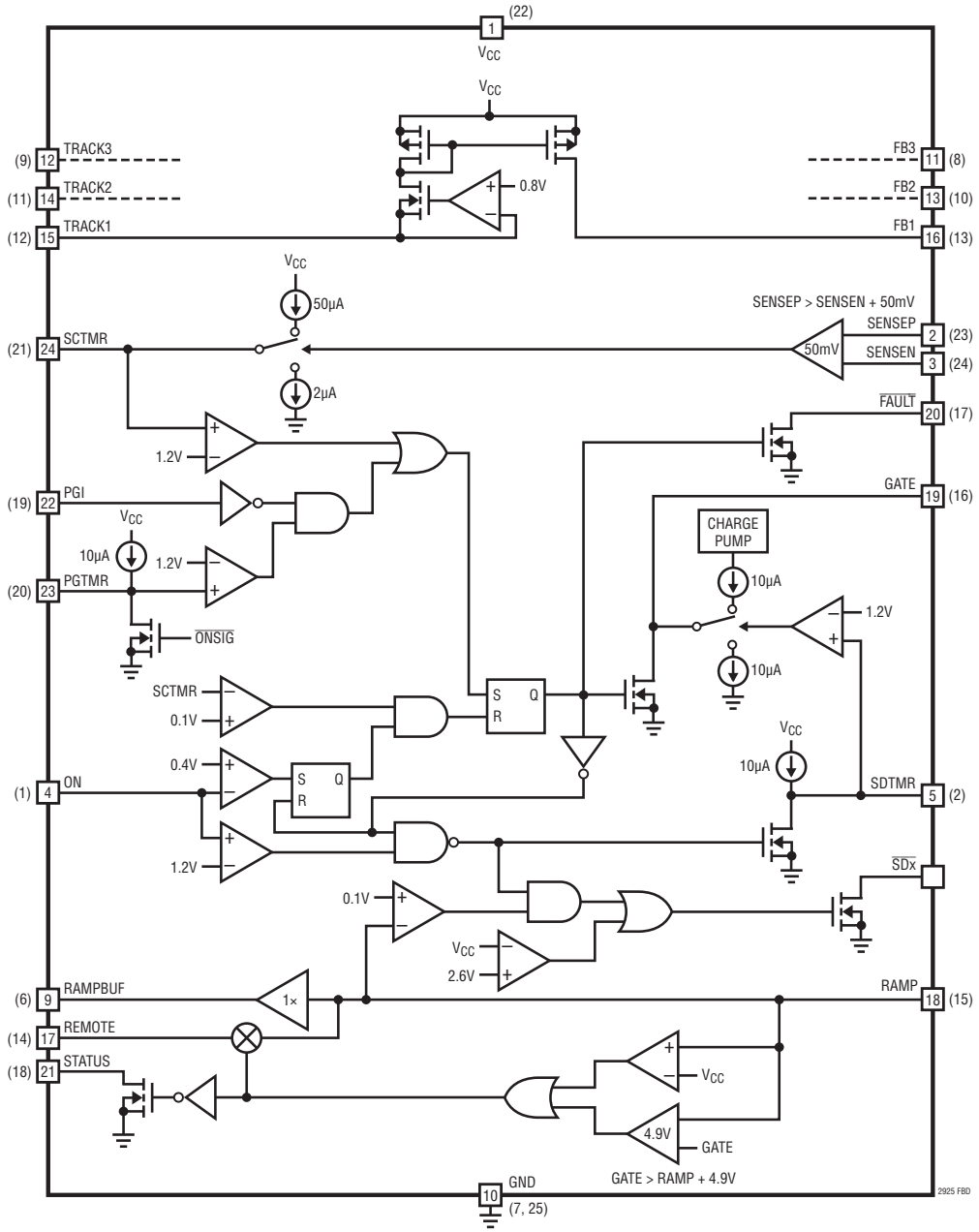
PGI (Pin 22/Pin 19): Power Good Timer Input. PGI connects to the $\overline{\text{RST}}$ pin of the downstream supply monitor. If PGI has not transitioned high within a power good timer cycle (see PGTMR), the $\overline{\text{FAULT}}$ pin will be pulled low and the supplies will be turned off by pulling the GATE pin low with 20mA. PGI is pulled up with 10µA. An internal Schottky diode allows PGI to be pulled safely above V_{CC}. Float PGI when it is unused.

PGTMR (Pin 23/Pin 20): Power Good Timer. A capacitor from PGTMR to GND sets the power good timer duration. While ON > 1.23V, the PGTMR pin will pull up to V_{CC} with 10µA. Otherwise, it pulls to GND. If the voltage on the PGTMR pin exceeds 1.23V and PGI is still low, $\overline{\text{FAULT}}$ will be pulled low and the GATE will be pulled to ground with 20mA until the power good timer fault is cleared by pulling ON below 0.4V. If $\overline{\text{FAULT}}$ is tied back to ON the system will automatically retry after a $\overline{\text{FAULT}}$. In this mode, verify that the slave supplies' current limits provide sufficient protection under short-circuit conditions. Tie PGTMR to GND when it is unused.

PIN FUNCTIONS GN/UF Packages

SCTMR (Pin 24/Pin 21): Circuit Breaker Timer. A capacitor from SCTMR to GND programs the maximum time that a short circuit can be sustained before GATE is pulled low. When (SENSEP – SENSEN) > 50mV, SCTMR will pull up with 50µA, otherwise it pulls down with 2µA. When the voltage at SCTMR exceeds 1.23V, the GATE will be pulled to ground with 20mA and the $\overline{\text{FAULT}}$ pin will be pulled low. The circuit breaker function is reset by pulling ON below 0.4V. The GATE pin will not rise again until SCTMR has been pulled below 100mV by the 2µA current source. If FAULT is tied back to ON the system will automatically retry after a fault. Tie SCTMR to GND if the circuit breaker is not used.

BLOCK DIAGRAM Pin numbers in parentheses are for the UF package.



APPLICATIONS INFORMATION

Power Supply Tracking and Sequencing

The LTC2925 handles a variety of power-up profiles to satisfy the requirements of digital logic circuits including FPGAs, PLDs, DSPs and microprocessors. These requirements fall into one of the four general categories illustrated in Figures 1 to 4.

Some applications require that the potential difference between two power supplies must never exceed a specified voltage. This requirement applies during power-up and power-down as well as during steady-state operation, often to prevent destructive latch-up in a dual supply IC. Typically, this is achieved by ramping the supplies up and down together (Figure 1). In other applications it is desirable to have the supplies ramp up and down with fixed voltage offsets between them (Figure 2) or to have them ramp up and down ratiometrically (Figure 3).

Certain applications require one supply to come up after another. For example, a system clock may need to start before a block of logic. In this case, the supplies are sequenced as in Figure 4 where the 1.8V supply ramps up completely followed by the 2.5V supply and then the 1.5V supply.

Operation

The LTC2925 provides a simple solution to all of the power supply tracking and sequencing profiles shown in Figures 1 to 4. A single LTC2925 controls up to four supplies with three "slave" supplies that track a "master" signal. With just two resistors, a slave supply is configured to ramp up as a function of the master signal. This master signal can be a fourth supply that is ramped up through an external FET, whose ramp rate is set with a single capacitor, or it can be a signal generated by tying the GATE and RAMP pins to an external capacitor.

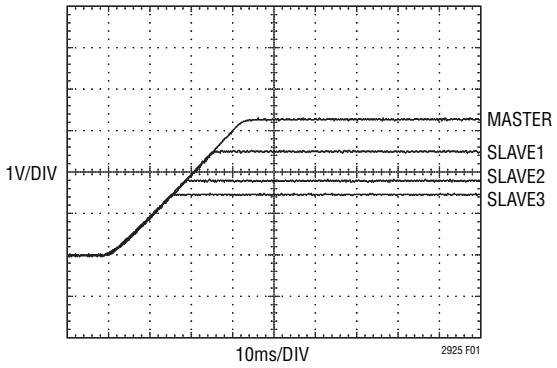


Figure 1. Coincident Tracking

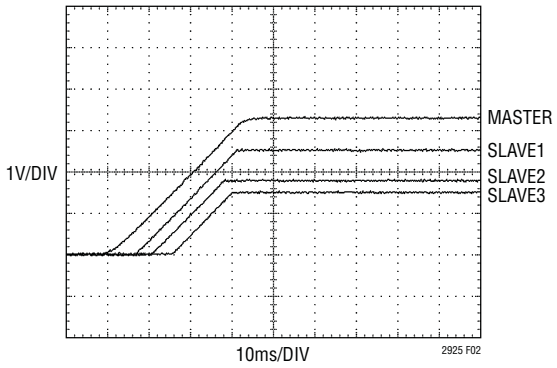


Figure 2. Offset Tracking

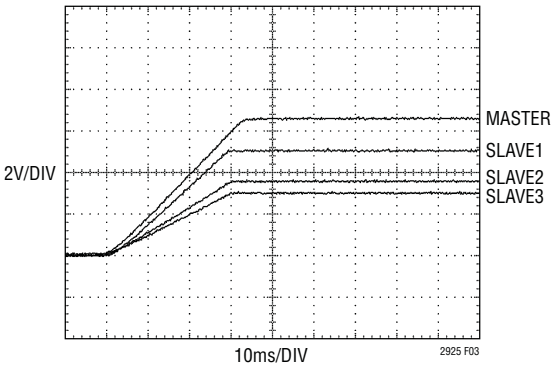


Figure 3. Ratiometric Tracking

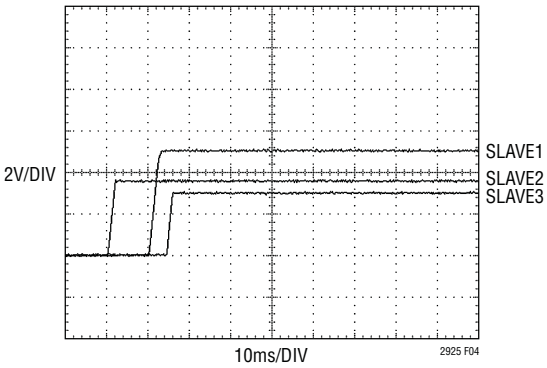


Figure 4. Supply Sequencing

APPLICATIONS INFORMATION

Tracking Cell

The LTC2925's operation is based on the tracking cell shown in Figure 5, which uses a proprietary wide-range current mirror. The tracking cell shown in Figure 5 servos the TRACK pin at 0.8V. The current supplied by the TRACK pin is mirrored at the FB pin to establish a voltage at the output of the slave supply. The slave output voltage varies with the master signal, enabling the slave supply to be controlled as a function of the master signal with terms set by R_{TA} and R_{TB}. By selecting appropriate values of R_{TA} and R_{TB}, it is possible to generate any of the profiles in Figures 1 to 4.

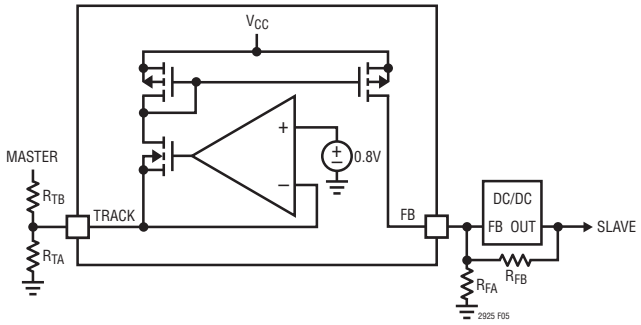


Figure 5. Simplified Tracking Cell

Controlling the Ramp-Up and Ramp-Down Behavior

The operation of the LTC2925 is most easily understood by referring to the simplified functional diagram in Figure 6. When the ON pin is low, the GATE pin is pulled to ground causing the master signal to remain low. Since the current through R_{TB1} is at its maximum when the master signal is low, the current from FB1 is also at its maximum. This current drives the slave's output to its minimum voltage.

When the ON pin rises above 1.23V, the master signal rises and the slave supply tracks the master signal. The ramp rate is set by an external capacitor driven by a 10µA current source from an internal charge pump. If no external FET is used, the ramp rate is set by tying the RAMP and GATE pins together at one terminal of the external capacitor (see the Ratiometric Tracking Example).

In a properly designed system, when the master signal has reached its maximum voltage the current from the TRACK1 pin is zero. In this case, there is no current from the FB1 pin and the LTC2925 has no effect on the output voltage accuracy, transient response or stability of the slave supply.

When the ON pin falls below $V_{ON(TH)} - \Delta V_{ON(HYST)}$, typically 1.225V, the GATE pin pulls down with 10µA and the master signal and the slave supplies will fall at the same rate as they rose previously.

The ON pin can be controlled by a digital I/O pin or it can be used to monitor an input supply. By connecting a resistive divider from an input supply to the ON pin, the supplies will ramp up only after the monitored supply has reached a preset voltage.

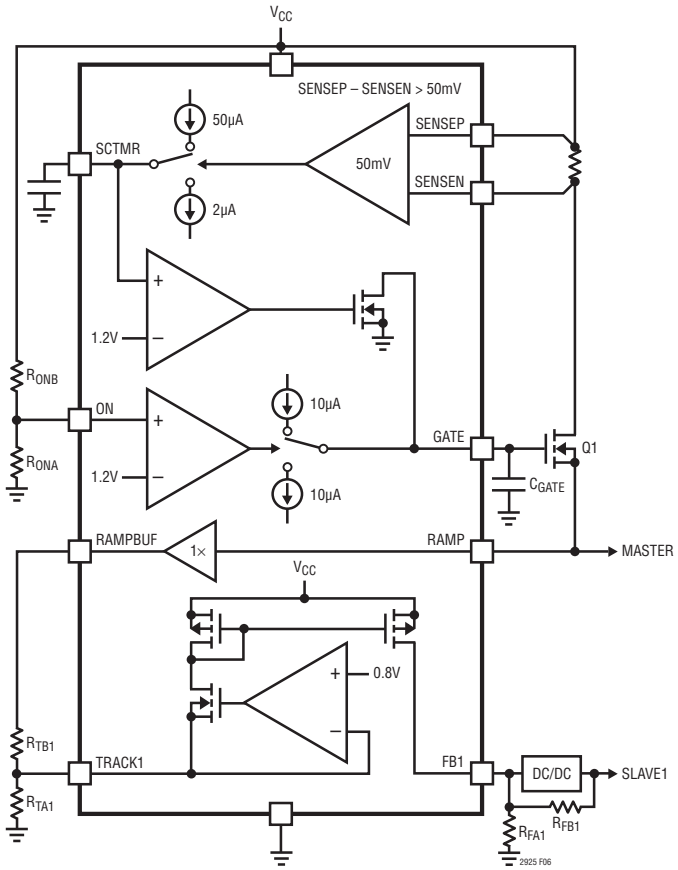


Figure 6. Simplified Functional Block Diagram

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Optional External FET

Figure 7 illustrates how an optional external N-channel FET can ramp up a single supply that becomes the master signal. When used, the FET's gate is tied to the GATE pin and its source is tied to the RAMP pin. Under normal operation, the GATE pin sources or sinks 10µA to ramp the FET's gate up or down at a rate set by the external capacitor connected to the GATE pin.

The series FET easily controls any supply with an output voltage between 0V and V_{CC}. See the Typical Applications section for examples.

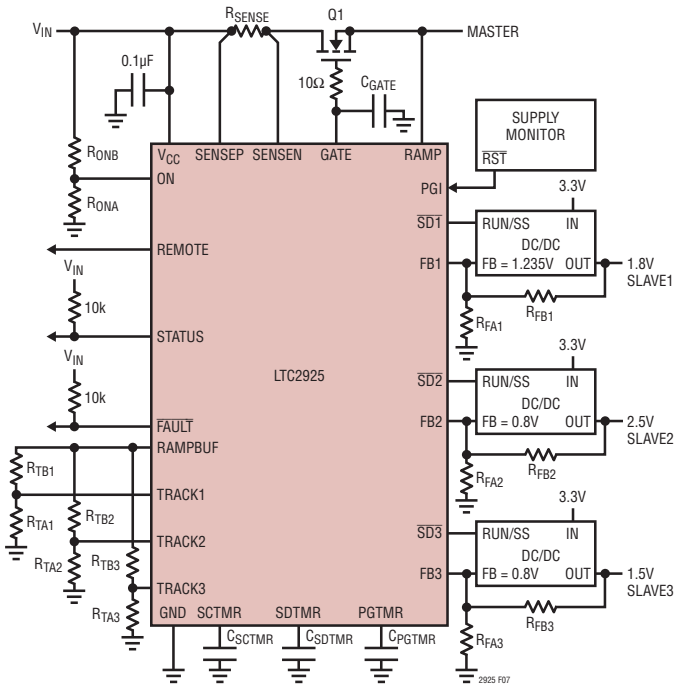

Figure 7. Typical Application with External FET

Electronic Circuit Breaker

The LTC2925 features an electronic circuit breaker function that protects the optional series FET against short circuits. An external sense resistor is used to measure the current flowing in the FET. If the voltage across the sense resistor exceeds 50mV for more than a short-circuit timer cycle, the gate of the FET is pulled low with 20mA, turning it off.

The short-circuit timer duration is configured by a capacitor tied between SCTMR and GND. SCTMR will pull up with 50µA when SENSEP – SENSEN > 50mV. Otherwise, it pulls down with 2µA. When the voltage at SCTMR exceeds 1.23V, the GATE will be pulled to ground with 20mA and the $\overline{FAULT}$ pin will be pulled low. Thus, the capacitor, C_{SCTMR}, required to configure the short-circuit timer duration, t_{SCTMR} is determined from:

$$C_{SCTMR} = \frac{50\mu A \bullet t_{SCTMR}}{1.23V}$$

Because the slave supplies track the RAMP pin which is driven by the external FET, they are pulled low by the tracking circuit when a short-circuit fault occurs. Following a short-circuit fault, the FET is latched off and $\overline{FAULT}$ is pulled low until the fault is cleared by pulling the ON pin below 0.4V. Note that the supplies will not be allowed to ramp up again until SCTMR has been pulled below about 100mV by the 2µA pull-down current source. The electronic circuit breaker supports any supply voltage between 0V and V_{CC}. Although it is normally used to monitor current through the optional series FET, it is capable of monitoring other currents, including the current from a slave supply. The Typical Applications section shows one such example.

If the electronic circuit breaker is not used, tie SENSEP and SENSEN to V_{CC} and SCTMR to GND.

Power Good Timeout

The power good timeout circuit turns off the supplies if an external supply monitor, connected to the PGI pin, fails to indicate that all supplies have entered regulation in time after power up begins. After power up is complete, it turns off the supplies if any supply exits regulation.

The power good timer duration is configured by a capacitor tied between PGTMR and GND. PGTMR will pull up the CPGTMR capacitor with 10µA starting when the ON pin is driven above 1.23V. Once the voltage at the PGTMR exceeds 1.23V, a fault will trip if the PGI pin is low. When the power good timeout circuit detects a fault, the GATE

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pin is pulled low, the supplies are latched off, and the $\overline{FAULT}$ pin is held low until the fault is cleared by taking the ON pin below 0.4V.

The PGI pin, which is normally connected to the $\overline{RST}$ pin of an external supply monitor, is pulled up with 10µA through a Schottky diode allowing it to be pulled safely above V_{CC}. Since, PGTMR pulls up with a 10µA current source, the capacitor, C_{PGTMR}, required to configure the power good timeout duration, t_{PGTMR}, is determined from:

$$C_{PGTMR} = \frac{10\mu A \bullet t_{PGTMR}}{1.23V}$$

If the power good timeout circuit is unused, tie PGTMR low and float PGI.

The Ramp Buffer

The RAMPBUF pin provides a buffered version of the RAMP pin voltage that drives the resistive dividers on the TRACKx pins. When there is no external FET, it provides up to 3mA to drive the resistors even though the GATE pin only supplies 10µA (Figure 8). The RAMPBUF pin also proves useful in systems with an external FET. Since the track cell drives 0.8V on the TRACKx pins, if R_{TBx} is connected directly to the FET's source, the TRACKx pin could potentially pull up the FET's source towards 0.8V when the FET is off. RAMPBUF blocks this path.

Shutdown Outputs

In some applications it might be necessary to control the shutdown or RUN/SS pins of the slave supplies. The LTC2925 may not be able to supply the rated 1mA of current from the FB1, FB2, and FB3 pins when V_{CC} is below 2.9V. If the slave power supplies are capable of operating at low input voltages, use the open-drain $\overline{SDx}$ outputs to drive the SHDN or RUN/SS pins of the slave supplies (Figures 7 and 8). The $\overline{SDx}$ pins are released when the ON pin rises above 1.23V, V_{CC} is above the 2.6V undervoltage lockout condition, and there are no faults latched. The shutdown timer begins at the same time, and the supplies begin to ramp up after the shutdown timer cycle completes. The duration of the timer cycle is configured by a capacitor tied between SDTMR and GND. The capacitor voltage is ramped up by a 10µA current source and the SDTMR cycle completes when its voltage reaches 1.23V. Thus, the capacitor, C_{SDTMR}, required for a given shutdown timer cycle, t_{SDTMR}, is determined from:

$$C_{SDTMR} = \frac{10\mu A \bullet t_{SDTMR}}{1.23V}$$

The $\overline{SDx}$ pins pull low again when the ON pin is pulled below 1.23V and the RAMP pin is below about 100mV.

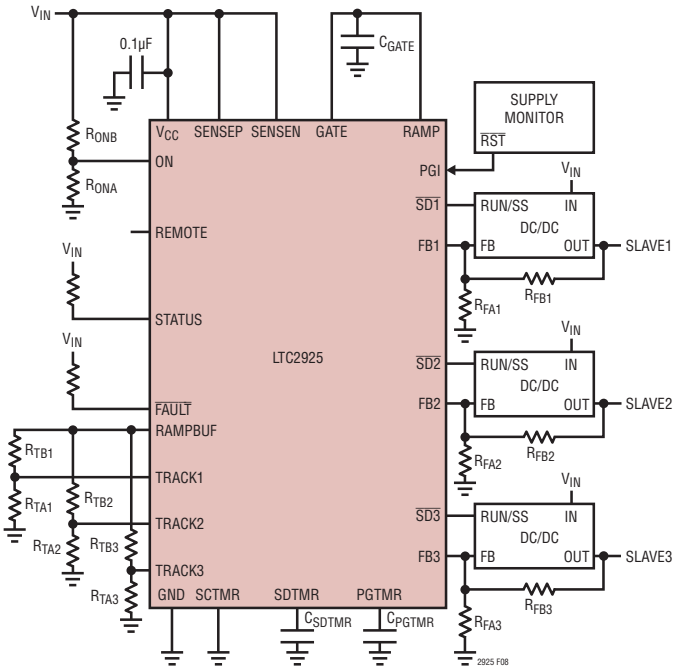

Figure 8. Typical Application Without External FET

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Status Output

The STATUS pin provides an indication that the supplies are finished ramping up. This pin is an open-drain output that pulls low until the GATE has been fully charged. Since the GATE pin drives the gate of the external FET, or the RAMP pin directly when no FET is used, the supplies are completely ramped up when the GATE pin is fully charged. The STATUS pin will go low again when the GATE pin is pulled low, either because of a short-circuit fault, a power good timeout fault, or because the ON pin has been pulled low.

Fault Output

The $\overline{\text{FAULT}}$ pin is an open-drain output that pulls low when the electronic circuit breaker is activated due to a short-circuit or power good timeout fault. $\overline{\text{FAULT}}$ is reset by pulling ON below 0.4V. The supplies will not be allowed to ramp up again until the SCTMR, PGTMR and SDTMR pins are below about 100mV, and the ON pin is pulled above 1.23V.

Retry on Fault

The LTC2925 continuously attempts to ramp up the outputs after a fault if the $\overline{\text{FAULT}}$ pin is tied to the ON pin (Figure 9). If a short-circuit fault occurs in this configuration, the SCTMR pin ramps up the C_{SCTMR} capacitor with 50µA until it reaches 1.23V. Then, GATE is pulled low turning off the shorted FET. At the same time, the $\overline{\text{FAULT}}$ pin's open-drain output pulls ON low. The C_{SCTMR} capacitor is pulled down with 2µA until it reaches about 100mV. After the C_{SCTMR} capacitor reaches 100mV, the shutdown timer begins and upon completing a shutdown timer cycle, the supplies start ramping up again. If there is no short-circuit this time, the supplies will come up normally. Otherwise the retry cycle will repeat. If a longer off time is required between retry attempts, the C_{SDTMR} capacitor value can be increased, providing a greater delay before the FET's GATE ramps up on each cycle. Note that tying $\overline{\text{FAULT}}$ to ON also causes the LTC2925 to retry on Power Good Timeout faults. In this mode, verify that the slave supplies' current limits provide sufficient protection under short-circuit conditions.

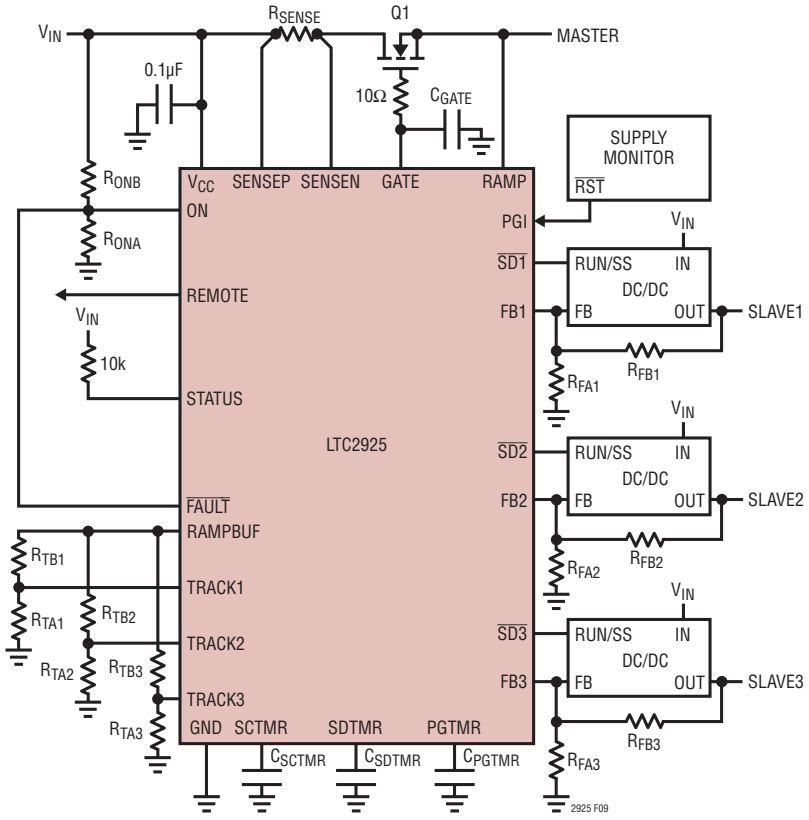

Figure 9. Retry on Fault

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3-Step Design Procedure

The following 3-step design procedure allows one to choose the TRACK resistors, R_{TAx} and R_{TBx}, and the gate capacitor, C_{GATE}, that give any of the tracking or sequencing profiles shown in Figures 1 to 4. A basic four supply application circuit is shown in Figure 10.

1. *Set the ramp rate of the master signal.*

Solve for the value of C_{GATE}, the capacitor on the GATE pin, based on the desired ramp rate (V/s) of the master supply, S_M:

$$C_{GATE} = \frac{I_{GATE}}{S_M} \text{ where } I_{GATE} \approx 10\mu A \quad (1)$$

If the external FET has a gate capacitance comparable to C_{GATE}, then the external capacitor's value should be reduced to compensate for the FET's gate capacitance.

If no external FET is used, tie the GATE and RAMP pins together, connect SENSEN and SENSEP to V_{CC}, and connect SCTMR to GND.

2. *Solve for the pair of resistors that provide the desired ramp rate of the slave supply, assuming no delay.*

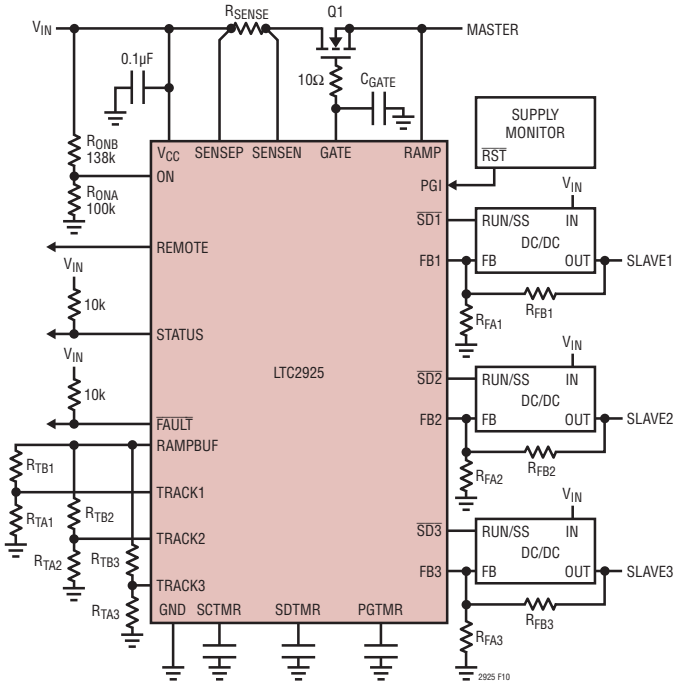

Figure 10. Four Supply Application

Choose a ramp rate for the slave supply, S_S. If the slave supply ramps up coincident with the master supply or with a fixed voltage offset, then the ramp rate equals the master supply's ramp rate. Be sure to use a fast enough ramp rate for the slave supply so that it will finish ramping before the master supply has reached its final supply value. If not, the slave supply will be held below the intended regulation value by the master supply. Use the following formulas to determine the resistor values for the desired ramp rate, where R_{FB} and R_{FA} are the feedback resistors in the slave supply and V_{FB} is the feedback reference voltage of the slave supply:

$$R_{TB} = R_{FB} \bullet \frac{S_M}{S_S} \quad (2)$$

$$R_{TA}' = \frac{V_{TRACK}}{\frac{V_{FB}}{R_{FB}} + \frac{V_{FB}}{R_{FA}} - \frac{V_{TRACK}}{R_{TB}}} \quad (3)$$

where $V_{TRACK} \approx 0.8V$.

Note that large ratios of slave ramp rate to master ramp rate, S_S/S_M, may result in negative values for R_{TA}'. If a sufficiently large delay is used in step 3, R_{TA} will be positive, otherwise S_S/S_M must be reduced.

3. *Choose R_{TA} to obtain the desired delay.*

If no delay is required, such as in coincident and ratiometric tracking, then simply set $R_{TA} = R_{TA}'$. If a delay is desired, as in offset tracking and supply sequencing, calculate R_{TA}'' to determine the value of R_{TA} where t_D is the desired delay.

$$R_{TA}'' = \frac{V_{TRACK} \bullet R_{TB}}{t_D \bullet S_M} \quad (4)$$

$$R_{TA} = R_{TA}' \,||\, R_{TA}'' \quad (5)$$

the parallel combination of R_{TA}' and R_{TA}''.

As noted in step 2, small delays and large ratios of slave ramp rate to master ramp rate (usually only seen in sequencing) may result in solutions with negative values for R_{TA}. In such cases, either the delay must be increased or the ratio of slave ramp rate to master ramp rate must be reduced.

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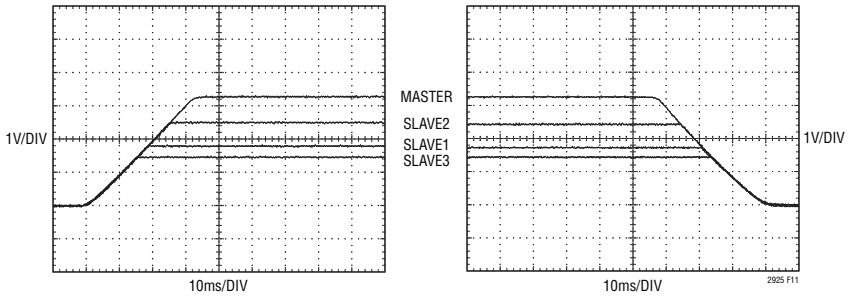

Figure 11. Coincident Tracking from Figure 12

Coincident Tracking Example

A typical four supply application is shown in Figure 12. The master signal is a 3.3V module. The slave 1 supply is a 1.8V switching power supply, the slave 2 supply is a 2.5V switching power supply, and the slave 3 supply is a 1.5V supply. All three slave supplies track coincidently with the 3.3V supply that is controlled with an external FET. The ramp rate of the supplies is 100V/s. The 3-step design procedure detailed previously can be used to determine component values. Only the slave 1 supply is considered here as the procedure is the same for the other supplies.

1. *Set the ramp rate of the master signal.*

From Equation 1:

$$C_{GATE} = \frac{10\mu A}{100V/s} = 0.1\mu F$$

2. *Solve for the pair of resistors that provide the desired slave supply behavior, assuming no delay.*

From Equation 2:

$$R_{TB} = 16.5k \bullet \frac{100V/s}{100V/s} = 16.5k$$

From Equation 3:

$$R_{TA}' = \frac{0.8V}{\frac{1.235V}{16.5k} + \frac{1.235V}{35.7k} - \frac{0.8V}{16.5k}} \approx 13k$$

3. *Choose RTA to obtain the desired delay.*

Since no delay is desired, $R_{TA} = R_{TA}'$.

In this example, all supplies remain low while the ON pin is held below 1.23V. When the ON pin rises above 1.23V, 10µA pulls up CGATE and the gate of the FET at 100V/s. As the gate of the FET rises, the source follows and pulls up the output to 3.3V at 100V/s. This output serves as the master signal and is buffered from the RAMP pin to the RAMPBUF pin. As this output and the RAMPBUF pin rise, the current from the TRACKx pins is reduced. Consequently, the voltages at the slave supplies' outputs increase, and the slave supplies track the master supply. When the ON pin is again pulled below 1.23V, 10µA will pull down C_{GATE} and the gate of the FET at 100V/s. If the loads on the outputs are sufficient, all outputs will track down coincidently at 100V/s.

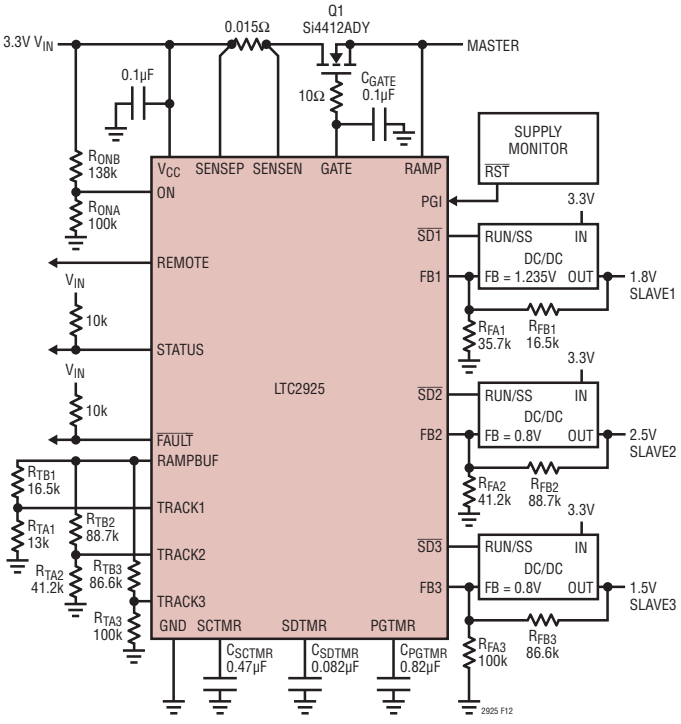

Figure 12. Coincident Tracking Example

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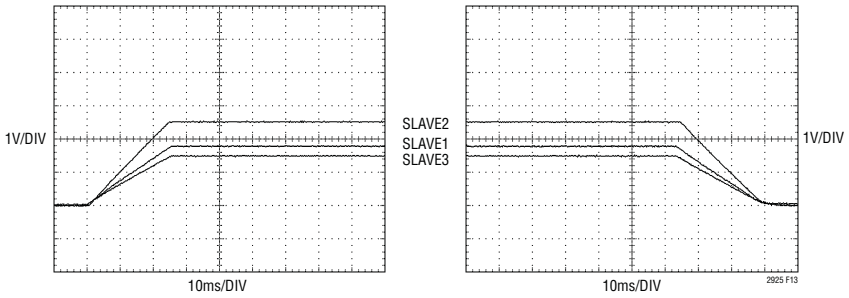

Figure 13. Ratiometric Tracking from Figure 14

Ratiometric Tracking Example

This example converts the coincident tracking example to the ratiometric tracking profile shown in Figure 13, using three supplies without an external FET. The ramp rate of the master signal remains unchanged (step 1) and there is no delay in ratiometric tracking (step 3), so only the result of step 2 in the 3-step design procedure needs to be considered. In this example, the ramp rate of the 1.8V slave 1 supply ramps up at 60V/s, the 2.5V slave 2 supply ramps up at 85V/s, and the 1.5V slave 3 supply ramps up at 50V/s. Always verify that the chosen ramp rate will allow the supplies to ramp-up completely before RAMPBUF reaches V_{CC}. If the 1.8V supply were to ramp-up at 50V/s it would only reach 1.65V because the RAMPBUF signal would reach its final value of V_{CC} = 3.3V before the slave supply reached 1.8V.

2. *Solve for the pair of resistors that provide the desired slave supply behavior, assuming no delay.*

From Equation 2:

$$R_{TB} = 16.5k \bullet \frac{100V/s}{60V/s} \approx 27.4k$$

From Equation 3:

$$R_{TA}' = \frac{0.8V}{\frac{1.235V}{16.5k} + \frac{1.235V}{35.7k} - \frac{0.8V}{27.5k}} \approx 10k$$

Step 3 is unnecessary because there is no delay, so $R_{TA} = R_{TA}'$.

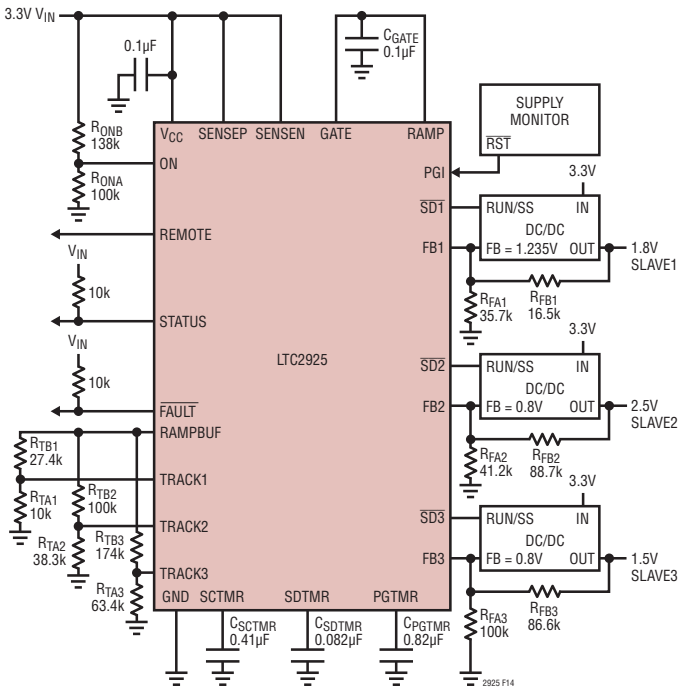

Figure 14. Ratiometric Tracking Example

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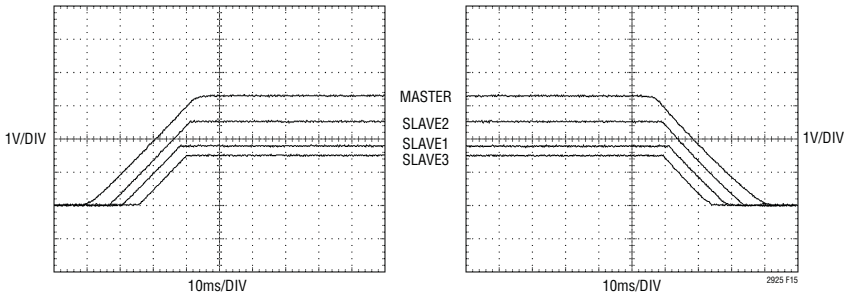

Figure 15. Offset Tracking from Figure 16

Offset Tracking Example

Converting the circuit in the coincident tracking example to the offset tracking shown in Figure 15 is relatively simple. Here the 1.8V slave 1 supply ramps up 1V below the master. The ramp rate remains the same (100V/s), so there are no changes necessary to steps 1 and 2 of the 3-step design procedure. Only step 3 must be considered. Be sure to verify that the chosen voltage offsets will allow the slave supplies to ramp up completely. In this example, if the voltage offset were 2V, the slave supply would only ramp up to 3.3V – 2V = 1.3V.

3. *Choose R_{TA} to obtain the desired delay.*

First, convert the desired voltage offset, V_{OS}, to a delay, t_D, using the ramp rate:

$$t_D = \frac{V_{OS}}{S_S} = \frac{1V}{100V/s} = 10ms \quad (6)$$

From Equation 4:

$$R_{TA}'' = \frac{0.8V \bullet 16.5k}{1ms \bullet 100V/s} = 13.2k$$

From Equation 5:

$$R_{TA} = 13.1k \,||\, 13.2k \approx 6.65k$$

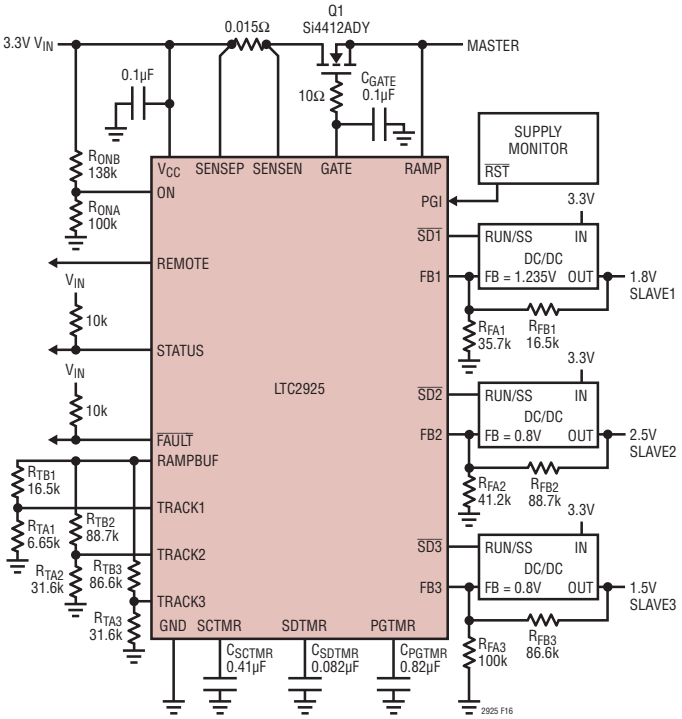

Figure 16. Offset Tracking Example

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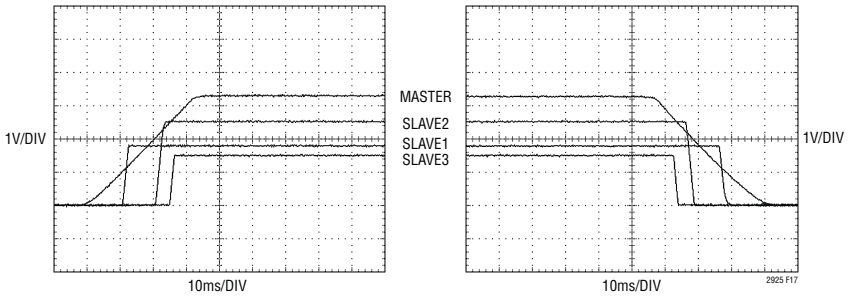

Figure 17. Supply Sequencing from Figure 18

Supply Sequencing Example

In Figure 17, the three slave supplies are sequenced instead of tracking. As in the coincident tracking example, the 3.3V master supply ramps up at 100V/s through an external FET, so step 1 remains the same. The 1.8V slave 1 supply ramps up at 1000V/s beginning 10ms after the master signal starts to ramp up. The 2.5V slave 2 supply ramps up at 1000V/s beginning 20ms after the master signal begins to ramp up. The 1.5V slave 3 supply ramps up at 1000V/s beginning 25ms after the master signal begins to ramp up. Note that not every combination of ramp rates and delays is possible. Small delays and large ratios of slave ramp rate to master ramp rate may result in solutions that require negative resistors. In such cases, either the delay must be increased or the ratio of slave ramp rate to master ramp rate must be reduced. In this example, solving for the slave 1 supply yields:

2. *Solve for the pair of resistors that provide the desired slave supply behavior, assuming no delay.*

From Equation 2:

$$R_{TB} = 16.5k \bullet \frac{100V/s}{1000V/s} \approx 1.65k$$

From Equation 3:

$$R_{TA}' = \frac{0.8V}{\frac{1.235V}{16.5k} + \frac{1.235V}{35.7k} - \frac{0.8V}{1.65k}} \approx -2.13k$$

3. *Choose R_{TA} to obtain the desired delay.*

From Equation 4:

$$R_{TA}'' = \frac{0.8V \bullet 1.65k}{10ms \bullet 100V/s} = 1.32k$$

From Equation 5:

$$R_{TA} = -2.13k \,||\, 1.32k \approx 3.48k$$

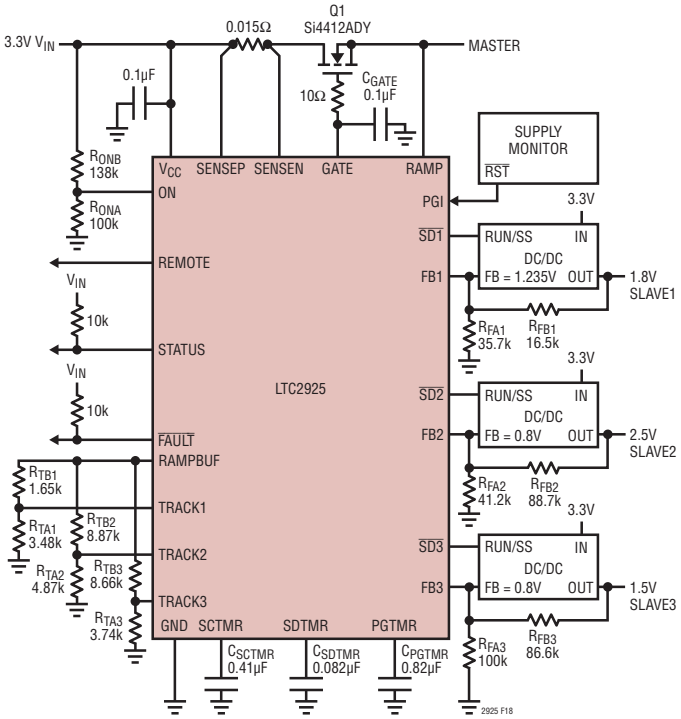

Figure 18. Supply Sequencing Example

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Final Sanity Checks

The collection of equations below is useful for identifying unrealizable solutions.

As stated in step 2, the slave supply must finish ramping before the master signal has reached its final voltage. This can be verified by the following equation:

$$V_{TRACK}\left(1+\frac{R_{TB}}{R_{TA}}\right) < V_{MASTER}$$

Here, $V_{TRACK} = 0.8V$. V_{MASTER} is the final voltage of the master signal, either the supply voltage ramped up through the optional external FET or V_{CC} when no FET is present.

It is possible to choose resistor values that require the LTC2925 to supply more current than the Electrical Characteristics table guarantees. To avoid this condition, check that I_{TRACKx} does not exceed 1mA and $I_{RAMPBUF}$ does not exceed ±3mA.

To confirm that $I_{TRACKx} < 1mA$, the TRACKx pin(s) maximum guaranteed current, verify that:

$$\frac{V_{TRACK}}{R_{TA} \| R_{TB}} < 1mA$$

Finally, check that the RAMPBUF pin will not be forced to sink more than 3mA when it is at 0V or be forced to source more than 3mA when it is at V_{MASTER}.

$$\frac{V_{TRACK}}{R_{TB1}} + \frac{V_{TRACK}}{R_{TB2}} + \frac{V_{TRACK}}{R_{TB3}} < 3mA \text{ and}$$

$$\frac{V_{MASTER}}{R_{TA1}+R_{TB1}} + \frac{V_{MASTER}}{R_{TA2}+R_{TB2}} + \frac{V_{MASTER}}{R_{TA3}+R_{TB3}} < 3mA$$

Caution with Boost Regulators and Linear Regulators

Note that the LTC2925's tracking cell is not able to control the outputs of all types of power supplies. If it is necessary to control a supply, where the output is not controllable through its feedback node, the series FET can be used to control its output. For example, boost regulators commonly contain an inductor and diode between the input supply and the output supply providing a DC current path when the output voltage falls below the input voltage. Therefore, the LTC2925's tracking cell will not effectively drive the supply's output below the input.

Special caution should be taken when considering the use of linear regulators. Three-terminal linear regulators have a reference voltage that is referred to the output supply rather than to ground. In this case, driving current into the regulator's feedback node will cause its output to rise rather than fall. Even linear regulators that have their reference voltage referred to ground, including low-dropout regulators (LDOs), may be problematic. Linear regulators commonly contain circuitry that prevents driving their outputs below their reference voltage. This may not be obvious from the datasheets, so lab testing is recommended whenever the LTC2925's tracking cell is used to control linear regulators.

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Load Requirements

When the supplies are ramped down quickly, either the load or the supply itself must be capable of sinking enough current to support the ramp rate. For example, if there is a large output capacitance on the supply and a weak resistive load, supplies that do not sink current will have their falling ramp rate limited by the RC time constant of the load and the output capacitance. Figure 19 shows the case when the 2.5V supply does not track the 1.8V and 3.3V supplies near ground.

Start-Up Delays

Often power supplies do not start-up immediatley when their input supplies are applied. If the LTC2925 tries to ramp-up these power supplies as soon as the input supply is present, the start-up of the outputs may be delayed defeating the tracking circuit (Figure 20). Often this delay is intentionally configured by a soft-start capacacitor. This can be remedied either by reducing the soft-start capacitor on the slave supply or by increasing the shutdown timer cycle configured by C_{SDTMR}.

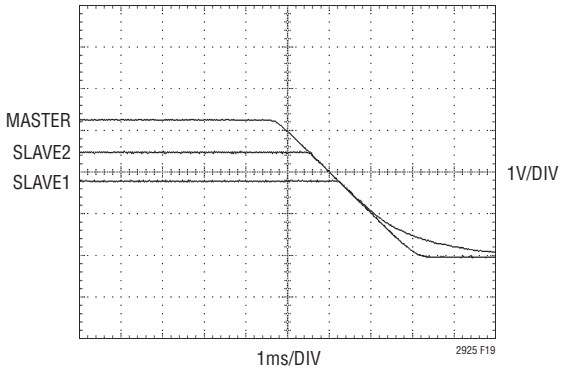


Figure 19. Weak Resistive Load

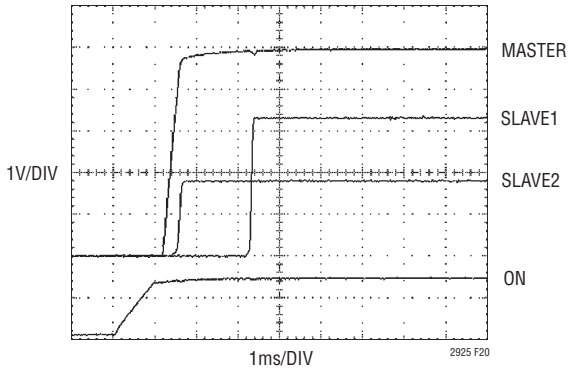


Figure 20. Power Supply Start-Ups Delayed

APPLICATIONS INFORMATION

Layout Considerations

Be sure to place a 0.1µF bypass capacitor as near as possible to the supply pin of the LTC2925.

To minimize the noise on the slave supplies' outputs, keep the traces connecting the FBx pins of the LTC2925 and the feedback nodes of the slave supplies as short as possible. In addition, do not route those traces next to signals with fast transition times. In some circumstances it might be advantageous to add a resistor near the feedback node of the slave supply in series with the FBx pin of the LTC2925.

This resistor must not exceed:

$$R_{SERIES} = \frac{1.6V - V_{FB}}{I_{MAX}} = \left(\frac{1.6V}{V_{FB}} - 1\right)\left(R_{FA} || R_{FB}\right)$$

This resistor is most effective if there is already a capacitor at the feedback node of the slave supply (often a compensation component). Increasing the capacitance on a slave supply's feedback node will further improve the noise immunity, but could affect the stability and transient response of the supply.

For proper circuit breaker operation, Kelvin-sense PCB connections between the sense resistor and the LTC2925's SENSEP and SENSEN pins are strongly recommended. The drawing in Figure 22 illustrates the correct way of making connections between the LTC2925 and the sense resistor. PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor should include good thermal management techniques for optimal sense resistor power dissipation.

The power rating of the sense resistor should accommodate steady-state fault current levels so that the component is not damaged before the circuit breaker trips.

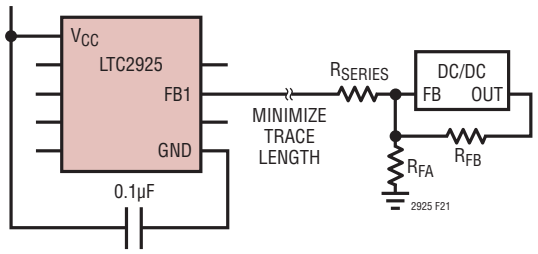


Figure 21. Layout Considerations

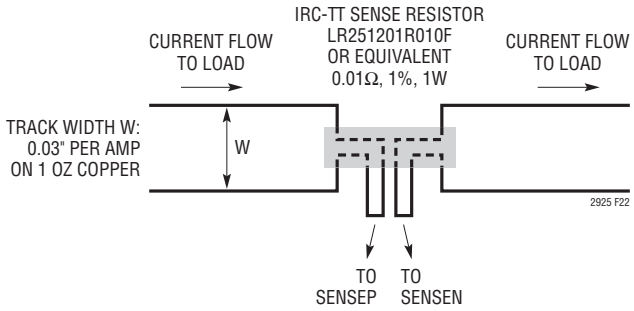
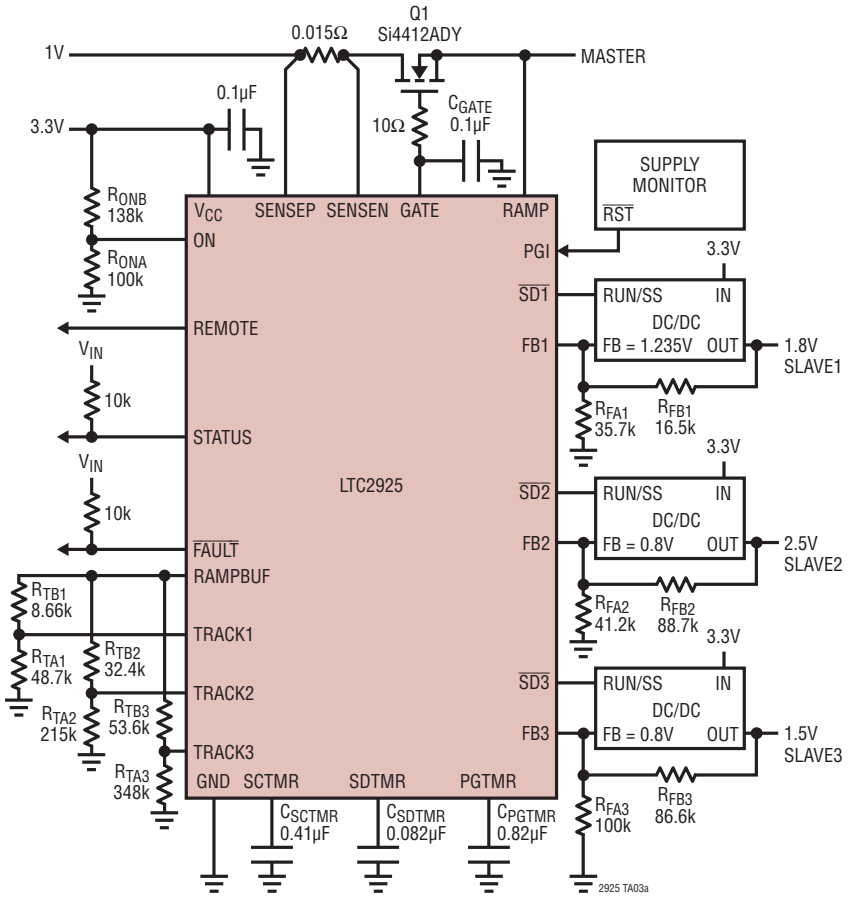


Figure 22. Making PCB Connections to the Sense Resistor

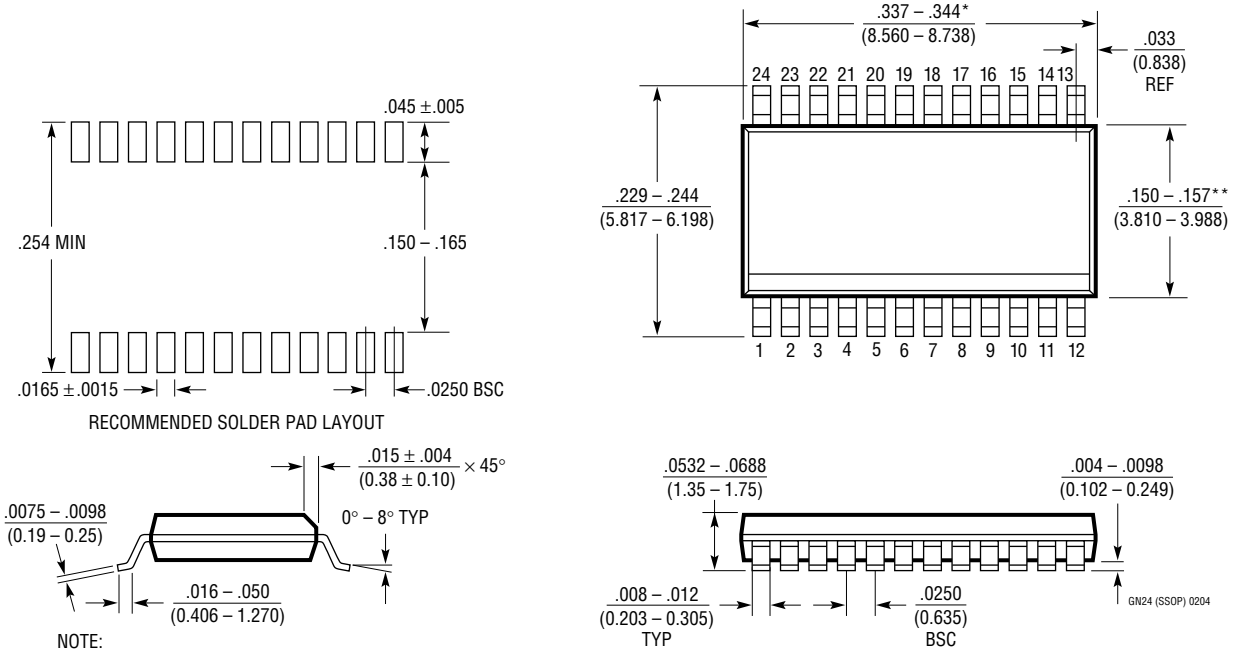
TYPICAL APPLICATION

External FET Controls 1V Supply



PACKAGE DESCRIPTION

GN Package
24-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



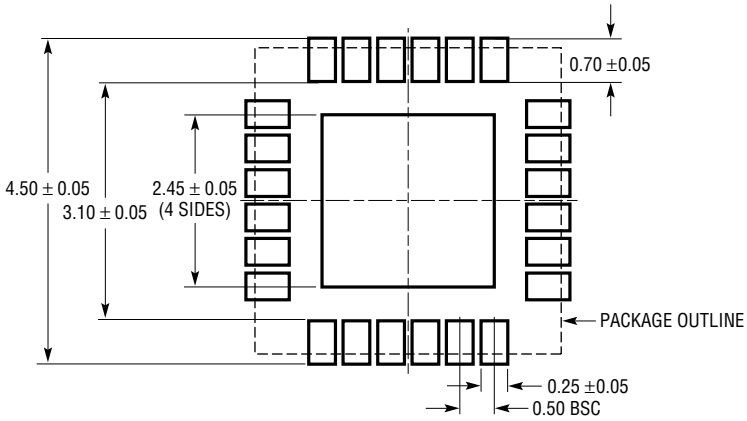
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

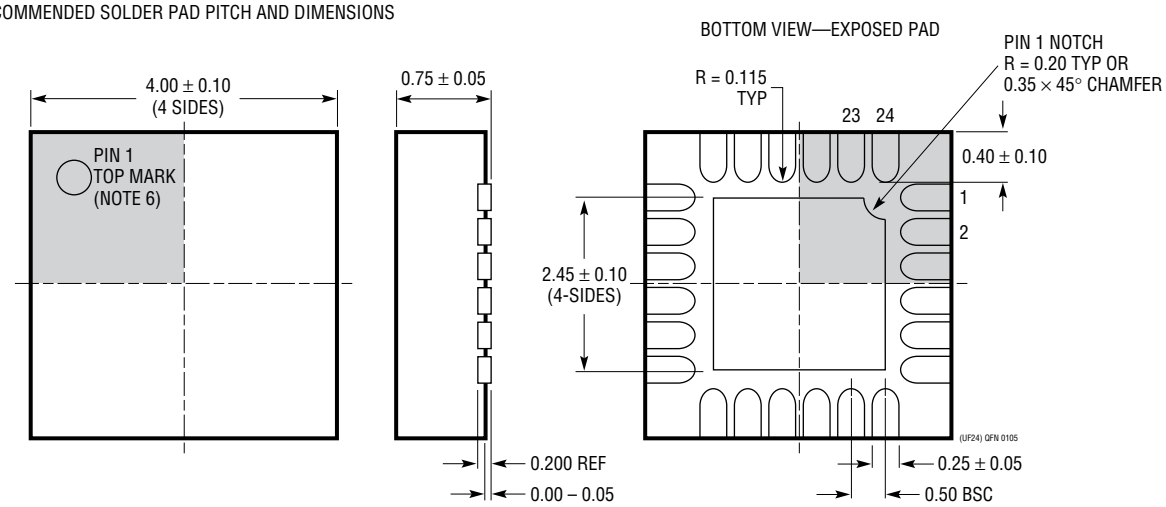
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



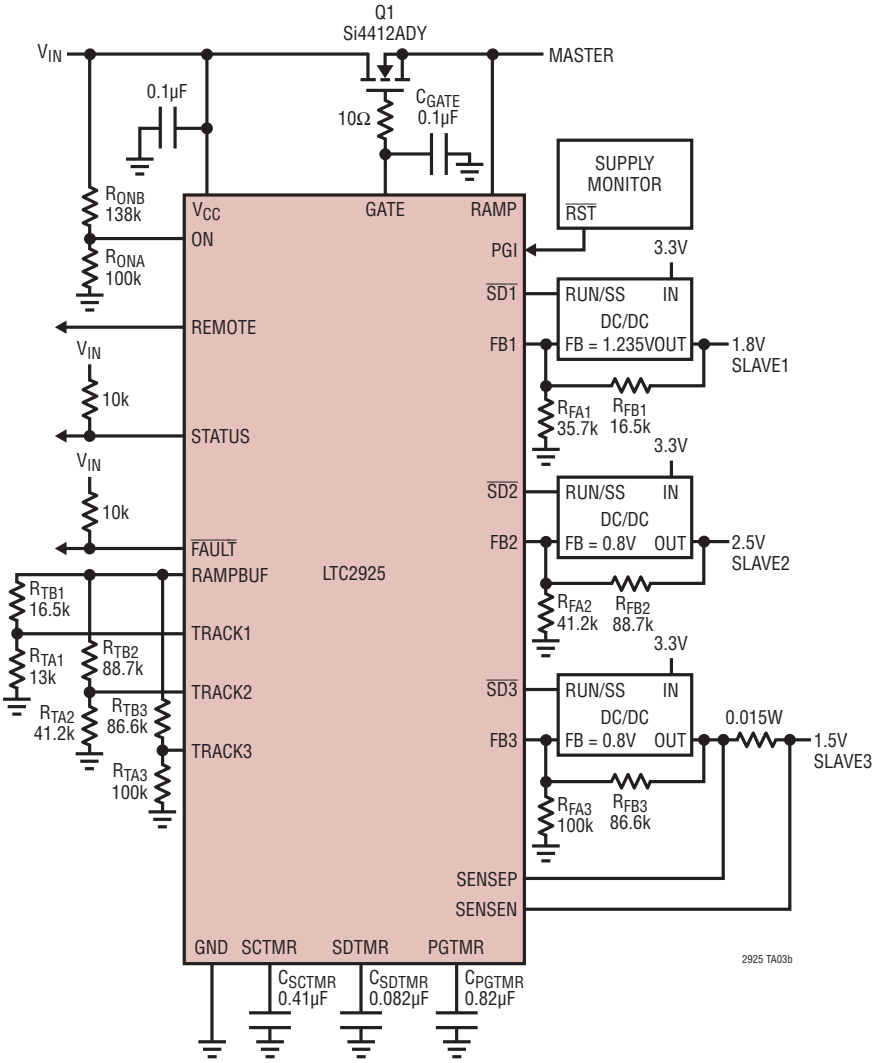
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Electronic Circuit Breaker Monitors Slave Output



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2900	Quad Voltage Monitor in MSOP and DFN	16 User Selectable Combinations, ±1.5% Threshold Accuracy
LTC2901	Quad Voltage Monitor with Watchdog	16 User Selectable Combinations, Adjustable Timers
LTC2902	Quad Voltage Monitor with Adjustable Reset	5%, 2.5%, 10% and 12.5% Selectable Supply Tolerances
LTC2920	Power Supply Margining Controller	Single or Dual, Symmetric/Asymmetric High and Low Margining
LTC2921/LTC2922	Power Supply Tracker with Input Monitors	Includes Three (LTC2921) or Five (LTC2922) Remote Sense Switches
LTC2923	Power Supply Sequencing/Tracking Controller	Controls Two Supplies Without FETs, MSOP-10 and DFN-12 Packages

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