

# UT54ACS193/UT54ACTS193

## Radiation-Hardened Synchronous 4-Bit Up-Down Dual Clock Counters

### FEATURES

- Look-ahead circuitry enhances cascaded counters
- Fully synchronous in count modes
- Parallel asynchronous load for modulo-N count lengths
- Asynchronous clear
- 1.2μ radiation-hardened CMOS
  - Latchup immune
- High speed
- Low power consumption
- Single 5 volt supply
- Available QML Q or V processes
- Flexible package
  - 16-pin DIP
  - 16-lead flatpack

### DESCRIPTION

The UT54ACS193 and the UT54ACTS193 are synchronous 4-bit, binary reversible up-down binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed. Synchronous operation eliminates the output counting spikes normally associated with asynchronous counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of either count input (Up or Down). The direction of the counting is determined by which count input is pulsed while the other count input is high.

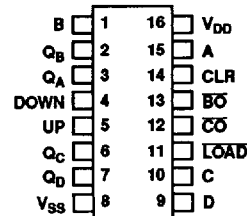
The counters are fully programmable. The outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the count pulses. Asynchronous loading allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided that forces all outputs to the low level when a high level is applied. The clear function is independent of the count and the load inputs.

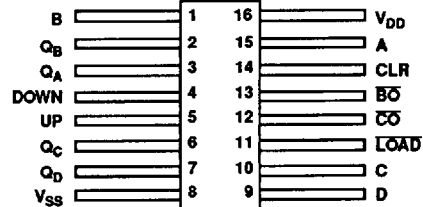
The counter is designed for efficient cascading without the need for external circuitry. The borrow output (BO) produces a low-level pulse while the count is zero and the down input is low. Similarly, the carry output (CO) produces a low-level pulse while the count is maximum

### PINOUTS

16-Pin DIP  
Top View



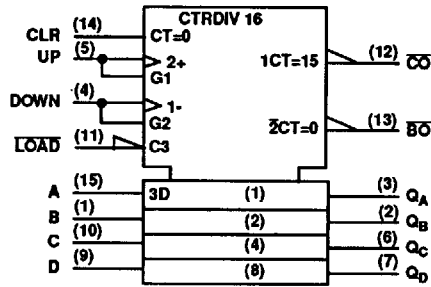
16-Lead Flatpack  
Top View



### FUNCTION TABLE

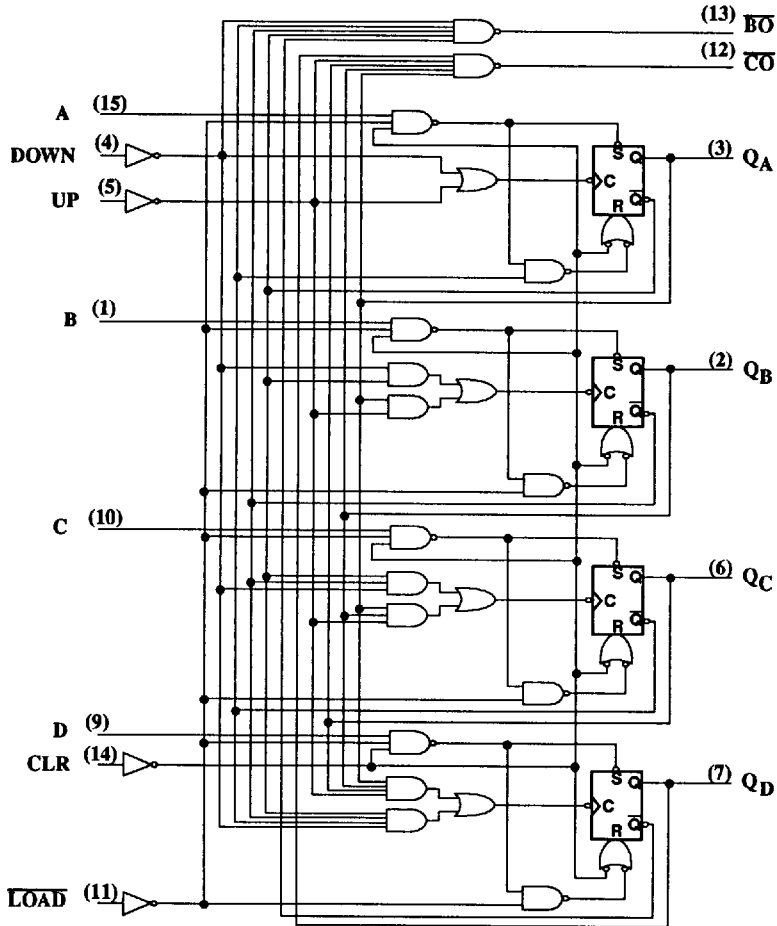
| FUNCTION          | CLOCK UP | CLOCK DOWN | CLR | LOAD |
|-------------------|----------|------------|-----|------|
| Count Up          | ↑        | H          | L   | H    |
| Count Down        | H        | ↑          | L   | H    |
| Reset             | X        | X          | H   | X    |
| Load Preset Input | X        | X          | L   | L    |

LOGIC SYMBOL



Note:  
 1. Logic symbol in accordance with ANSI/IEEE standard 91-1984 and IEC Publication 617-12.

LOGIC DIAGRAM



**RADIATION HARDNESS SPECIFICATIONS <sup>1</sup>**

| PARAMETER                        | LIMIT  | UNITS                   |
|----------------------------------|--------|-------------------------|
| Total Dose                       | 1.0E6  | rads(Si)                |
| SEU & SEL Threshold <sup>2</sup> | 80     | MeV-cm <sup>2</sup> /mg |
| Neutron Fluence                  | 1.0E14 | n/cm <sup>2</sup>       |

**Notes:**

1. Logic will not latchup during radiation exposure within the limits defined in the table.
2. Device storage elements are immune to SEU affects.

**ABSOLUTE MAXIMUM RATINGS**

| SYMBOL           | PARAMETER                              | LIMIT                      | UNITS |
|------------------|--|----------------------------|-------|
| V <sub>DD</sub>  | Supply voltage                         | -0.3 to 7.0                | V     |
| V <sub>IO</sub>  | Voltage any pin                        | -.3 to V <sub>DD</sub> +.3 | V     |
| T <sub>STG</sub> | Storage Temperature range              | -65 to +150                | °C    |
| T <sub>J</sub>   | Maximum junction temperature           | +175                       | °C    |
| T <sub>LS</sub>  | Lead temperature (soldering 5 seconds) | +300                       | °C    |
| θ <sub>JC</sub>  | Thermal resistance junction to case    | 20                         | °C/W  |
| I <sub>I</sub>   | DC input current                       | ±10                        | mA    |
| P <sub>D</sub>   | Maximum power dissipation              | 1                          | W     |

**Note:**

1. Stresses outside the listed absolute maximum ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions beyond limits indicated in the operational sections is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

| SYMBOL          | PARAMETER             | LIMIT                | UNITS |
|-----------------|-----------------------|----------------------|-------|
| V <sub>DD</sub> | Supply voltage        | 4.5 to 5.5           | V     |
| V <sub>IN</sub> | Input voltage any pin | 0 to V <sub>DD</sub> | V     |
| T <sub>C</sub>  | Temperature range     | -55 to + 125         | °C    |

**DC ELECTRICAL CHARACTERISTICS <sup>7</sup>**

( $V_{DD} = 5.0V \pm 10\%$ ;  $V_{SS} = 0V$  <sup>6</sup>,  $-55^{\circ}C < T_C < +125^{\circ}C$ )

| SYMBOL      | PARAMETER   | CONDITION                                 | MIN                            | MAX                | UNIT       |
|-------------|---|---|--------------------------------|--------------------|------------|
| $V_{IL}$    | Low-level input voltage <sup>1</sup><br>ACTS<br>ACS     |   |                                | 0.8<br>.3 $V_{DD}$ | V          |
| $V_{IH}$    | High-level input voltage <sup>1</sup><br>ACTS<br>ACS    |   | .5 $V_{DD}$<br>.7 $V_{DD}$     |                    | V          |
| $I_{IN}$    | Input leakage current<br>ACTS/ACS                       | $V_{IN} = V_{DD}$ or $V_{SS}$             | -1                             | 1                  | $\mu A$    |
| $V_{OL}$    | Low-level output voltage <sup>3</sup><br>ACTS<br>ACS    | $I_{OL} = 8.0mA$<br>$I_{OL} = 100\mu A$   |                                | 0.40<br>0.25       | V          |
| $V_{OH}$    | High-level output voltage <sup>3</sup><br>ACTS<br>ACS   | $I_{OH} = -8.0mA$<br>$I_{OH} = -100\mu A$ | .7 $V_{DD}$<br>$V_{DD} - 0.25$ |                    | V          |
| $I_{OS}$    | Short-circuit output current <sup>2,4</sup><br>ACTS/ACS | $V_O = V_{DD}$ and $V_{SS}$               | -200                           | 200                | mA         |
| $P_{total}$ | Power dissipation <sup>8,9</sup>                        | $C_L = 50pF$                              |                                | 2.1                | mW/<br>MHz |
| $I_{DDQ}$   | Quiescent Supply Current                                | $V_{DD} = 5.5V$                           |                                | 10                 | $\mu A$    |
| $C_{IN}$    | Input capacitance <sup>5</sup>                          | $f = 1MHz @ 0V$                           |                                | 15                 | pF         |
| $C_{OUT}$   | Output capacitance <sup>5</sup>                         | $f = 1MHz @ 0V$                           |                                | 15                 | pF         |

**Notes:**

- Functional tests are conducted in accordance with MIL-STD-883 with the following input test conditions:  $V_{IH} = V_{IH(min)} + 20\%$ ,  $-0\%$ ;  $V_{IL} = V_{IL(max)} + 0\%$ ,  $-50\%$ , as specified herein, for TTL, CMOS, or Schmitt compatible inputs. Devices may be tested using any input voltage within the above specified range, but are guaranteed to  $V_{IH(min)}$  and  $V_{IL(max)}$ .
- Supplied as a design limit but not guaranteed or tested.
- Per MIL-M-38510, for current density  $\leq 5.0E5$  amps/cm<sup>2</sup>, the maximum product of load capacitance (per output buffer) times frequency should not exceed 3,765 pF MHz.
- Not more than one output may be shorted at a time for maximum duration of one second.
- Capacitance measured for initial qualification and when design changes may affect the value. Capacitance is measured between the designated terminal and  $V_{SS}$  at frequency of 1MHz and a signal amplitude of 50mV rms maximum.
- Maximum allowable relative shift equals 50mV.
- All specifications valid for radiation dose  $\leq 1E6$  rads(Si).
- Power does not include power contribution of any TTL output sink current.
- Power dissipation specified per switching output.

**AC ELECTRICAL CHARACTERISTICS <sup>2</sup>**

( $V_{DD} = 5.0V \pm 10\%$ ;  $V_{SS} = 0V$  <sup>1</sup>,  $-55^{\circ}C < T_C < +125^{\circ}C$ )

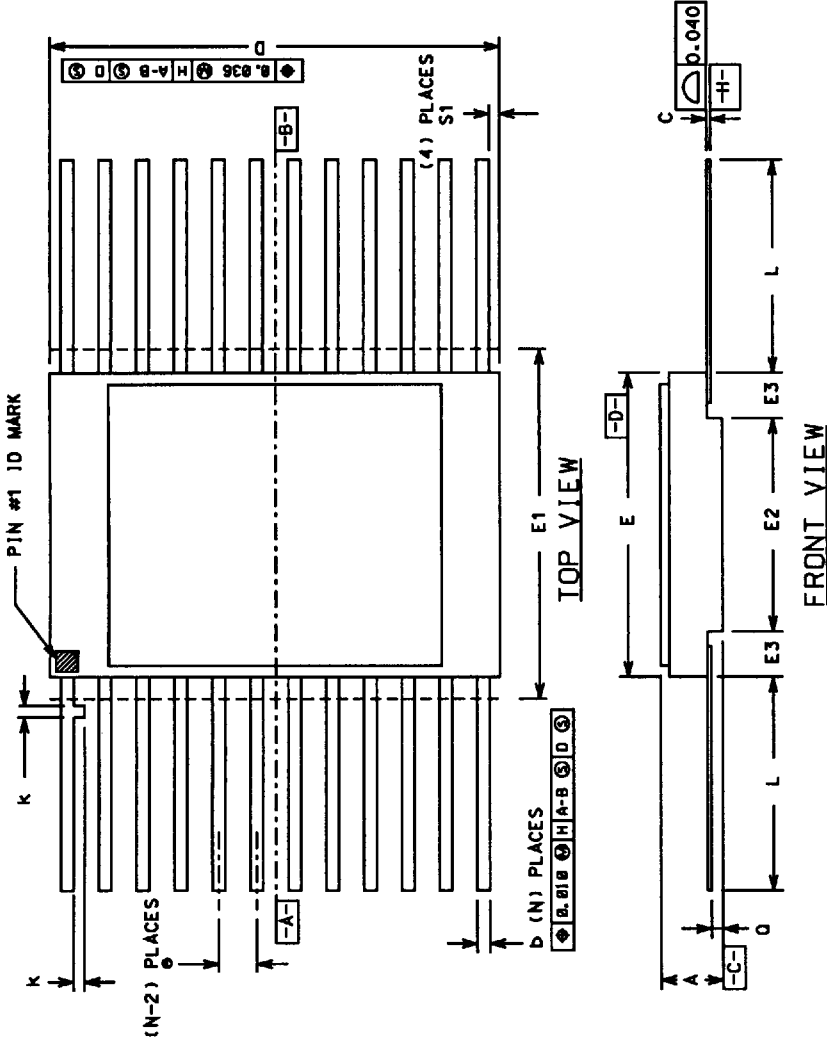
| SYMBOL           | PARAMETER  | MINIMUM | MAXIMUM | UNIT |
|------------------|--|---------|---------|------|
| t <sub>PLH</sub> | UP to Q <sub>n</sub>   | 2       | 20      | ns   |
| t <sub>PHL</sub> | UP to Q <sub>n</sub>   | 2       | 24      | ns   |
| t <sub>PLH</sub> | UP to $\overline{CO}$  | 2       | 13      | ns   |
| t <sub>PHL</sub> | UP to $\overline{CO}$  | 2       | 16      | ns   |
| t <sub>PLH</sub> | DOWN to $\overline{BO}$  | 2       | 13      | ns   |
| t <sub>PHL</sub> | DOWN to $\overline{BO}$  | 2       | 16      | ns   |
| t <sub>PLH</sub> | DOWN to Q <sub>n</sub>   | 2       | 20      | ns   |
| t <sub>PHL</sub> | DOWN to Q <sub>n</sub>   | 2       | 24      | ns   |
| t <sub>PLH</sub> | $\overline{LOAD}$ to Q <sub>n</sub>  | 2       | 22      | ns   |
| t <sub>PHL</sub> | $\overline{LOAD}$ to Q <sub>n</sub>  | 2       | 23      | ns   |
| t <sub>PHL</sub> | CLR to Q <sub>n</sub>  | 2       | 22      | ns   |
| f <sub>MAX</sub> | Maximum clock frequency  |         | 56      | MHz  |
| t <sub>SU</sub>  | Setup time before UP or DOWN ↑<br>LOAD inactive<br>CLR inactive                                | 3       |         | ns   |
|                  | A, B, C, D setup time before $\overline{LOAD}$ ↑   | 6       |         |      |
| t <sub>H</sub>   | UP high hold time after DOWN ↑<br>DOWN high hold time after UP ↑                               | 20      |         | ns   |
|                  | A, B, C, D hold time after $\overline{LOAD}$ ↑   | 2       |         |      |
| t <sub>w</sub>   | Minimum pulse width<br>UP high or low<br>DOWN high or low<br>$\overline{LOAD}$ low<br>CLR high | 9       |         | ns   |

**Notes:**

1. Maximum allowable relative shift equals 50mV.
2. All specifications valid for radiation dose ≤ 1E6 rads(Si).



# Flatpack Packages



| PKG CONFIG | LEAD COUNT | MIL-STD 1835 DWG CONF B | DIMENSION SYMBOLS |       |       |       |       |       |     |     |       |       |       |       |       |       |       |
|------------|------------|-------------------------|-------------------|-------|-------|-------|-------|-------|-----|-----|-------|-------|-------|-------|-------|-------|-------|
|            |            |                         | A                 | b     | c     | D     | E     | E1    | E2  | E3  | e     | k     | L     | o     | S1    |       |       |
| -03        | 14         | F-2A                    | 0.115             | 0.022 | 0.009 | 0.390 | 0.260 | 0.290 | --- | --- | 0.130 | 0.030 | 0.050 | 0.015 | 0.370 | 0.045 | ---   |
|            |            |                         | 0.045             | 0.015 | 0.004 | ---   | 0.235 | ---   | --- | --- | ---   | ---   | BSC   | 0.008 | 0.270 | 0.026 | 0.005 |
| -04        | 16         | F-5A                    | 0.115             | 0.022 | 0.009 | 0.440 | 0.285 | 0.315 | --- | --- | 0.130 | 0.030 | 0.050 | 0.015 | 0.370 | 0.045 | ---   |
|            |            |                         | 0.045             | 0.015 | 0.004 | ---   | 0.245 | ---   | --- | --- | ---   | ---   | BSC   | 0.008 | 0.250 | 0.026 | 0.005 |
| -05        | 20         | F-9A                    | 0.115             | 0.022 | 0.009 | 0.540 | 0.300 | 0.330 | --- | --- | 0.130 | 0.030 | 0.050 | 0.015 | 0.370 | 0.045 | ---   |
|            |            |                         | 0.045             | 0.015 | 0.004 | ---   | 0.245 | ---   | --- | --- | ---   | ---   | BSC   | 0.008 | 0.250 | 0.026 | 0.000 |