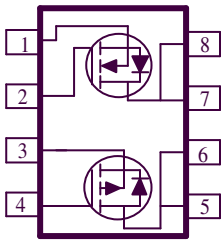
P & N-Channel 20-V (D-S) MOSFET

These miniature surface mount MOSFETs utilize a high cell density trench process to provide low $r_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ m(Ω)	I_D (A)
20	40 @ V_{GS} = 2.5V	6.0
	31 @ V_{GS} = 4.5V	6.9
-20	80 @ V_{GS} = -2.5V	-4.2
	52 @ V_{GS} = -4.5V	-5.2

- Low $r_{DS(on)}$ provides higher efficiency and extends battery life
- Low thermal impedance copper leadframe SOIC-8 saves board space
- Fast switching speed
- High performance trench technology



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C UNLESS OTHERWISE NOTED)					
Parameter		**Symbol**	**N-Channel**	**P-Channel**	**Units**
Drain-Source Voltage		V_{DS}	20	-20	V
Gate-Source Voltage		V_{GS}	±8	±8	
Continuous Drain Current[a]	T_A=25°C	I_D	6.9	-5.2	A
	T_A=70°C		5.4	-6.8	
Pulsed Drain Current[b]		I_{DM}	20	-20	
Continuous Source Current (Diode Conduction)[a]		I_S	1.3	-1.3	A
Power Dissipation[a]	T_A=25°C	P_D	2.1	2.1	W
	T_A=70°C		1.3	1.3	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS				
Parameter		**Symbol**	**Maximum**	**Units**
Maximum Junction-to-Ambient[a]	t <= 10 sec	$R_{\theta JA}$	62.5	°C/W
	Steady-State		110	°C/W

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

b. Pulse width limited by maximum junction temperature

SPECIFICATIONS (T_A = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Conditions	Limits				Unit
			Ch	Min	Typ	Max	
Static							
Gate-Threshold Voltage	$V_{GS(th)}$	V_{GS} = V_{DS}, I_D = 250 uA	N	0.4			V
		V_{GS} = V_{DS}, I_D = -250 uA	P	-0.4			
Gate-Body Leakage	I_{GSS}	V_{GS} = -8 V, V_{DS} = 0 V	P			±100	nA
		V_{GS} = 8 V, V_{DS} = 0 V	N			±100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -16 V, V_{GS} = 0 V	P			-1	uA
		V_{DS} = 16 V, V_{GS} = 0 V	N			1	
On-State Drain Current[A]	$I_{D(on)}$	V_{DS} = 5 V, V_{GS} = 4.5 V	N	20			A
		V_{DS} = -5 V, V_{GS} = -4.5 V	P	-20			
Drain-Source On-Resistance[A]	$r_{DS(on)}$	VGS = 4.5 V, I_D = 6.9 A	N			31	mΩ
		VGS = 2.5 V, I_D = 6 A				40	
		VGS = -4.5 V, I_D = -5.2 A	P			52	
		VGS = -2.5 V, I_D = -4.2 A				80	
Forward Tranconductance[A]	g_{fs}	V_{DS} = 15 V, I_D = 6.9 A	N		25		S
		V_{DS} = -15 V, I_D = -5.2 A	P		10		
Dynamic							
Total Gate Charge	Q_g	N-Channel V_{DS}=15V, V_{GS}=4.5V, I_D=6.9A P-Channel V_{DS}=-15V, V_{GS}=-4.5V, I_D=-5.2A	N		6.0		nC
			P		25		
Gate-Source Charge	Q_{gs}		N		1.0		
			P		2.4		
Gate-Drain Charge	Q_{gd}		N		1.5		
			P		3.9		
Turn-On Delay Time	$t_{d(on)}$	N-Chaneel V_{DD}=15V, V_{GS}=4.5V, I_D=1A , R_{GEN}=6Ω, P-Channel V_{DD}=-15V, V_{GS}=-4.5V, I_D=-1A R_{GEN}=6Ω	N		7.4		nS
			P		7.6		
Rise Time	t_r		N		4		
			P		6.8		
Turn-Off Delay Time	$t_{d(off)}$		N		22.2		
			P		33.6		
Fall-Time	t_f		N		3.6		
			P		23.2		

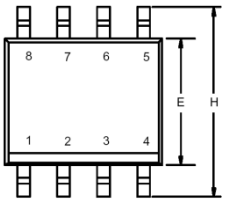
Notes

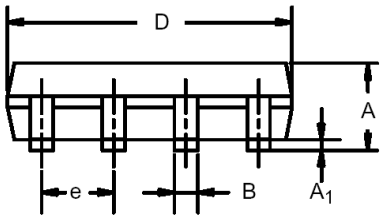
a. Pulse test: PW <= 300us duty cycle <= 2%.

b. Guaranteed by design, not subject to production testing.

Package Information

SO-8: 8LEAD





Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°