Agilent HPFC-5200 Tachyon XL2 High-Performance Fibre Channel IC
Product Overview

Description
The Tachyon XL2 (HPFC-5200) is a high-performance PCI-native multi-gigabit Fibre Channel (FC) controller for host bus adapters and embedded subsystems.

Tachyon Architecture
XL2 advances with the Tachyon architecture—a complete hardware-based design in a single chip FC solution. Numerous independent functional blocks concurrently process inbound data, outbound data, control and commands in hardware. This results in the lowest latency and the highest level of performance available today.

Performance
- 2.125 and 1.0625 gigabits/sec (400 and 200 MBytes/sec)
- Processes up to 32,768 concurrent SCSI I/Os
- Processes up to 8,192 commands in the I/O request queue
- One or less interrupts per initiator exchange
- PCI burst transfer rate of 528 MBytes/sec (64-bit, 66 MHz)

Features
- One-chip PCI-to-FC solution
- 32-bit/64-bit, 0-66 MHz PCI backplane
- 2-gigabit / 1-gigabit integrated transceiver and external SERDES interface (High Speed Parallel Interface)
- No external SRAM required
- FC-AL-2 compliant
- BIOS support
- Supports inbound frame buffers for eight 2 KByte (payload) frames
- Full 8-bit data parity protection
- Programmable interrupt delay reduces interrupts
- Ability to send High Priority frames
- Hardware support for Class 3 and Class 2 (ACK_0 and ACK_1 model)
- Enhanced SCSI (FCP) hardware assists
- Secondary Port Interface for control (optional)
- Supports all FC topologies (point-to-point, loop, and fabric)
- Multiple outbound and inbound sequence support
- Tachyon Product Software Developer's Kit (TSDK) available
- SAN interoperability

Applications
- High-performance host bus adapters
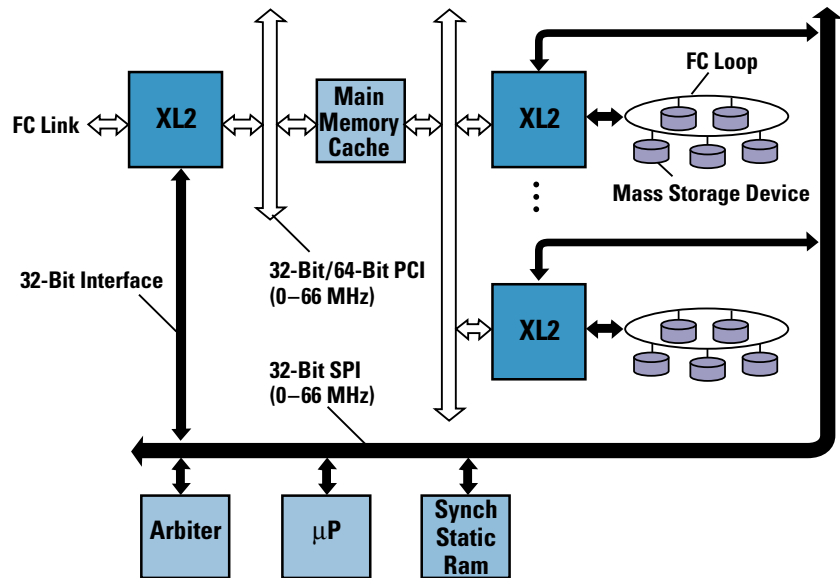- SCSI bridge
- Embedded subsystems
- Disk arrays

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Separate Data and Control Application

The figure to the right shows XL2 in an optional high-performance configuration that provides total separation of data and control paths.

In this example, XL2 chips share a common 32-bit bus (SPI) with a local microprocessor (subsystem processor) and memory.

The subsystem processor can access control structures located in the shared synchronous static RAM as well as the XL2 register sets. Data and control commands move concurrently within XL2.

FC Link — XL2 — Main Memory Cache — XL2 — FC Loop / Mass Storage Device — XL2

32-Bit Interface

32-Bit/64-Bit PCI (0–66 MHz)

32-Bit SPI (0–66 MHz)

Arbiter — μP — Synch Static Ram

Specifications

Fibre Channel Operation

- 2.125 and 1.0625 gigabit/sec (400 and 200 MByte/sec) full-duplex support
- Frame payload size — up to 2048 bytes
- Point-to-point, loop, and fabric topologies
- Class 3 and Class 2 (ACK_0 and ACK_1 model)
- Loop Map, Loop Directed Reset, Loop Broadcast
- Compliance to FC-PH, FC-AL, FC-AL2, FC-PLDA, FC-FLA, FCP, HSPI Profile
- FC-MI Level 1 (SAN interoperability)

FCP (SCSI) Features

- Up to 32,768 maximum concurrent I/Os
- Up to 8192 commands in the I/O request queue
- 1 or less interrupts per exchange (initiator mode)
- Simultaneous initiator and target mode
- Byte level addressability on both inbound and outbound data buffers
- Simplified error notification and recovery

PCI

- Compliance to PCI Local Bus Specification, Revision 2.2
- 32-bit or 64-bit selectable, 0-66 MHz PCI backplane
- Burst transfer rate of 528 MBytes/sec (64-bit, 66 MHz)
- Configurable to optimize performance
- Dual address cycle support
- Compliance to ACPI Specification
- Hot plug PCI capable

Other

- 16-entry inbound cache for low latency context switching / restore
- Parity protection on all data paths at byte level
- Synchronous SRAM memory support (up to 2 MBytes)
- Flash ROM support for Boot BIOS and SVID
- 32-bit, 66 MHz Secondary Port Interface (SPI)
- For test and debug: JTAG and full internal scan supported; link status pins; and user definable signal pins
- 388-pin Enhanced Plastic Ball Grid Array (EPBGA) package for maximum signal integrity
- Compliance with Hardware Design Guide for Microsoft Windows NT Server, Version 2.0

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