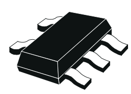
LK112S SERIES

LOW NOISE LOW DROP VOLTAGE REGULATOR WITH SHUTDOWN FUNCTION

- OUTPUT CURRENT UP TO 200mA
- LOW DROPOUT VOLTAGE (500mV MAX AT I_{OUT}=200mA)
- VERY LOW QUIESCENT CURRENT: 0.1µA IN OFF MODE AND MAX 250µA IN ON MODE AT I_{OUT}=0mA
- LOW OUTPUT NOISE: TYP 30µV AT I_{OUT}=60mA AND 10Hz<f<80KHz
- WIDE RANGE OF OUTPUT VOLTAGES
- INTERNAL CURRENT AND THERMAL LIMIT
- V_{OUT} TOLERANCE ± 2% (AT 25°C)



SOT23-5L

DESCRIPTION

The LK112S is a low dropout linear regulator with a built in electronic switch. The internal switch can be controlled by TTL or CMOS logic levels. The device is ON state when the control pin is pulled to a logic high level. An external capacitor can be used connected to the noise bypass pin to lower the output noise level to 30µV_{rms}. An internal PNP pass transistor is used to achieve a low dropout voltage.

The LK112S has a very low quiescent current in ON MODE while in OFF MODE the Iq is reduced down to 100nA max. The internal thermal shutdown circuitry limits the junction temperature to below 150°C. The load current is internally monitored and the device will shutdown in the presence of a short circuit or overcurrent condition at the output.

Figure 1: Schematic Diagram

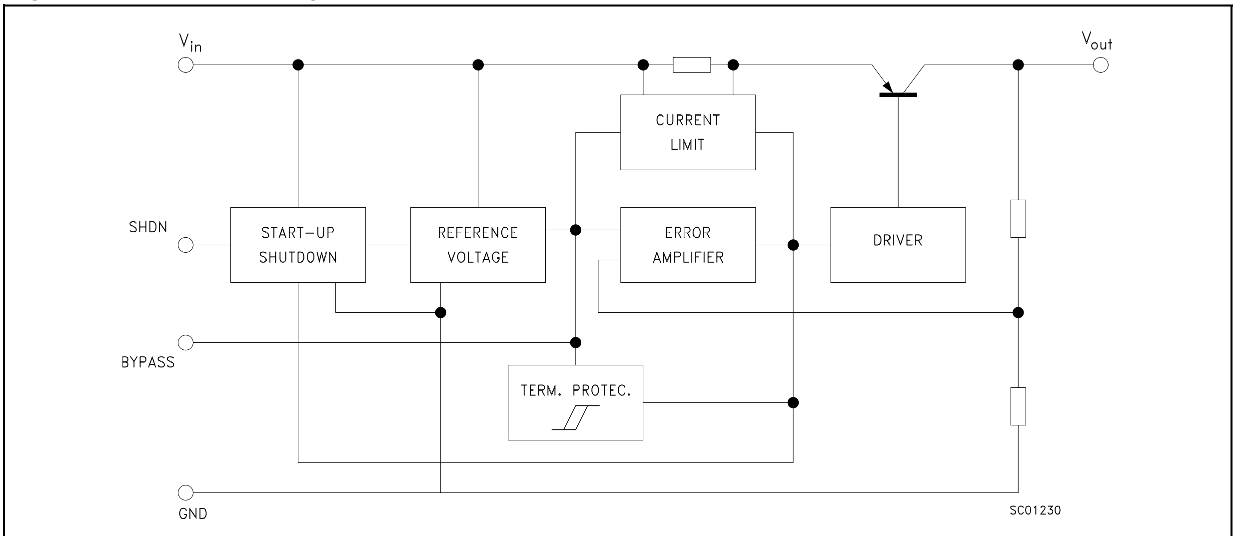


Table 1: Order Codes

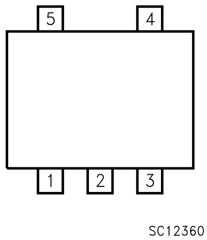
Part Number	Output Voltage	V_{OUT} Min	V_{OUT} Max	Test Voltage
LK112SM13TR	1.3V	1.24V	1.36V	2.4V
LK112SM14TR (*)	1.4V	1.34V	1.46V	2.4V
LK112SM15TR	1.5V	1.44V	1.56V	2.4V
LK112SM16TR	1.6V	1.54V	1.66V	2.4V
LK112SM17TR (*)	1.7V	1.64V	1.76V	2.4V
LK112SM18TR	1.8V	1.74V	1.86V	2.4V
LK112SM19TR (*)	1.9V	1.84V	1.96V	2.4V
LK112SM20TR (*)	2.0V	1.94V	2.06V	3.0V
LK112SM21TR	2.1V	2.04V	2.16V	3.1V
LK112SM22TR (*)	2.2V	2.14V	2.26V	3.2V
LK112SM23TR (*)	2.3V	2.24V	2.36V	3.3V
LK112SM24TR (*)	2.4V	2.34V	2.46V	3.4V
LK112SM25TR	2.5V	2.44V	2.56V	3.5V
LK112SM26TR (*)	2.6V	2.54V	2.66V	3.6V
LK112SM27TR (*)	2.7V	2.64V	2.76V	3.7V
LK112SM28TR	2.8V	2.74V	2.86V	3.8V
LK112SM29TR (*)	2.9V	2.84V	2.96V	3.9V
LK112SM30TR	3.0V	2.94V	3.06V	4.0V
LK112SM31TR (*)	3.1V	3.04V	3.16V	4.1V
LK112SM32TR	3.2V	3.14V	3.26V	4.2V
LK112SM33TR	3.3V	3.24V	3.36V	4.3V
LK112SM34TR (*)	3.4V	3.335V	3.465V	4.4V
LK112SM35TR (*)	3.5V	3.435V	3.565V	4.5V
LK112SM36TR	3.6V	3.535V	3.655V	4.6V
LK112SM37TR (*)	3.7V	3.630V	3.770V	4.7V
LK112SM38TR	3.8V	3.725V	3.875V	4.8V
LK112SM39TR (*)	3.9V	3.825V	3.975V	4.9V
LK112SM40TR	4.0V	3.920V	4.080V	5.0V
LK112SM41TR (*)	4.1V	4.020V	4.180V	5.1V
LK112SM42TR (*)	4.2V	4.120V	4.280V	5.2V
LK112SM43TR (*)	4.3V	4.215V	4.385V	5.3V
LK112SM44TR (*)	4.4V	4.315V	4.485V	5.4V
LK112SM45TR (*)	4.5V	4.410V	4.590V	5.5V
LK112SM46TR (*)	4.6V	4.510V	4.690V	5.6V
LK112SM47TR	4.7V	4.605V	4.795V	5.7V
LK112SM48TR (*)	4.8V	4.705V	4.895V	5.8V
LK112SM49TR (*)	4.9V	4.800V	5.000V	5.9V
LK112SM50TR	5.0V	4.900V	5.100V	6.0V
LK112SM55TR	5.5V	5.390V	5.610V	6.5V
LK112M60TR	6.0V	5.880V	6.120V	7.0V
LK112SM80TR	8.0V	7.840V	8.160V	9.0V

(*) Available on request

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_I	DC Input Voltage	16	V
V_{SHDN}	Shutdown Input Voltage	16	V
I_O	Output Current	Internally limited	
T_{stg}	Storage Temperature Range	-55 to +150	°C
T_{op}	Operating Junction Temperature Range	-30 to +80	°C

Figure 2: Pin Connection (top view)



SOT23-5L

Table 3: Pin Description

Pin N°	Symbol	Name and Function
1	SHDN	Shutdown Input: Disables the regulator when is connected to GND or to positive voltage less than 0.6V
2	GND	Ground Pin: Internally connected to the die attach flag to decrease the total thermal resistance and increase the package ability to dissipate power.
3	Bypass	Bypass Pin: Bypass with 0.1µF to improve the V_{REF} thermal noise performances.
4	OUT	Output Port
5	IN	Input Port

Table 4: Electrical Characteristics For LK112S (T_j = 25°C, V_{IN}=V_{OUT}+1V (see Note 1), I_{OUT}=0mA, V_{SHDN}=1.8V, C_I = 1 µF, C_O = 2.2µF, C_{BYPASS} = 0.1µF unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_d	Quiescent Current	ON MODE (except I_{SHDN})		175	250	µA
		OFF MODE V_I = 8V V_{SHDN} = 0V		0	0.1	µA
V_O	Output Voltage	I_O = 30mA		(see table)		
ΔV_O	Line Regulation	V_I = V_O+1V to V_O+6V, $V_O \leq 5.6V$		0.7	20	mV
		V_I = V_O+1V to V_O+6V, V_O > 5.6V		0.8	40	mV
ΔV_O	Load Regulation	I_O = 1 to 60mA		15	30	mV
		I_O = 1 to 200mA		30	90	mV
V_d	Dropout Voltage	I_O = 60 mA (see Note 2)		0.17	0.24	V
		I_O = 200 mA (see Note 2)		0.35	0.5	V
I_{SC}	Short Circuit Current		200			mA
SVR	Supply Voltage Rejection	V_I = V_O+1.5V C_{BYP} = 0.1µF C_O = 10µF f = 400Hz I_O = 30mA		55		dB
eN	Output Noise Voltage	B= 10Hz to 80KHz C_{BYP} = 0.1µF C_O = 10µF V_I = V_O+1.5V, I_O = 60mA		30		µVrms
I_{SHDN}	Shutdown Input Current	V_{SHDN} = 1.8V Output ON		12	35	µA
V_{SHDN}	Shutdown Input Logic	Output ON Output OFF	1.8		 0.6	V V
$\Delta V_O/T_j$	Output Voltage Temperature Coefficient	I_O = 10mA		0.09		mV/°C

Note 1: for version with output voltage less than 2V V_{IN}=2.4V
Note 2: only for version with output voltage more than 2.1V

TYPICAL CHARACTERISTICS (unless otherwise specified T_j = 25°C, C_I=1µF, C_O=2.2µF, C_{BYP}=100nF)

Figure 3: Output Voltage vs Temperature

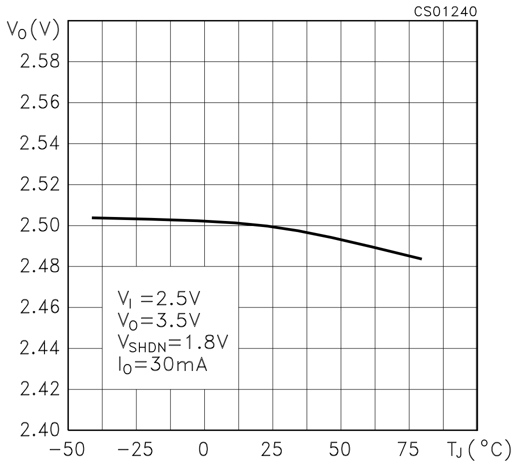


Figure 6: Load Regulation vs Temperature

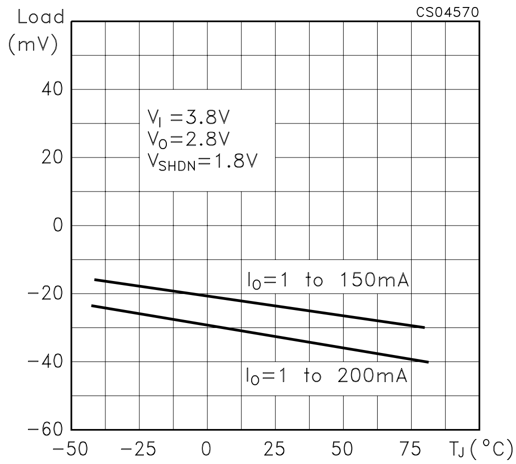


Figure 4: Output Voltage vs Temperature

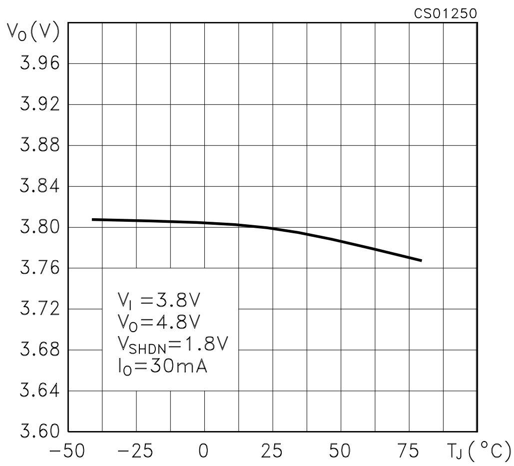


Figure 7: Dropout Voltage vs Temperature

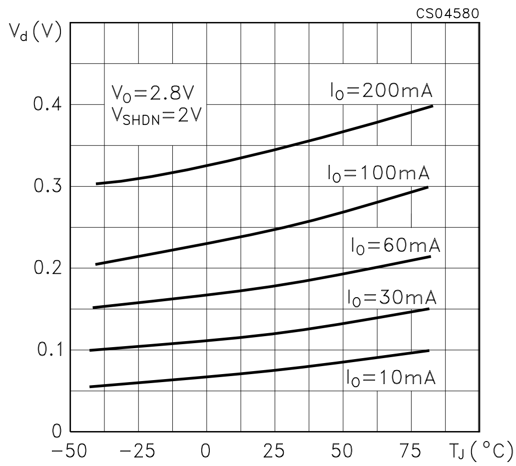


Figure 5: Line Regulation vs Temperature

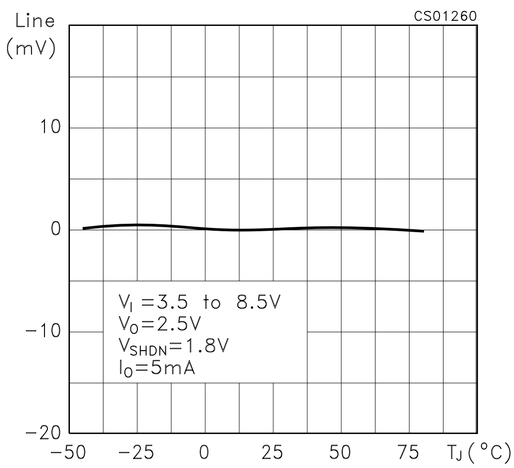


Figure 8: Short Circuit Current vs Dropout Voltage

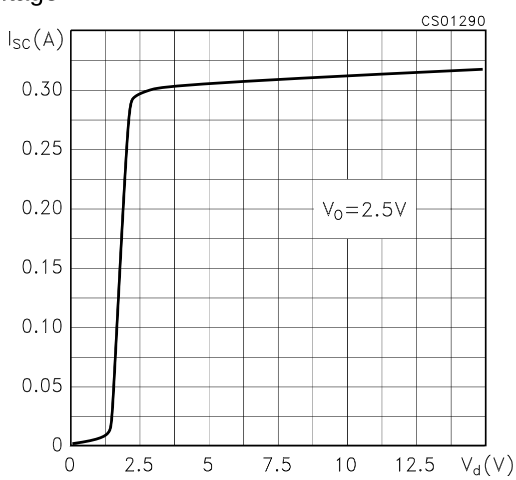


Figure 9: Output Voltage vs Input Voltage

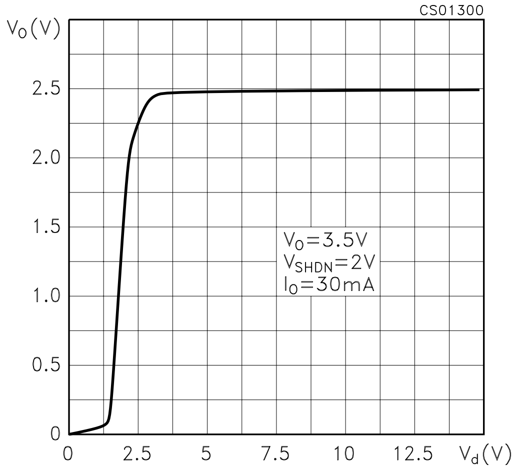


Figure 10: Shutdown Voltage vs Temperature

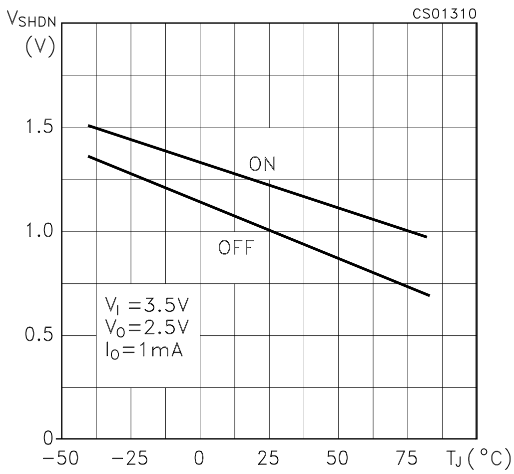


Figure 11: Shutdown Current vs Shutdown Voltage

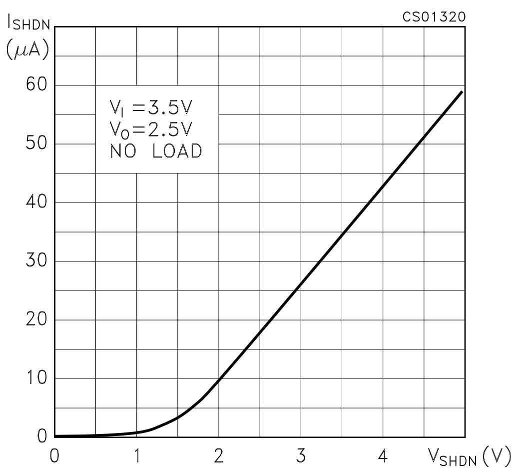


Figure 12: Supply Voltage Rejection vs Temperature

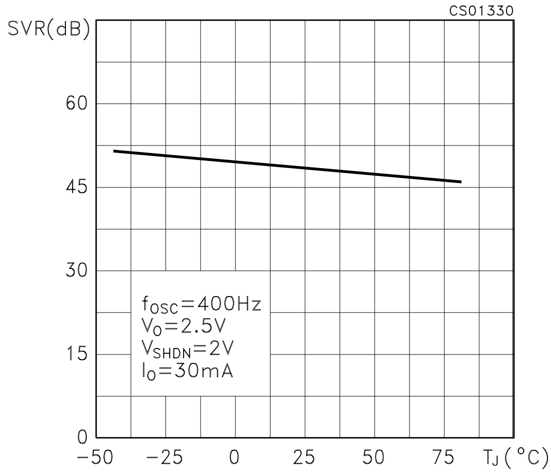


Figure 13: Supply Voltage Rejection vs Output Current

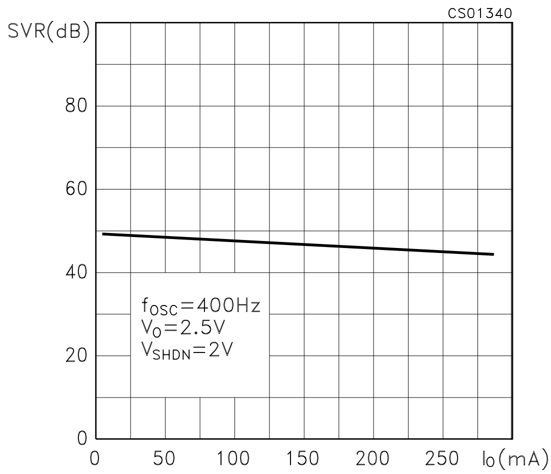


Figure 14: Supply Voltage Rejection vs Frequency

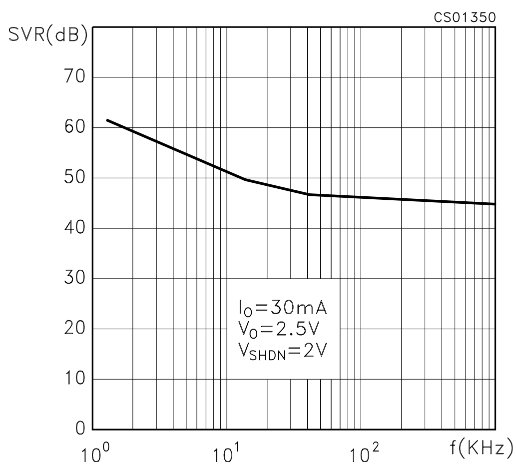


Figure 15: Supply Voltage Rejection vs Temperature

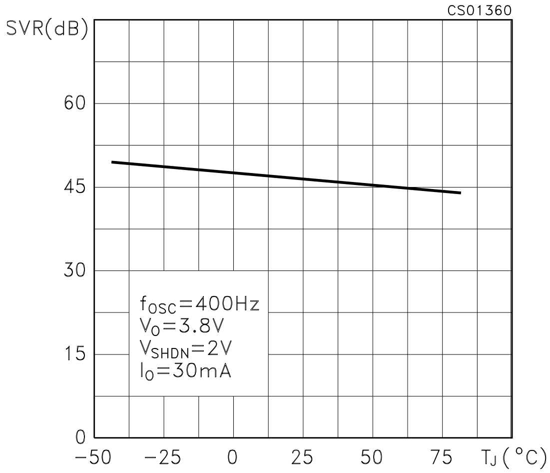


Figure 16: Quiescent Current vs Temperature

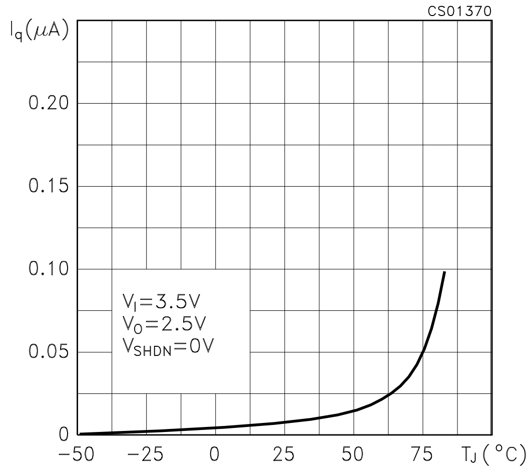


Figure 17: Quiescent Current vs Input Voltage

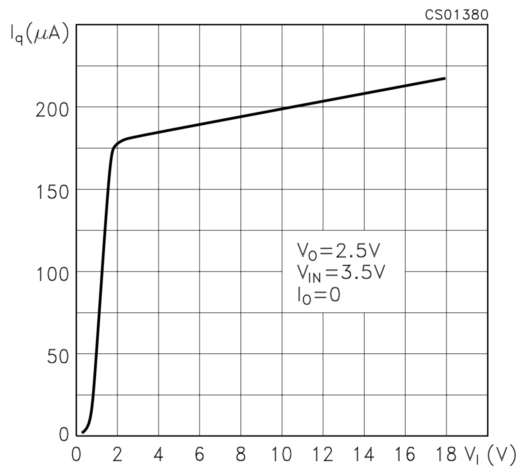


Figure 18: Quiescent Current vs Shutdown Voltage

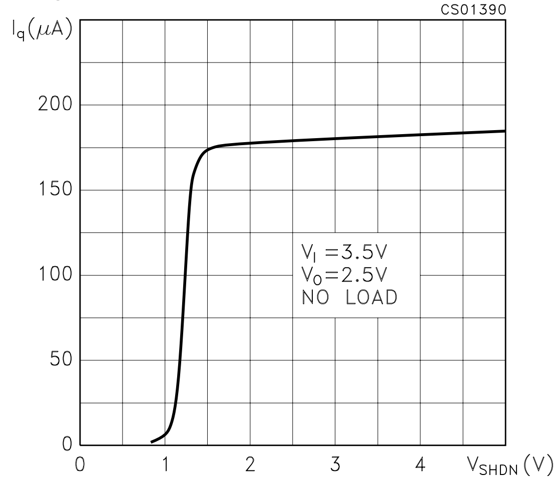


Figure 19: Quiescent Current vs Temperature

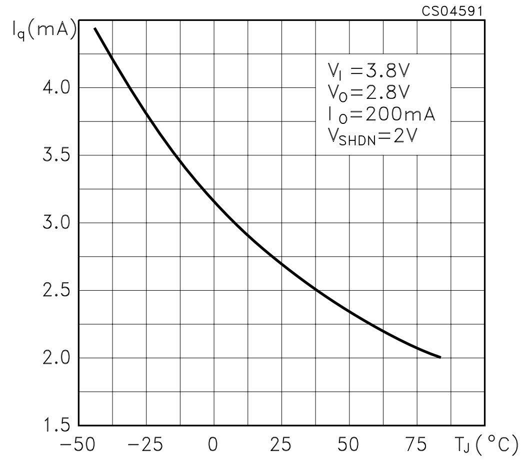


Figure 20: Reverse Current vs Reverse Voltage

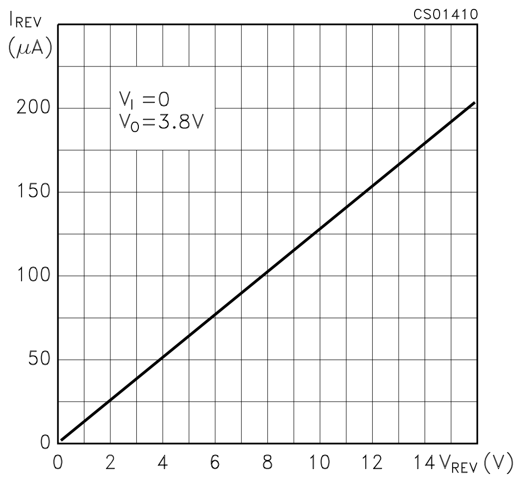


Figure 21: Stability

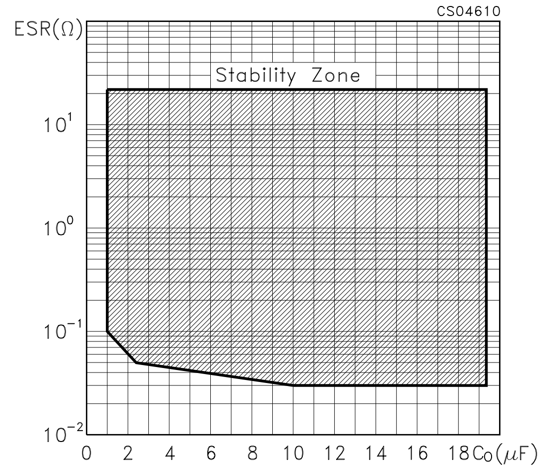
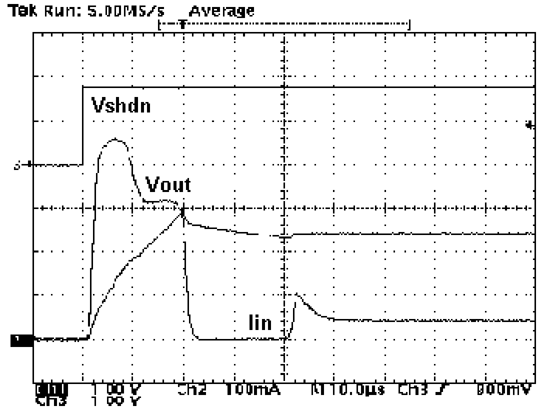


Figure 24: Start-up Transient



V_I=3.5V, V_O=2.5V, V_{SHDN}= 0 to 1.8V, R_L=68Ω, C_I=1μF, C_O=4.7μF, C_{BY}=100nF

Figure 22: Spectrum Noise

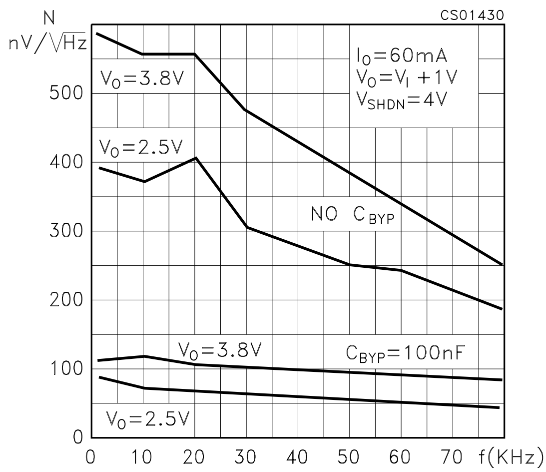
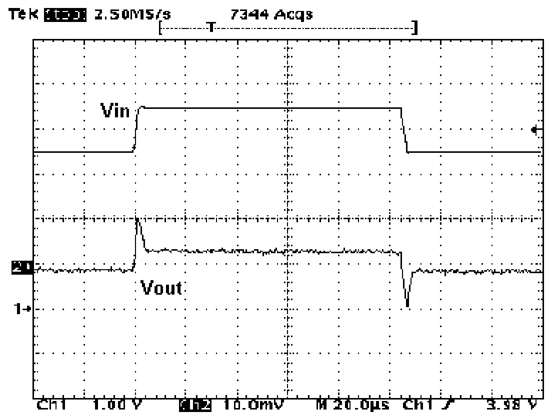
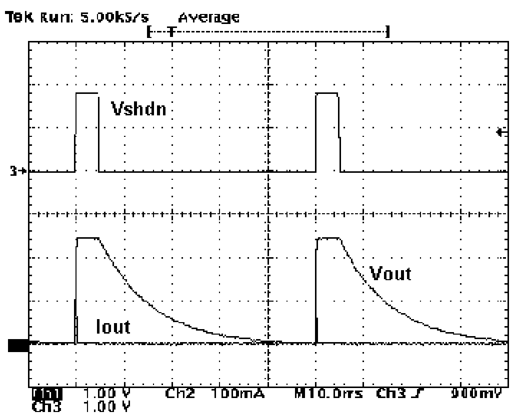


Figure 25: Line Transient



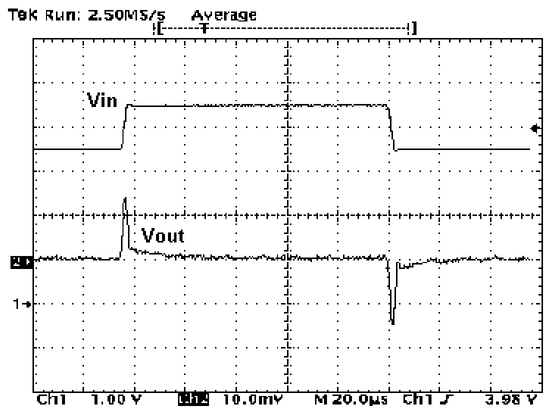
V_I=3.5 to 4.5V, V_O=2.5V, V_{SHDN}=1.8V, I_O=30mA, No C_I, C_O=10μF, C_{BY}=100nF, t_s=t_f=2μs

Figure 23: Start-up Transient



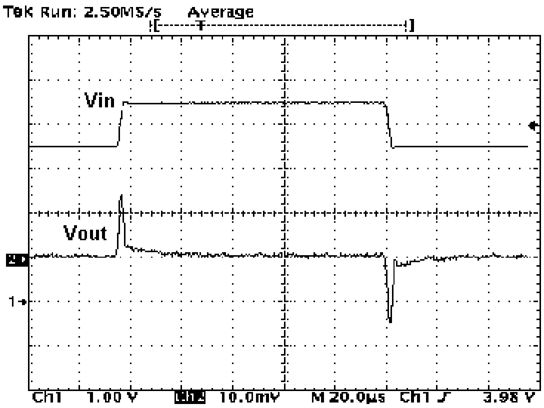
V_I=3.5V, V_O=2.5V, V_{SHDN}= 0 to 1.8V, R_L=2.5KΩ, C_I=1μF, C_O=4.7μF, C_{BY}=10nF

Figure 26: Line Transient



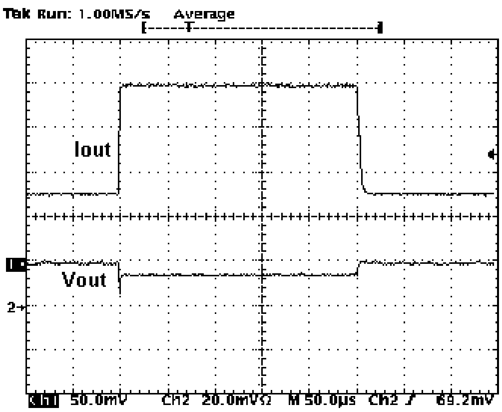
V_I=3.5 to 4.5V, V_O=2.5V, V_{SHDN}=1.8V, I_O=30mA, No C_I, C_O=10μF, C_{BY}=10nF, t_s=t_f=2μs

Figure 27: Line Transient



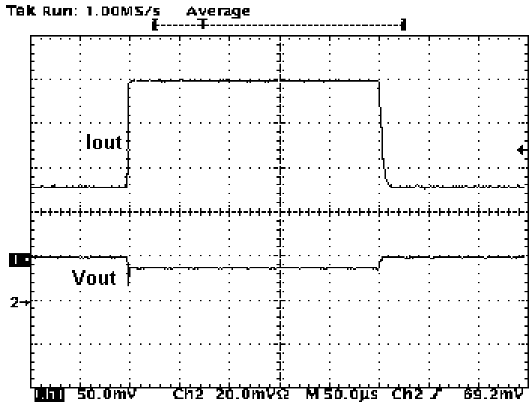
V_I=3.5 to 4.5V, V_O=2.5V, V_{SHDN}=1.8V, I_O=30mA, No C_I, C_O=1µF, C_{BY}=1nF, t_s=t_f=2µs

Figure 28: Load Transient



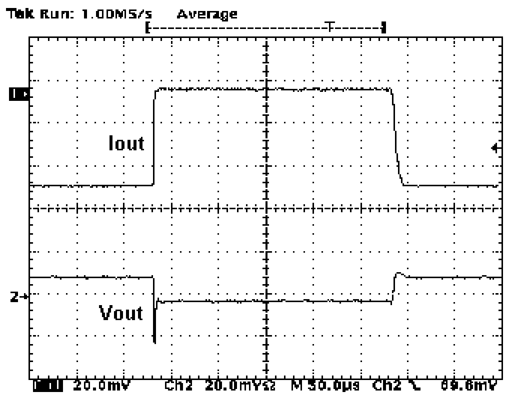
V_I=3.5 V, V_O=2.5V, V_{SHDN}=1.8V, I_O=50 to 100mA, C_I=1µF, C_O=2.2µF, C_{BY}=10nF, t_s=t_f=250ns

Figure 29: Load Transient



V_I=3.5V, V_O=2.5V, V_{SHDN}=1.8V, I_O=50 to 100mA, C_I1µF, C_O=10µF, C_{BY}=100nF, t_s=t_f=250ns

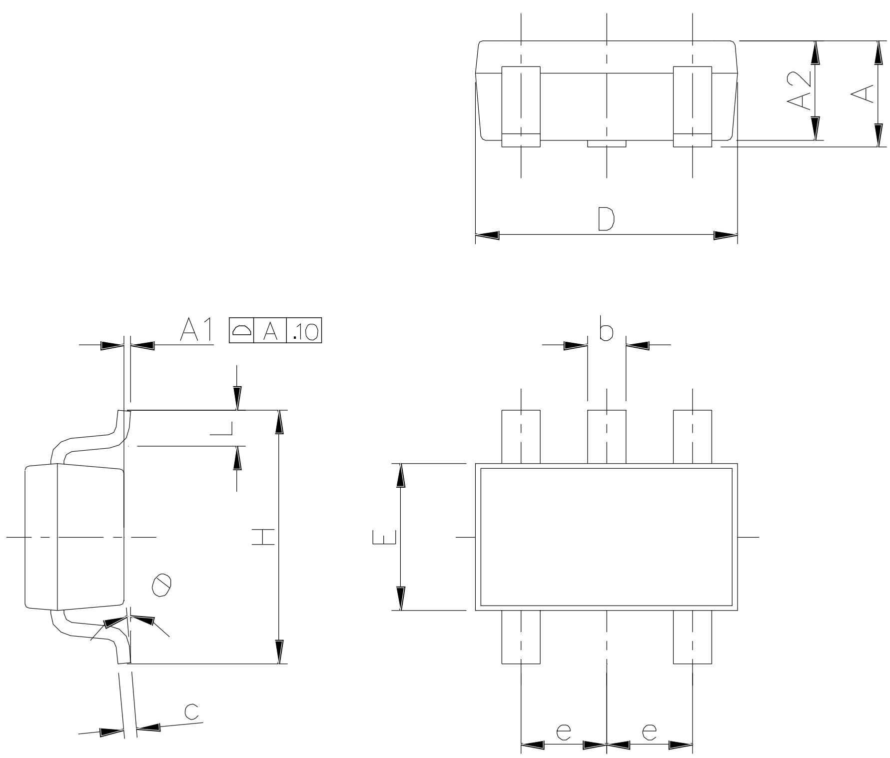
Figure 30: Load Transient



V_I=4.8 V, V_O=3.8V, V_{SHDN}=1.8V, I_O=50 to 100mA, C_I=1µF, C_O=2.2µF, C_{BY}=10nF, t_s=t_f=250ns

SOT23-5L MECHANICAL DATA

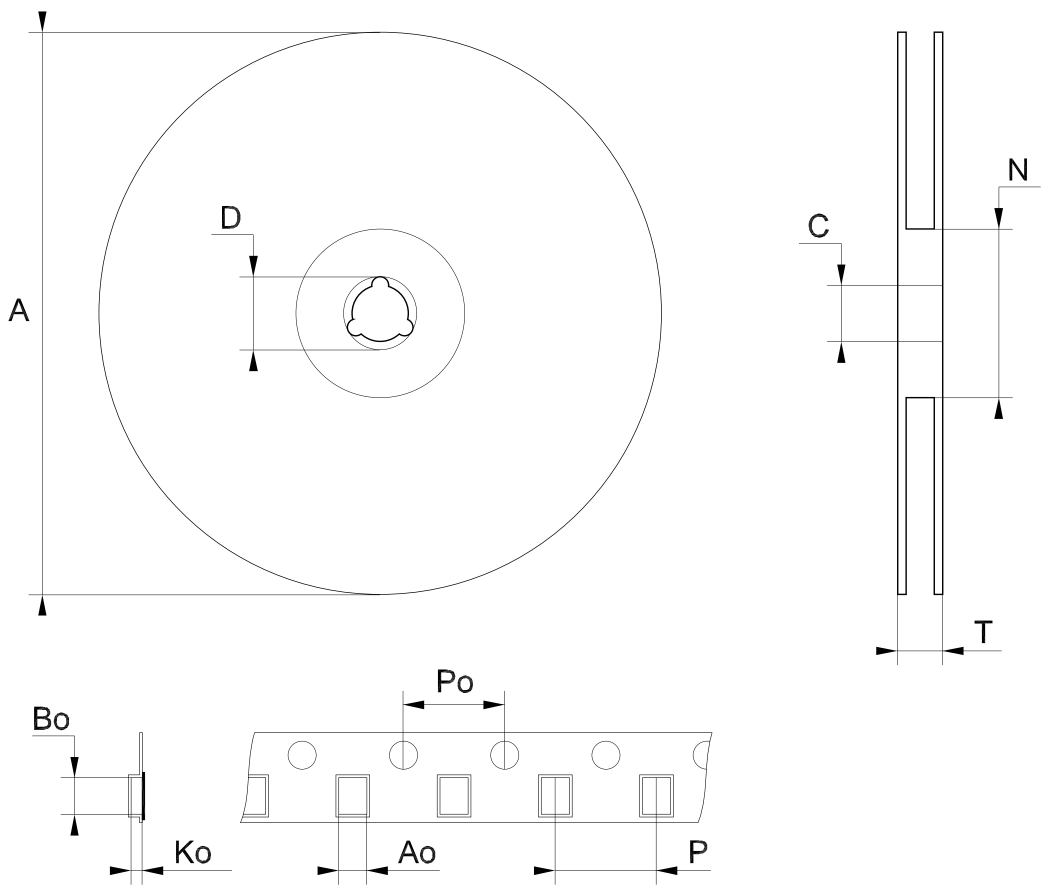
DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	35.4		57.1
A1	0.00		0.10	0.0		3.9
A2	0.90		1.30	35.4		51.2
b	0.35		0.50	13.7		19.7
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	1.50		1.75	59.0		68.8
e		0.95			37.4	
H	2.60		3.00	102.3		118.1
L	0.10		0.60	3.9		23.6



7049676C

Tape & Reel SOT23-xL MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.0.58
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161



Note: Drawing not in scale

Table 5: Revision History

Date	Revision	Description of Changes
31-Aug-2004	2	Mistake on Fig. 19.
31-Jan-2005	3	Change Maturity Code.