Ordering number : ENA1964

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

Bi-CMOS IC

LV58761MX — Step-down Switching Regulator

Overview

LV58761MX is a 1ch step-down switching regulator. With built-in 0.25Ω power MOSFET switch, it achieves high output current and high efficiency. With low-heat resistance, miniature package MFP8J (200mil) with heat-sink is adopted. Since it is Current mode control type, it has good load current response, and phase compensation is easy. With ON/OFF pin, operating can be less than 60μA at stand-by mode. It has cycle-by-cycle over current protection for load devices. With external capacitor, it achieves soft start.

Functions

- 1.5A 1ch step-down regulator
- Small package: MFP8J (200mil) with heat sink
- High efficiency (88% I_{OUT} = 1A, V_{IN} = 12V, V_O = 5V)
- Standby mode
- Over-current protection
- Thermal shutdown protection
- Reference voltage: 0.8V
- Inside frequency: 950kHz
- Soft start
- Wide input dynamic range (4.75 to 18V)

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum input V_{IN} voltage	V_{IN} max		20	V
BOOT pin maximum voltage	V_{BT} max		25	V
SW pin maximum voltage	V_{SW} max		V_{IN} max	V
BOOT pin-SW pin maximum voltage	V_{BS-SW} max		7	V
EN Maximum Voltage	V_{EN} max		20	V
FB, COMP, SS pin maximum voltage	V_{fs} max		7	V
Allowable power dissipation	Pd max	Mount on a specified board *1	1.25	W
Junction temperature	Tj max		150	°C
Operating temperature	Topr		-20 to 80	°C
Storage temperature	Tstg		-40 to 150	°C

*1: 46.4mm x 31.8mm x 1.7mm Four layers glass epoxy substrate.

Note: Plan the maximum voltage while including coil and surge voltages, so that the maximum voltage is not exceeded even for an instant.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
V_{IN} pin voltage	V_{IN}		4.75 to 18	V
BOOT pin voltage	V_{BT}		-0.3 to 23	V
SW pin voltage	V_{SW}		-0.4 to V_{IN}	V
BOOT pin-SW pin voltage	V_{BS-SW}		6.5	V
EN voltage	V_{EN}		18	V
FB, COMP, SS pin voltage	V_{FSO}		6	V

Electrical Characteristics at Ta = 25°C, V_{IN} = 12V

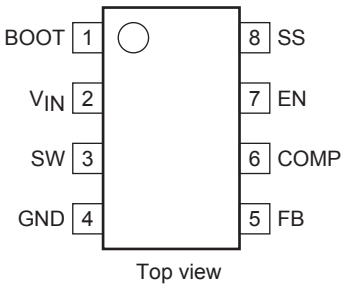
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
IC current drain at standby	$I_{CC}1$	EN=0V		60	80	μA
IC current drain in operation	$I_{CC}2$	EN=5v, FB=1V		2.3	3.1	mA
Efficiency	Effcy	V_{IN}=12V, I_{OUT}=1A, Vo=5V, Design target *2		88		%
Reference voltage	Vref	V_{IN}=4.75V to 28V	-2%	0.8	+2%	V
FB pin bias current	Iref	FB=0.8V		20	200	nA
High-side ON resistance	RonH	BOOT=5V, I_{OUT}=1A : *4		0.25		Ω
Oscillation frequency	f_{OSC}		760	950	1140	kHz
Oscillatory frequency when short-circuit is protected	f_{OSCS}		255	340	425	kHz
EN high-threshold voltage	$V_{EN}H$		0.9	1.8	2.7	V
EN low-threshold voltage	$V_{EN}L$		0.7	1.35	2.0	V
Maximum ON DUTY	D max			80		%
SW Peak Current limit 1	Icl1	V_{IN}=12V, V_{OUT}=1.2V, L=2.2μH	3.1		5.7	A
SW Peak Current limit 2	Icl2	V_{IN}=12V, V_{OUT}=3.3V, L=2.2μH	2.8		5.4	A
SW Peak Current limit 3	Icl3	V_{IN}=12V, V_{OUT}=5V, L=2.2μH	2.5		5.1	A
Thermal shutdown temperature	Ttsd	*Design guarantee *3		160		°C
Thermal shutdown temperature hysteresis	Dtsd	*Design guarantee *3		40		°C
Soft start current	I_{SS}	SS=0V	3	5	7	μA
UVLO threshold voltage	V_{UVLO}	V_{IN} Rising	3.9	4.2	4.5	V
UVLO hysteresis	V_{HYS}			0.2		V

*2: Reference value (not tested IC unit)

*3: Design guarantee (value guaranteed by design and not tested IC unit)

*4: Value in state of substrate mounting.

Pin Assignment

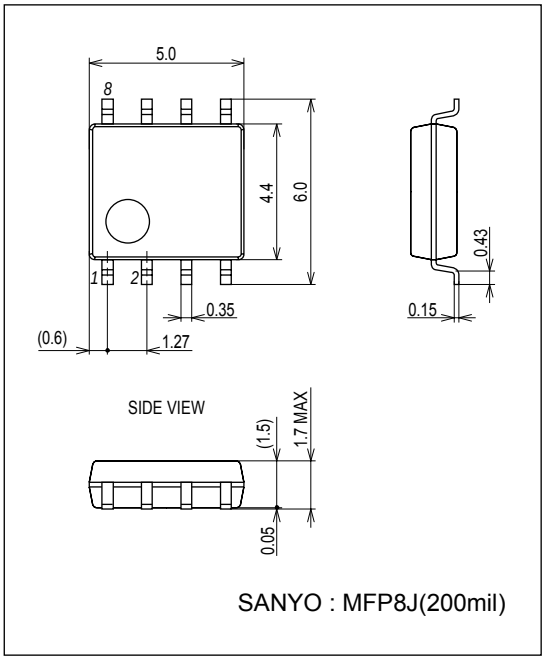


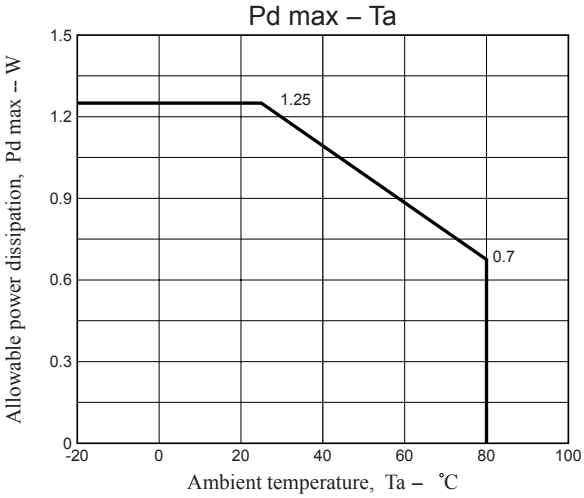
Top view

Package Dimensions

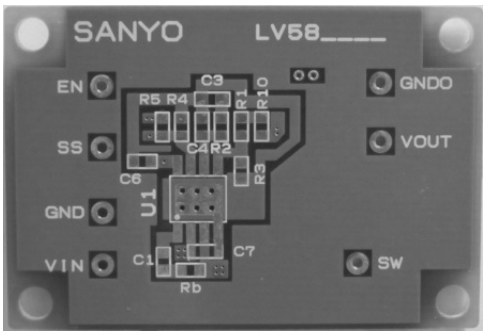
unit : mm (typ)

3411

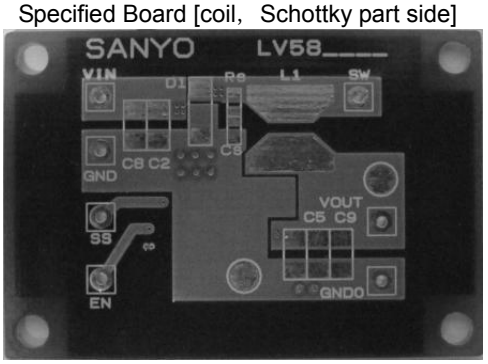




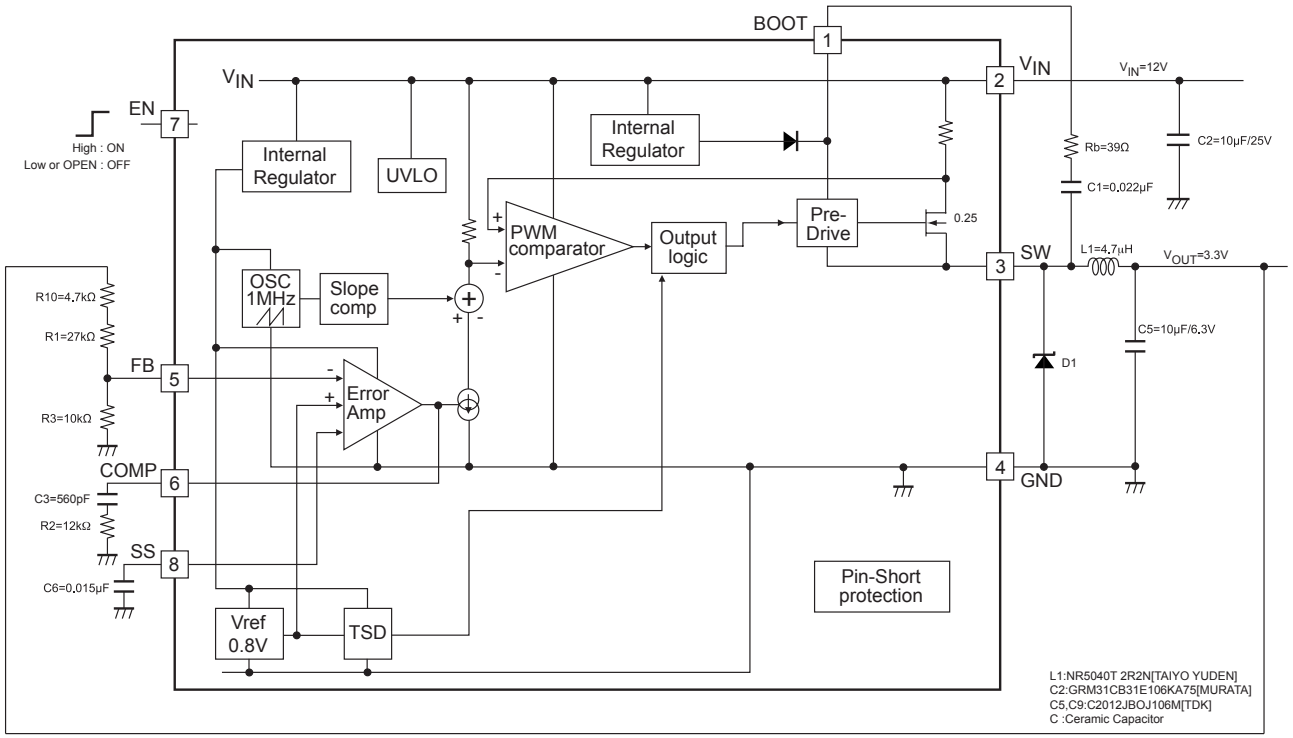
Specified Board [IC, Small signal part side]



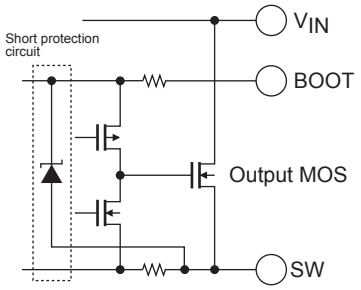
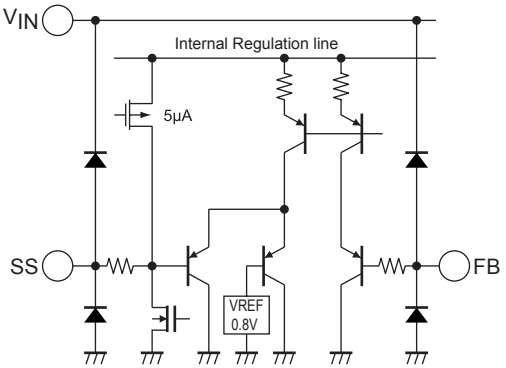
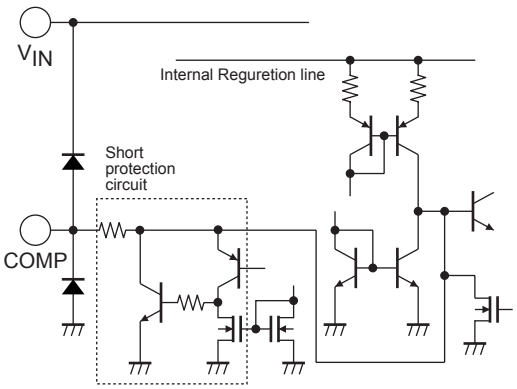
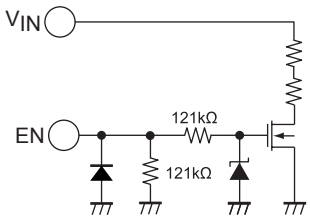
Specified Board [coil, Schottky part side]



Block Diagram and Sample Application Circuit

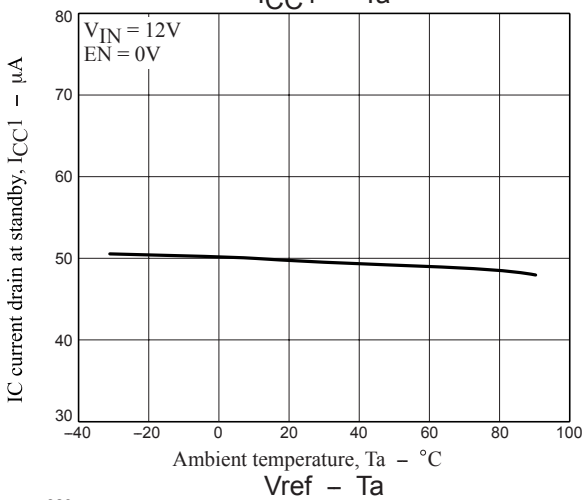


Pin Function

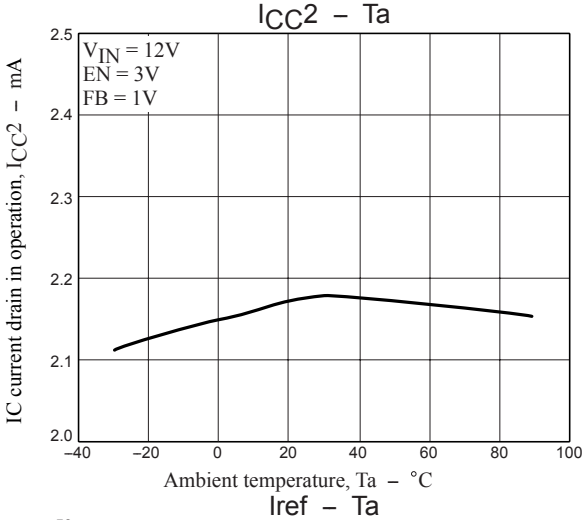
Pin No.	Pin name	Function	Equivalent circuit
1	BOOT	Upper MOS transistor boot strap capacitance connection pin. Connect the boot capacitance of about 0.022uF between SW pins. To protect the SW pin's absolute maximum rating , to ensure stable operation, and to eliminate noise , the boot capacitance serial resistance (about 100Ω) Rb proves effective.	
2	V_{IN}	Input Voltage Pin. Connect substantially large (10uF more) capacitance between this pin and GND.	
3	SW	Power Switch pin. Connect the output LC filter. Connect the above capacitance between this pin and BOOT pin.	
4	GND	Ground pin.	
5	FB	Feedback pin. Set the output voltage by means of split resistor in the section of the output voltage VOUT-FB-GND. VOUT setting is made as calculated below. $V_{OUT} = Vref \times \{ 1 + \frac{(R1 + R10)}{R3} \}$ Vref = 0.8V Example: 3.3V output voltage (See, Block Diagram and Application example) $V_{OUT} = 0.8 \times \{ 1 + \frac{(27k + 4.3k)}{10k} \}$ =3.304V	
8	SS	Soft start pin. Sets the soft start time by means of the built-in 5μA source voltage and external soft start capacity. The soft start capacity C_{SS} can be set as follows: $C_{SS} = 5\mu A \times \frac{Tss}{Vref}$ Where, Tss is the soft start time and Vref is the reference voltage. Example:2.4ms soft start time achieved $C_{SS} = 5\mu A \times \frac{2.4ms}{0.8V} = 0.015\mu F$	
6	COMP	Phase compensation pin. Connects with the phase compensation external capacitance and resistance of DC/DC converter close loop.	
7	EN	Enable pin. Converter enabled when set to the HIGH voltage and disabled when GND or OPEN state.	

Reference data (1)

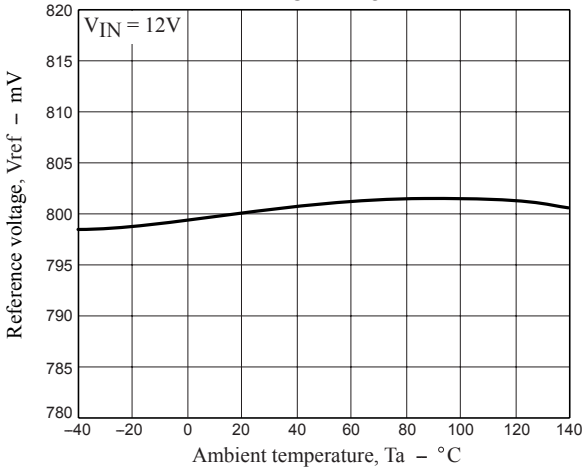
$I_{CC}1$ – Ta



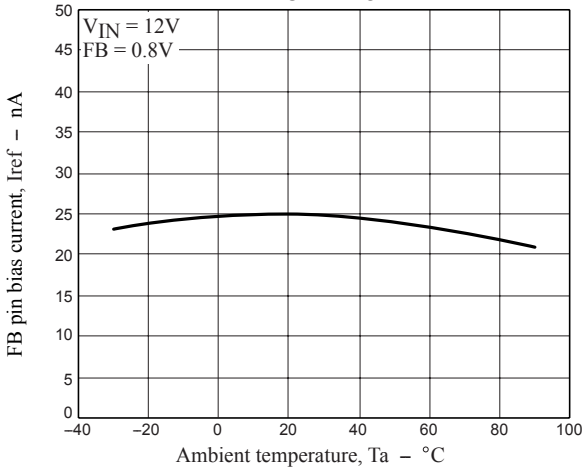
$I_{CC}2$ – Ta



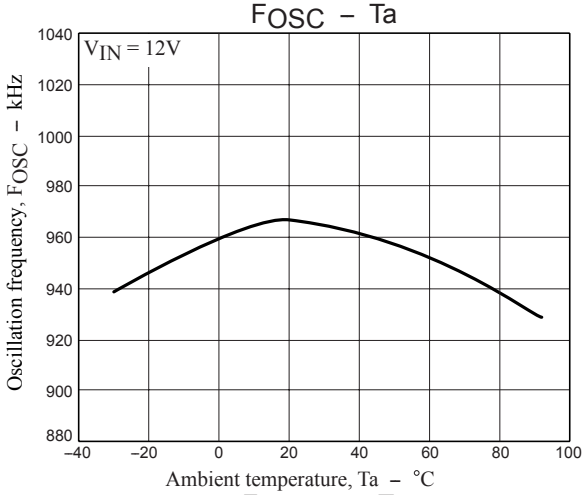
Vref – Ta



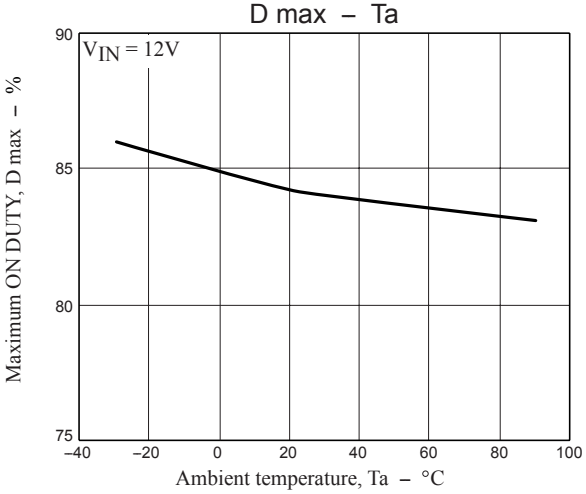
Iref – Ta



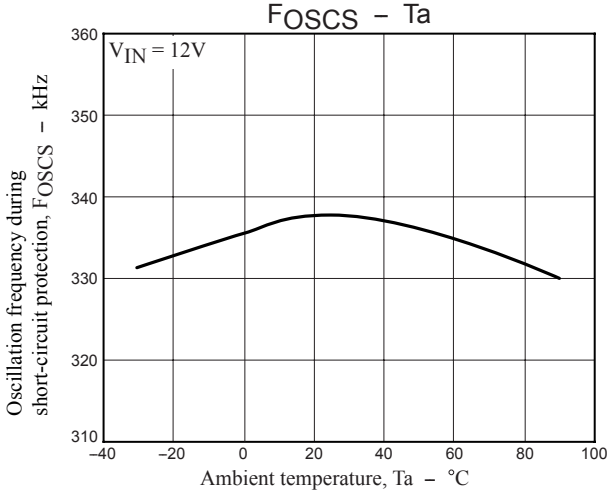
F_{OSC} – Ta



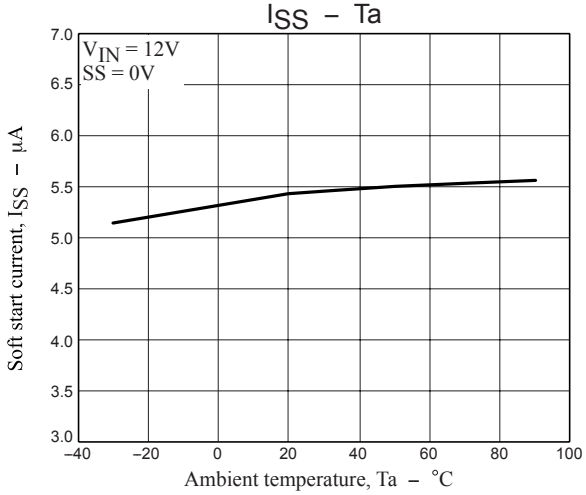
D max – Ta

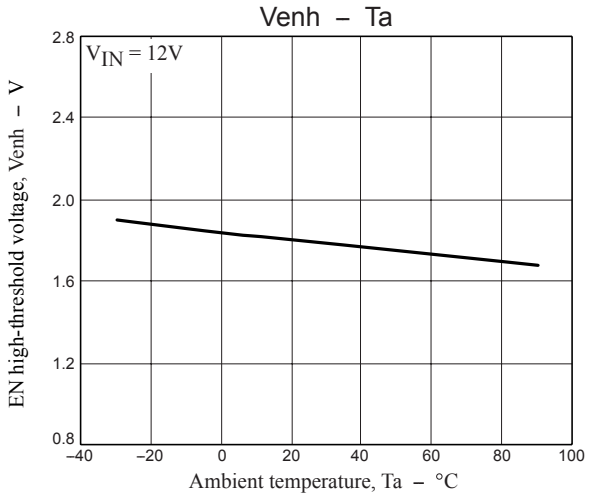


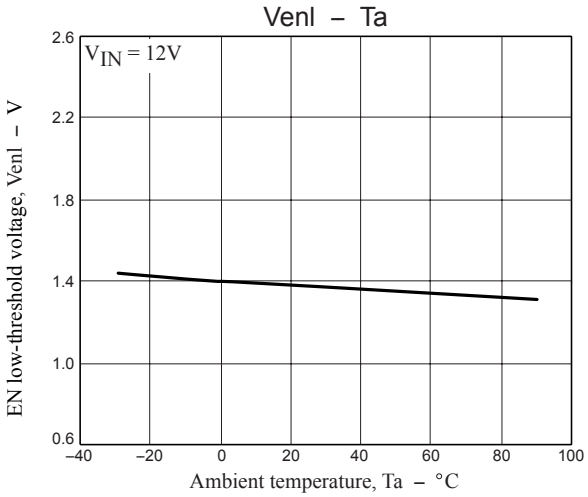
F_{OSCS} – Ta

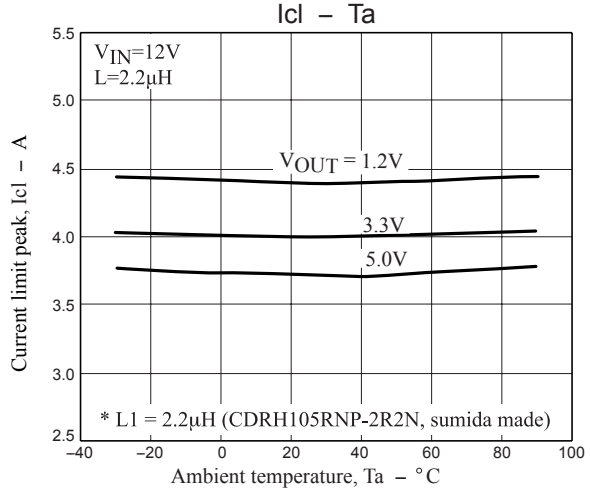


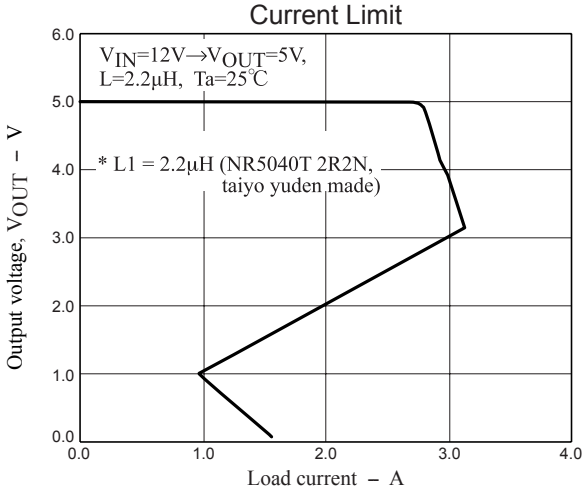
I_{SS} – Ta

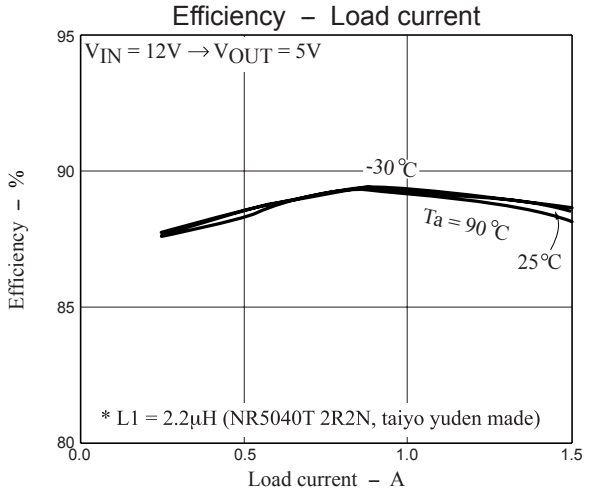


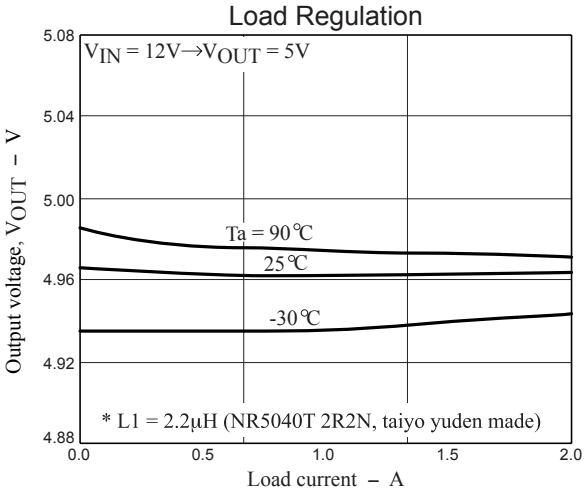








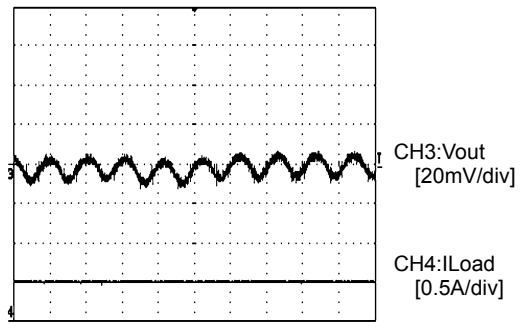




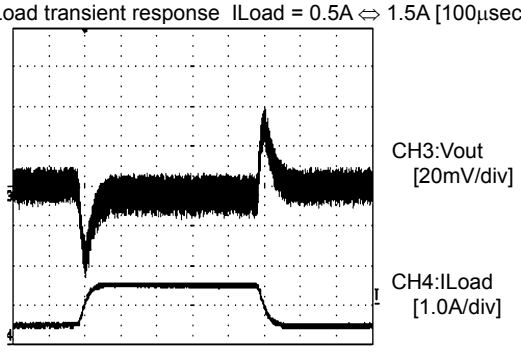
Reference data (2)

(* measurement circuit is shown in "Block Diagram and Sample Application circuit")

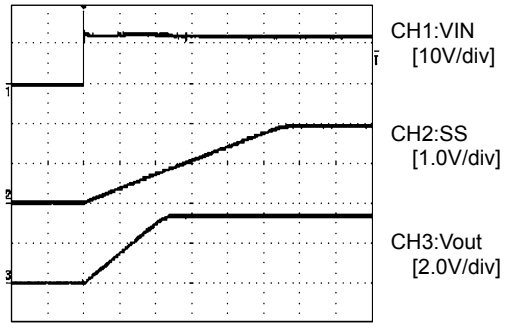
•Output voltage lipple ILoad=0.5A [1.0usec/div]



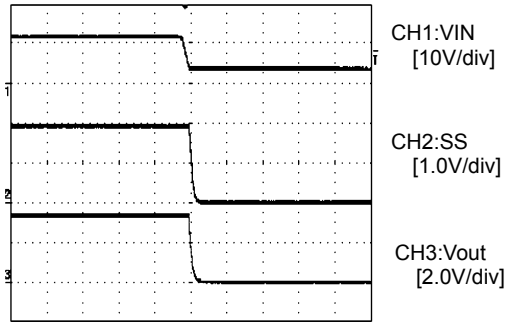
•Load transient response ILoad = 0.5A ⇔ 1.5A [100µsec/div]



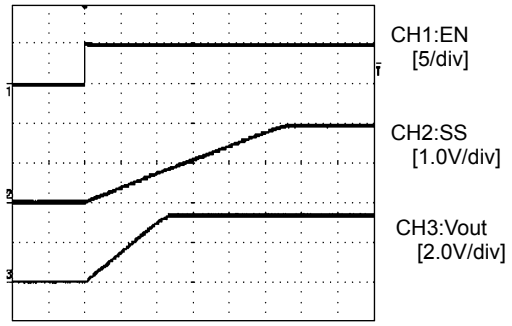
•V_{IN} start up waveform Rload = 6Ω [1msec/div]



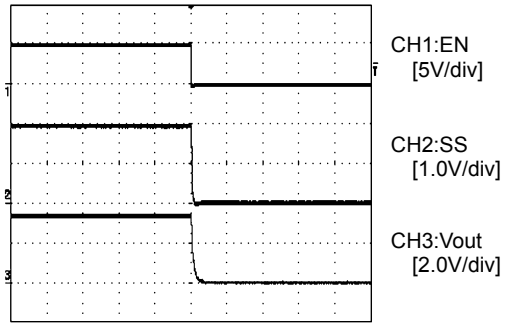
•V_{IN} stop waveform Rload = 6Ω [1msec/div]



•EN start up waveform Rload = 6Ω [1msec/div]



•EN stop waveform Rload = 6Ω [1msec/div]



Considerations for the design

• When V_{IN}=12V or less is used, boot strap voltage shortage because of intermittent operation at a no load might happen, and it not operate normally. The load of about 500Ω is put between V_{OUT}-GND, and in that case, avoid and use an intermittent mode.

• Insertion of serial beads in the Schottky diode for removal of noise may cause generation of the negative voltage deviating from the absolute maximum rating at the SW pin, resulting in failure of normal operation. In such an event, do not insert beads as above described and, instead, remove noise by means of the BOOT resistance Rb