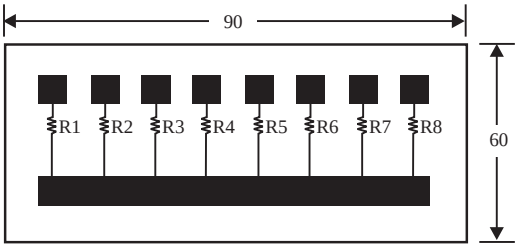
BUSSED RESISTOR NETWORK

California Micro Devices' resistor arrays are the hybrid equivalent to the bussed resistor networks available in surface-mount packages. The resistors are spaced on ten mil centers resulting in reduced real estate. These chips are manufactured using advanced thin film processing techniques and are 100% electrically tested and visually inspected.

STANDARD NETWORK SCHEMATIC DIAGRAM



Formats

Die Size: 90±3 x 60±3 mils
Bonding Pads: 5x7 mils typical

ELECTRICAL SPECIFICATIONS

Parameter	Test Conditions		
TCR	–55°C to 125°C	±100ppm/C	Max
Operating Voltage	–55°C to 125°C	50Vdc	Max
Power Rating (per resistor)	@ 70°C (Derate linearly to 0@150°C)	50mw	Max
Thermal Shock	Method 107 MIL-STD-202F	±0.25%@ΔR	Max
High Temperature Exposure	100Hrs @ 150°C Ambient	±0.25%ΔR	Max
Moisture	Method 106 MIL-STD-202F	±0.5%ΔR	Max
Life	Method 108 MIL-STD-202F (125°C/1000hr)	±0.5%ΔR	Max
Noise	Method 308 MIL-STD-202F	–35dB	Max
	≥250kΩ	–30dB	Max
Short Time Overload	MIL-R-83401	0.25%	Max
Insulation Resistance	@25°C	1 x 10_{12}Ω	Min.

MECHANICAL SPECIFICATIONS

Substrate	Silicon 10 ±2 mils thick
Isolation Layer	Si02 10,000Å thick, min
Backing	Lapped (gold optional)
Metalization	Aluminum 10,000Å thick, min (15,000Å gold optional)
Passivation	Silicon Nitride

VALUES

8 resistors from 100Ω to 500KΩ

PACKAGING

Two inch square trays of 196 chips maximum is standard.

NOTES

1. Resistor pattern may vary from one value to another.

PART NUMBER DESIGNATION

NCC	5003	F	A	G	W	P
Series	**Value**	**Tolerance**	**TCR**	**Bond Pads**	**Backing**	**Ratio Tolerance**
	First 3 digits are	D = ±0.5%	No Letter = ±100ppm	G = Gold	W = Gold	No Letter = 1%
	significant value.	F = ±1%	A = ±50ppm	No Letter = Aluminum	L = Lapped	P = 0.5%
	Last digit repres-	G = ±2%	B = ±25ppm		No Letter = Either	
	sents number of	J = ±5%				
	zeros. R indicates	K = ±10%				
	decimal point.	M = ±20%				

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