Low Charge Injection
8-Channel High Voltage Analog Switch

Features

▶ HVCMOS® technology for high performance
▶ Very low quiescent power dissipation (-10μA)
▶ Output on-resistance typically 22Ω
▶ Low parasitic capacitances
▶ DC to 50MHz small signal frequency response
▶ -60dB typical output off isolation at 5.0MHz
▶ CMOS logic circuitry for low power
▶ Excellent noise immunity
▶ On-chip shift register, latch and clear logic circuitry
▶ Flexible high voltage supplies

Applications

▶ Medical ultrasound imaging
▶ Piezoelectric transducer drivers

General Description

This device is a low charge injection, 8-channel, high-voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as ultrasound imaging and printers.

Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. To reduce any possible clock feed-through noise, Latch Enable Bar ($\overline{LE}$) should be left high until all bits are clocked in. Using HVCMOS® technology, this switch combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

These ICs are suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN} : +50V/-150V, or +100V/-100V.

Block Diagram
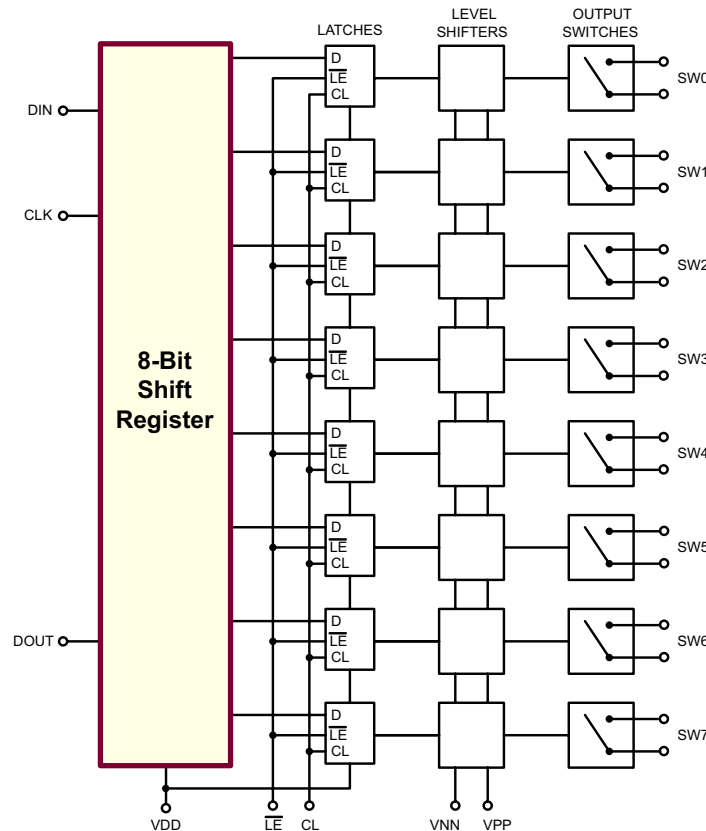
Ordering Information

| Device	28-Lead PLCC .453x.453in body .180in height (max) .050in pitch
HV20320	HV20320PJ-G

-G indicates the part is RoHS compliant ('Green')

Pin Configuration

28-Lead PLCC (PJ)
(top view)

Absolute Maximum Ratings

Parameter	Value
V_{DD} logic power supply voltage	-0.5V to +15V
V_{PP} - V_{NN} supply voltage	220V
V_{PP} positive high voltage supply	-0.5V to V_{NN} +200V
V_{NN} negative high voltage supply	+0.5V to -200V
Logic input voltages	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation	1.2W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.
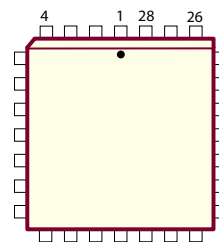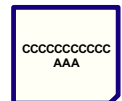
Product Marking

Top Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*

Bottom Marking

———— = "Green" Packaging

*May be part of top marking

Package may or may not include the following marks: Si or

28-Lead PLCC (PJ)

Operating Conditions

Sym	Parameter	Value
V_{DD}	Logic power supply voltage[1,3]	4.5V to 13.2V
V_{PP}	Positive high voltage supply[1,3]	40V to V_{NN} +200V
V_{NN}	Negative high voltage supply[1,3]	-40V to -160V
V_{IH}	High level input voltage	V_{DD} -1.5V to V_{DD}
V_{IL}	Low-level input voltage	0V to 1.5V
V_{SIG}	Analog signal voltage peak-to-peak	V_{NN} +10V toV_{PP} -10V[2]
T_A	Operating free air temperature	0°C to 70°C

Notes:
1. *Power up/down sequence is arbtrary except GND must be powered -up first and powered down last.*
2. *V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transition.*
3. *Rise and fall times of power supplies V_{DD}, V_{PP}, and V_{NN} should not be less than 1.0msec.*

DC Electrical Characteristics *(Over operating conditions unless otherwise specified)*

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R$_{ONS}$	Small signal switch on-resistance	-	30	-	26	38	-	48	Ω	I$_{SIG}$ = 5.0mA	V$_{PP}$ = +40V V$_{NN}$ = -160V
		-	25	-	22	27	-	32		I$_{SIG}$ = 200mA	
		-	25	-	22	27	-	30		I$_{SIG}$ = 5.0mA	V$_{PP}$ = +100V V$_{NN}$ = -100V
		-	18	-	18	24	-	27		I$_{SIG}$ = 200mA	
		-	23	-	20	25	-	30		I$_{SIG}$ = 5.0mA	V$_{PP}$ = +160V V$_{NN}$ = -40V
		-	22	-	16	25	-	27		I$_{SIG}$ = 200mA	
ΔR$_{ONS}$	Small signal switch on-resistance matching	-	20	-	5.0	20	-	20	%	I$_{SIG}$ = 5.0mA, V$_{PP}$ = +100V, V$_{NN}$ = -100V	
R$_{ONL}$	Large signal switch on-resistance	-	-	-	15	-	-	-	Ω	V$_{SIG}$ = V$_{PP}$ -10V, I$_{SIG}$ = 1.0A	
I$_{SOL}$	Switch off leakage per switch	-	5.0	-	1.0	10	-	15	µA	V$_{SIG}$ = V$_{PP}$ -10V, V$_{NN}$ +10V	
V$_{OS}$	DC offset switch off	-	300	-	100	300	-	300	mV	R$_L$ = 100kΩ	
	DC offset switch on	-	500	-	100	500	-	500	mV	R$_L$ = 100kΩ	
I$_{PPQ}$	Quiescent V$_{PP}$ supply current	-	-	-	10	50	-	-	µA	All switches Off	
I$_{NNQ}$	Quiescent V$_{NN}$ supply current	-	-	-	-10	-50	-	-	µA	All switches Off	
I$_{PPQ}$	Quiescent V$_{PP}$ supply current	-	-	-	10	50	-	-	µA	All switches On, I$_{SW}$ = 5.0mA	
I$_{NNQ}$	Quiescent V$_{NN}$ supply current	-	-	-	-10	-50	-	-	µA	All switches On, I$_{SW}$ = 5.0mA	
I$_{SW}$	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V$_{SIG}$ duty cycly < 0.1%	
f$_{SW}$	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I$_{PP}$	Supply current	-	6.5	-	-	7.0	-	8.0	mA	V$_{PP}$ = +40V V$_{NN}$ = -160V	All output switches are turning On and Off at 50kHz with no load
		-	4.0	-	-	5.0	-	5.5		V$_{PP}$ = +100V V$_{NN}$ = -100V	
		-	4.0	-	-	5.0	-	5.5		V$_{PP}$ = +160V V$_{NN}$ = -40V	
I$_{NN}$	Supply curent	-	6.5	-	-	7.0	-	8.0	mA	V$_{PP}$ = +40V V$_{NN}$ = -160V	All output switches are turning On and Off at 50kHz with no load
		-	4.0	-	-	5.0	-	5.5		V$_{PP}$ = +100V V$_{NN}$ = -100V	
		-	4.0	-	-	5.0	-	5.5		V$_{PP}$ = +160V V$_{NN}$ = -40V	
I$_{DD}$	Logic supply average current	-	4.0	-	-	4.0	-	4.0	mA	f$_{CLK}$ = 5.0MHz, V$_{DD}$ = 5.0V	
I$_{DDQ}$	Logic supply quiescent current	-	10	-	-	10	-	10	µA	---	
I$_{SOR}$	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V$_{OUT}$ = V$_{DD}$ -0.7V	
I$_{SINK}$	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V$_{OUT}$ = 0.7V	
C$_{IN}$	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

AC Electrical Characteristics

(Over recommended operating conditions: V_{DD} = 5.0V, unless otherwise specified)

| Sym	Parameter	0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+70°C Min	+70°C Max	Units	Conditions
t_{SD}	Set up time before $\overline{LE}$ rises	150	-	150	-	-	150	-	ns	---
t_{WLE}	Time width of $\overline{LE}$	150	-	150	-	-	150	-	ns	---
t_{DO}	Clock delay time to data out	-	150	-	-	150	-	150	ns	---
t_{WCL}	Time width of CL	150	-	150	-	-	150	-	ns	---
t_{SU}	Set up time data to clock	15	-	15	8.0	-	20	-	ns	---
t_{H}	Hold time data from clock	35	-	35	-	-	35	-	ns	---
f_{CLK}	Clock frequency	-	5.0	-	-	5.0	-	5.0	MHz	50% Duty cycle, $f_{DATA}= f_{CLK}/2$
t_{R}, t_{F}	Clock rise and fall times	-	50	-	-	50	-	50	ns	---
t_{ON}	Turn on time	-	5.0	-	-	5.0	-	5.0	µs	V_{SIG} = V_{PP} -10V, R_{LOAD} = 10kΩ
t_{OFF}	Turn off time	-	5.0	-	-	5.0	-	5.0	µs	V_{SIG} = V_{PP} -10V, R_{LOAD} = 10kΩ
dv/dt	Maximun V_{SIG} slew rate	-	20	-	-	20	-	20	V/ns	V_{PP} = +160V, V_{NN} = -40V
		-	20	-	-	20	-	20		V_{PP} = +100V, V_{NN} = -100V
		-	20	-	-	20	-	20		V_{PP} = +40V, V_{NN} = -160V
K_{O}	Off isolation	-30	-	-30	-33	-	-30	-	dB	f = 5.0MHz, 1.0kΩ/15pF load
		-58	-	-58	-	-	-58	-		f = 5.0MHz, 50Ω load
K_{CR}	Switch crosstalk	-60	-	-60	-70	-	-60	-	dB	f = 5.0MHz, 50Ω load
I_{ID}	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	Off capacitance SW to GND	5.0	17	5.0	12	17	5.0	17	pF	0V, f = 1.0MHz
$C_{SG(ON)}$	On capacitance SW to GND	25	50	25	38	50	25	50	pF	0V, f = 1.0MHz
$+V_{SPK}$	Output voltage spike	-	-	-	-	150	-	-	mV	V_{PP} = +40V, V_{NN} = -160V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	150	-	-		
$+V_{SPK}$		-	-	-	-	150	-	-		V_{PP} = +100V, V_{NN} = -100V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	150	-	-		
$+V_{SPK}$		-	-	-	-	150	-	-		V_{PP} = +160V, V_{NN} = -40V, R_{LOAD} = 50Ω
$-V_{SPK}$		-	-	-	-	150	-	-		
QC	Charge injection	-	-	-	820	-	-	-	pC	V_{PP} = +40V, V_{NN} = -160V, V_{SIG} = 0V
		-	-	-	600	-	-	-		V_{PP} = +100V, V_{NN} = -100V, V_{SIG} = 0V
		-	-	-	350	-	-	-		V_{PP} = +160V, V_{NN} = -40V, V_{SIG} = 0V

Truth Table

D0	D1	D2	D3	D4	D5	D6	D7	$\overline{LE}$	CLR	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	Off							
H								L	L	On							
	L							L	L		Off						
	H							L	L		On						
		L						L	L			Off					
		H						L	L			On					
			L					L	L				Off				
			H					L	L				On				
				L				L	L					Off			
				H				L	L					On			
					L			L	L						Off		
					H			L	L						On		
						L		L	L							Off	
						H		L	L							On	
							L	L	L								Off
							H	L	L								On
X	X	X	X	X	X	X	X	H	L	Hold Previous State							
X	X	X	X	X	X	X	X	X	H	All Switches Off							

Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L to H transition of the CLK.
3. The switches go to a state retaining their present condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift register data flow through the latch.
4. D_{OUT} is high when data in the shift register 7 is high.
5. Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.
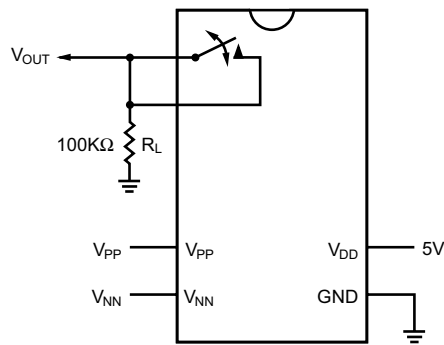*6. The CLR clear input overrides all other inputs.*
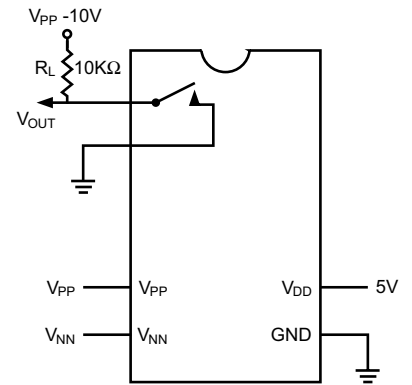
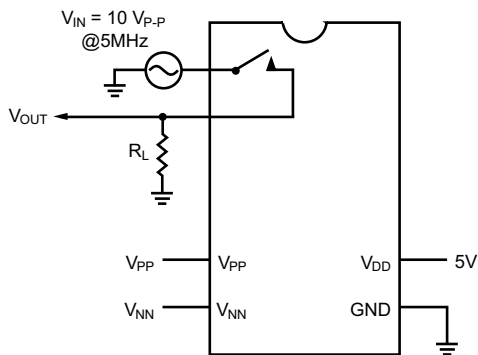## Logic Timing Waveforms
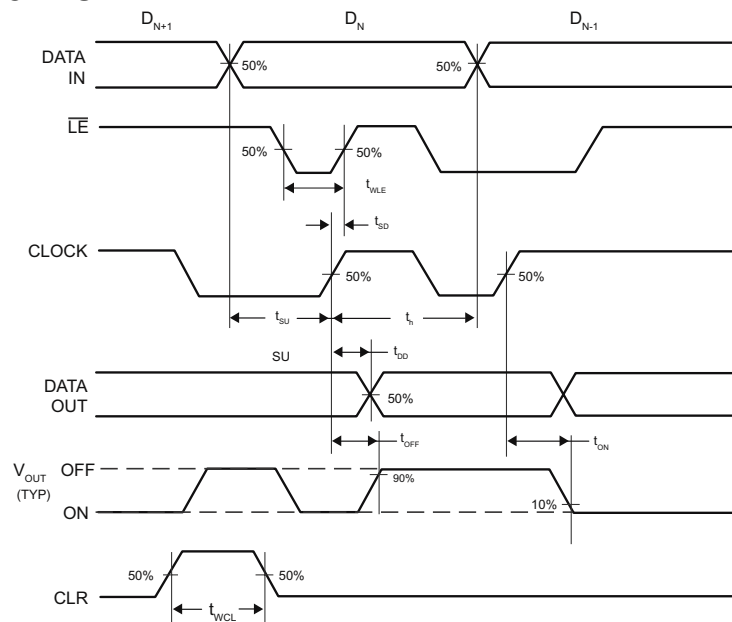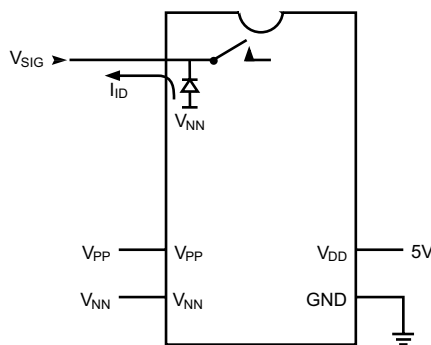
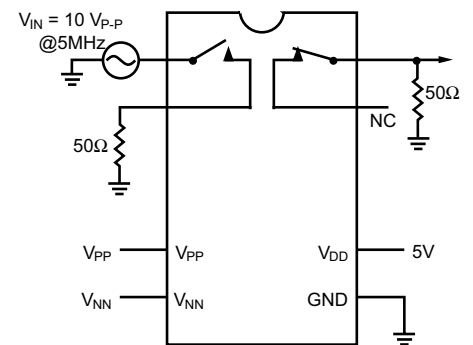# Test Circuits
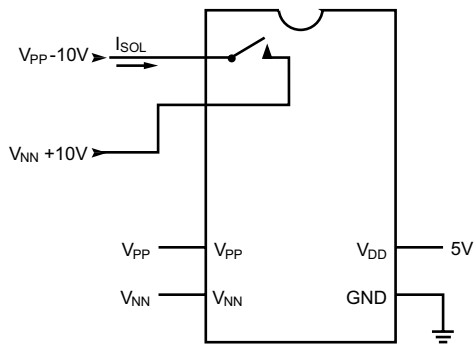
Switch OFF Leakage
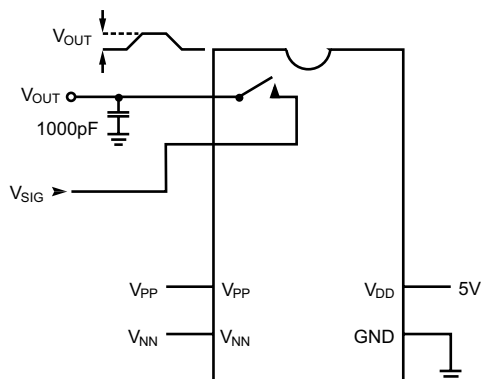

DC Offset ON/OFF

T_{ON}/T_{OFF} Test Circuit

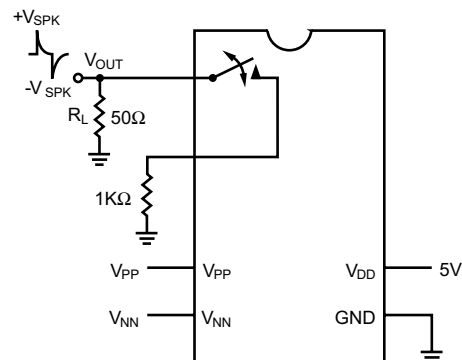$$K_O = 20 Log \frac{V_{OUT}}{V_{IN}}$$

OFF Isolation

Isolation Diode Current
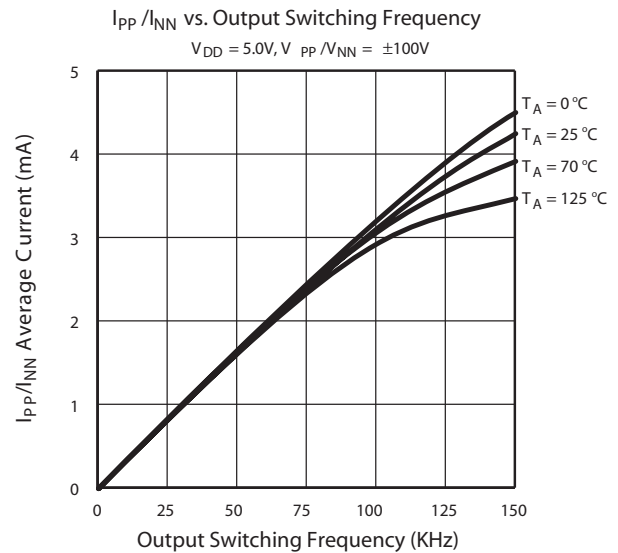

$$K_{CR} = 20 Log \frac{V_{OUT}}{V_{IN}}$$

Crosstalk

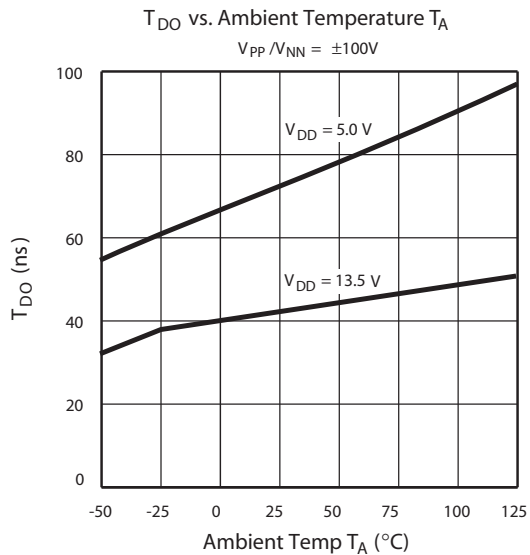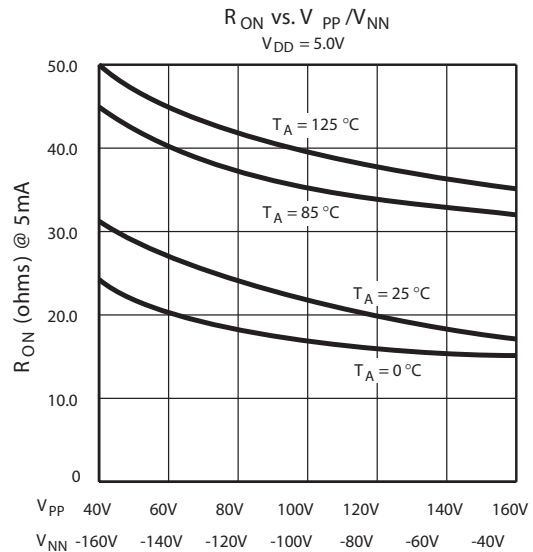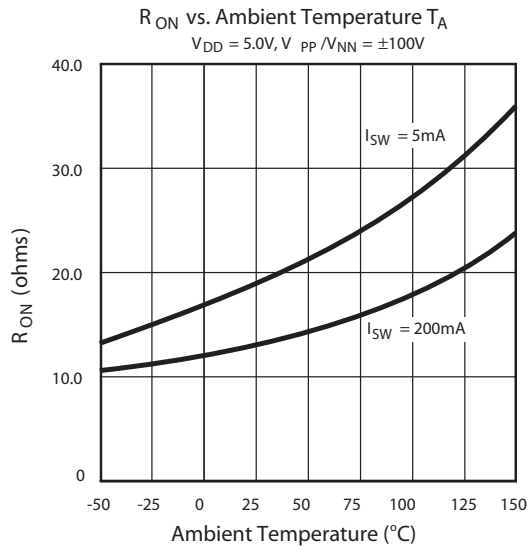$$Q = 1000pF \times V_{OUT}$$

Charge Injection

Output Voltage Spike

Typical Performance Curves

I_{DD} vs Clock Frequency
$V_{DD} = 5.0V$, $V_{PP}/V_{NN} = \pm100V$, $T_A = 0°C$ to $70°C$

Off-Isolation vs. Signal Voltage Frequency
$V_{DD} = 5.0V$, $V_{PP}/V_{NN} = \pm100V$

R_{ON} vs. Ambient Temperature T_A
$V_{DD} = 5.0V$, $V_{PP}/V_{NN} = \pm100V$

R_{ON} vs. V_{PP}/V_{NN}
$V_{DD} = 5.0V$

T_{DO} vs. Ambient Temperature T_A
$V_{PP}/V_{NN} = \pm100V$

I_{PP}/I_{NN} vs. Output Switching Frequency
$V_{DD} = 5.0V$, $V_{PP}/V_{NN} = \pm100V$
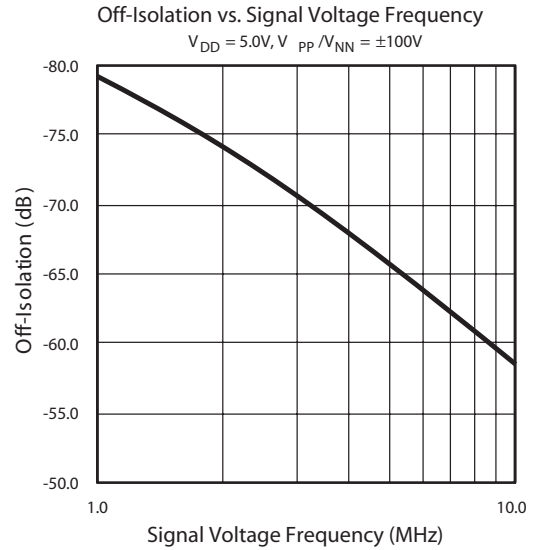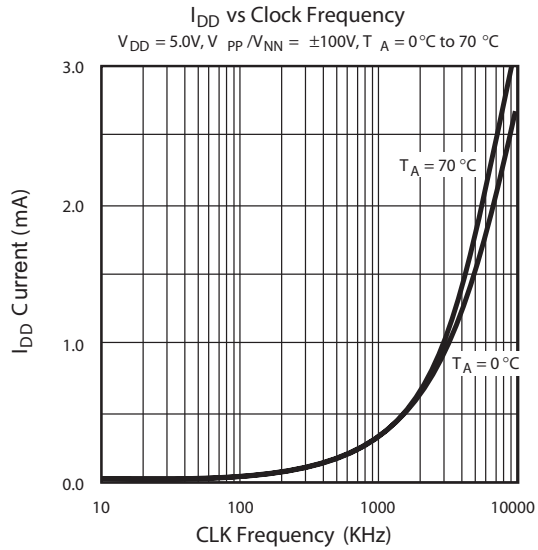
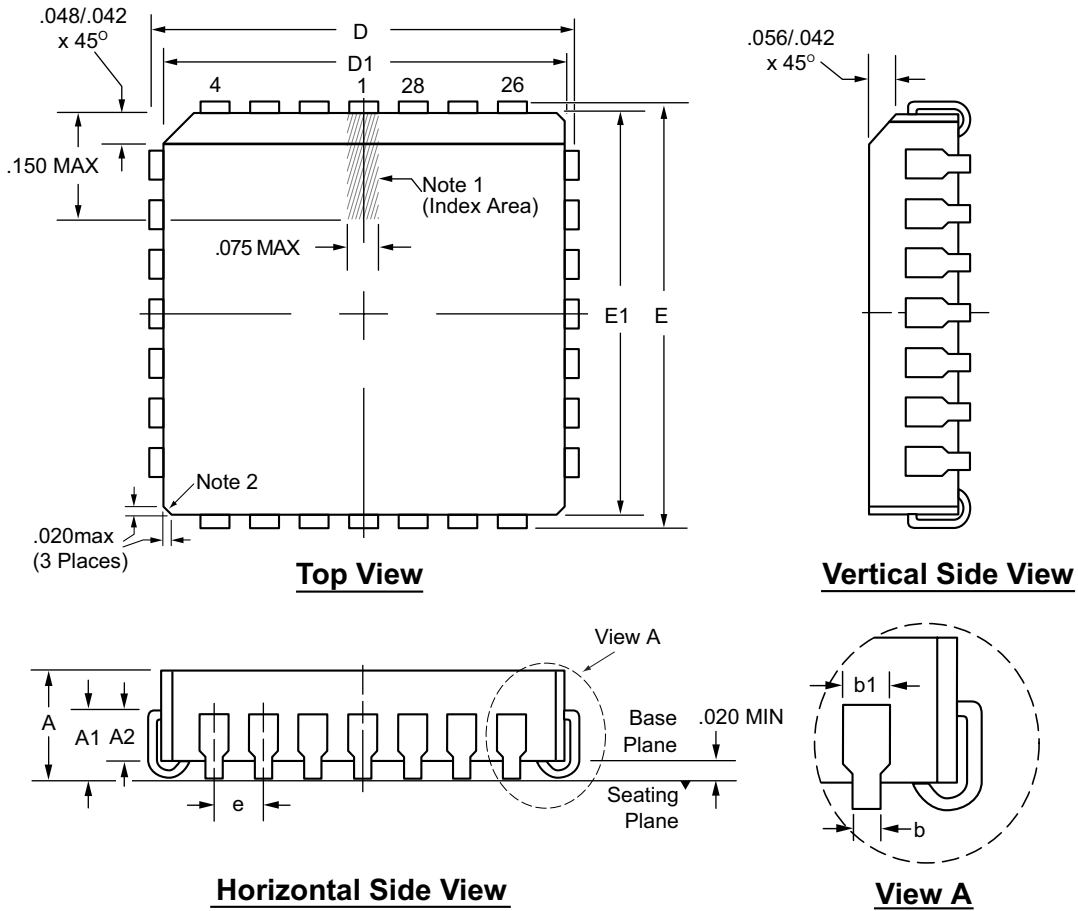## Pin Description

Pin #	Name	Pin #	Name
1	SW3	15	N/C
2	SW3	16	DIN
3	SW2	17	CLK
4	SW2	18	$\overline{\text{LE}}$
5	SW1	19	CL
6	SW1	20	DOUT
7	SW0	21	SW7
8	SW0	22	SW7
9	VPP	23	SW6
10	VNN	24	SW6
11	N/C	25	SW5
12	GND	26	SW5
13	VDD	27	SW4
14	N/C	28	SW4

28-Lead PLCC Package Outline (PJ)
.453x.453in. body, .180in. height (max), .050in. pitch

Top View

Vertical Side View

Horizontal Side View

View A

Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Actual shape of this feature may vary.

Symbol		A	A1	A2	b	b1	D	D1	E	E1	e
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.485	.450	.485	.450	.050 BSC
	NOM	.172	.105	-	-	-	.490	.453	.490	.453	
	MAX	.180	.120	.083	.021	.032	.495	.456	.495	.456	

JEDEC Registration MS-018, Variation AB, Issue A, June, 1993.
Drawings not to scale.
Supertex Doc. #: *DSPD-28PLCCPJ, Version A092408.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

Supertex inc.

1235 Bordeaux Drive, Sunnyvale, CA 94089
Tel: 408-222-8888
www.supertex.com