

54AC/74AC379 • 54ACT/74ACT379

Quad Parallel Register With Enable

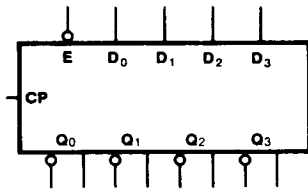
Description

The 'AC/'ACT379 is a 4-bit register with a buffered common Enable. This device is similar to the 'AC/'ACT175 but features the common Enable rather than common Master Reset.

- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Buffered Common Enable Input
- True and Complement Outputs
- Outputs Source/Sink 24 mA
- 'ACT379 has TTL-Compatible Inputs

Ordering Code: See Section 6

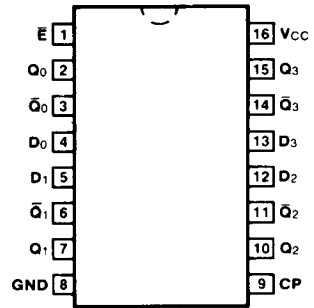
Logic Symbol



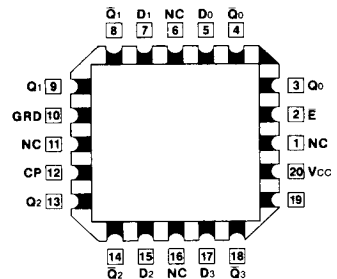
Pin Names

- E Enable Input
- D₀ - D₃ Data Inputs
- CP Clock Pulse Input
- Q₀ - Q₃ Flip-Flop Outputs
- \bar{Q}_0 - \bar{Q}_3 Complement Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC and PCC

AC379 • ACT379

Functional Description

The 'AC/ACT379 consists of four edge-triggered D-type flip-flops with individual D inputs and Q and \bar{Q} outputs. The Clock (CP) and Enable (\bar{E}) inputs are common to all flip-flops. When the \bar{E} input is HIGH, the register will retain the present data

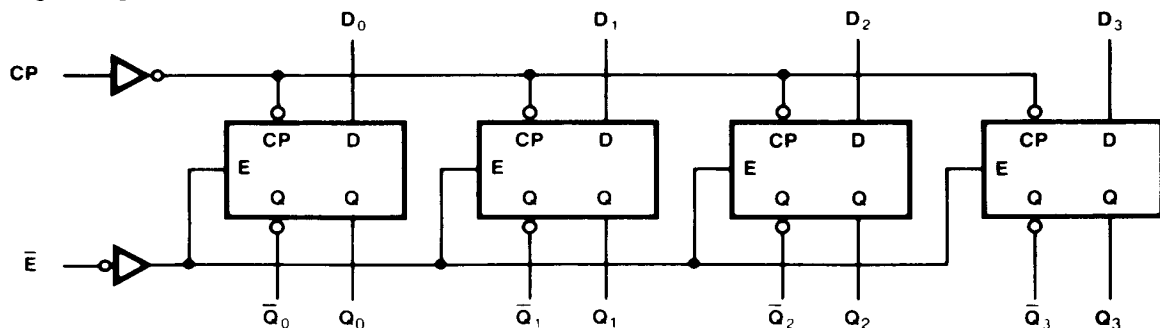
independent of the CP input. When the \bar{E} is LOW, new data is entered into the register on the LOW-to-HIGH transition of the CP input.

Truth Table

Inputs			Outputs	
\bar{E}	CP	D _n	Q _n	\bar{Q}_n
H	⌋	X	NC	NC
L	⌋	H	H	L
L	⌋	L	L	H

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 ⌋ = LOW-to-HIGH Transition
 NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I _{CC}	Maximum Quiescent Supply Current	160	80	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = Worst Case
I _{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	V _{IN} = V _{CC} or Ground, V _{CC} = 5.5 V, T _A = 25°C
I _{CC(T)}	Maximum Additional I _{CC} /Input ('ACT379)	1.6	1.5	mA	V _{IN} = V _{CC} - 2.1 V, V _{CC} = 5.5 V, T _A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC			54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF			TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
fmax	Maximum Clock Frequency	3.3 5.0	118	160					MHz	3-3	
tPLH	Propagation Delay CP to Qn, Qn	3.3 5.0	8.5	7.0					ns	3-6	
tPHL	Propagation Delay CP to Qn, Qn	3.3 5.0	8.5	6.0					ns	3-6	

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC		54AC		74AC		Units	Fig. No.
			TA = +25°C CL = 50 pF		TA = -55°C to +125°C CL = 50 pF		TA = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum						
ts	Setup Time, HIGH or LOW Dn to CP	3.3 5.0	4.5 3.0						ns	3-9
th	Hold Time, HIGH or LOW Dn to CP	3.3 5.0	0 0						ns	3-9
ts	Setup Time, HIGH or LOW E to CP	3.3 5.0	4.5 3.0						ns	3-9
th	Hold Time, HIGH or LOW E to CP	3.3 5.0	3.0 2.0						ns	3-9
tw	CP Pulse Width, HIGH or LOW	3.3 5.0	5.5 4.0						ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Characteristics

Symbol	Parameter	V _{cc} * (V)	74ACT			54ACT		74ACT		Units	Fig. No.
			T _A = +25°C CL = 50 pF			T _A = -55°C to +125°C CL = 50 pF		T _A = -40°C to +85°C CL = 50 pF			
			Min	Typ	Max	Min	Max	Min	Max		
f _{max}	Maximum Clock Frequency	5.0		160					MHz	3-3	
t _{PLH}	Propagation Delay CP to Q _n , Q _n	5.0		7.0					ns	3-6	
t _{PHL}	Propagation Delay CP to Q _n , Q _n	5.0		6.0					ns	3-6	

*Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Symbol	Parameter	V _{cc} * (V)	74ACT		54ACT		74ACT		Units	Fig. No.
			T _A = +25°C CL = 50 pF		T _A = -55°C to +125°C CL = 50 pF		T _A = -40°C to +85°C CL = 50 pF			
			Typ	Guaranteed Minimum						
t _s	Setup Time, HIGH or LOW D _n to CP	5.0	3.0						ns	3-9
t _h	Hold Time, HIGH or LOW D _n to CP	5.0	0						ns	3-9
t _s	Setup Time, HIGH or LOW E to CP	5.0	3.0						ns	3-9
t _h	Hold Time, HIGH or LOW E to CP	5.0	2.0						ns	3-9
t _w	CP Pulse Width, HIGH or LOW	5.0	4.0						ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT	Units	Conditions
		Typ		
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.5 V
C _{PD}	Power Dissipation Capacitance		pF	V _{CC} = 5.5 V