REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16	17	18	19	20	21	22	23											
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Kenneth Rice	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Jeff Bowling	
	APPROVED BY Raymond Monnin	MICROCIRCUIT, MEMORY, DIGITAL, CMOS, FIELD PROGRAMMABLE GATE ARRAY, 20,000 GATES, MONOLITHIC SILICON
	DRAWING APPROVAL DATE 99 - 01 - 22	
	REVISION LEVEL	SIZE: A; CAGE CODE: 67268; **5962-99527**
		SHEET 1 OF 23

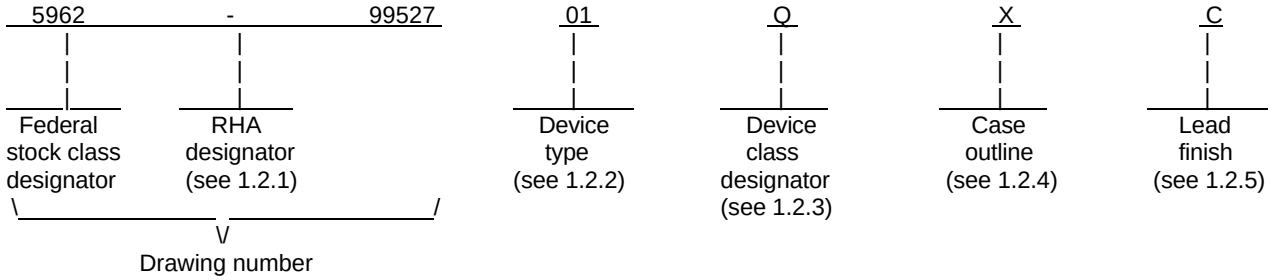
DSCC FORM 2233
APR 97

5962-E091-99

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Bin speed
01	A32200DX	20,000 gate, field programmable gate array	227 ns
02	A32200DX-1	20,000 gate, field programmable gate array	192 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See Figure 1 1/	256	Ceramic Quad Flat Pack
Y	See Figure 1 1/	208	Ceramic Quad Flat Pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ All exposed metalized areas and leads are gold plated 100 microinches (2.5µm) min. thickness over 80 to 350 microinches (2.0 to 8.9 µm) thickness of nickel.

1.3 Absolute maximum ratings. 2/

DC supply voltage range (V_{DD})	-0.5 V dc to +7.0 V dc
Input voltage range (V_I)	-0.5 V dc to V_{DD} + 0.5 V dc
Output voltage range (V_O)	-0.5 V dc to V_{DD} + 0.5 V dc
I/O source sink current (I_{IO})	±20 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (θ_{JC})	
Case outline X and Y	10°C/W 3/
Maximum junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+4.5 V dc to +5.5 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent 4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ When a thermal resistance for this case is specified in MIL-STD-1835 that value shall supersede the value indicated herein.
4/ 100 percent test coverage of blank programmable logic devices.

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-95 - Standard Guide for the Measurement of Single Event Procedures from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103).

ELECTRONICS INDUSTRIES ALLIANCE (EIA)

JEDEC Standard No. 17 - A Standard Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Alliance, 2500 Wilson Blvd., Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s).

3.2.3.1 Unprogrammed devices. The truth table or test vectors for unprogrammed devices for contracts involving no altered item drawing is not part of this drawing. When required in screening (see 4.2 herein) or quality conformance inspection group A, B, C, D, or E (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of logic modules shall be utilized or at least 25 percent of the total logic modules shall be utilized for any altered item drawing pattern.

3.2.3.2 Programmed devices. The truth table or test vectors for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.11 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract.

3.11.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.11.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (pre-burn-in) electrical parameters through interim (post-burn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device classes M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is five devices with no failures on a minimum of ten worst case pins from each device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC standard number 17 may be used for reference.

e. Programmed device (see 3.2.3.2) - For device class M, subgroups 7, 8A, and 8B tests shall consist of verifying the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device. These tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.6 herein).

f. Unprogrammed devices shall be tested for programmability and dc and ac performance compliance to the requirements of group A, subgroups 1 and 7.

(1) A sample shall be selected from each wafer lot to satisfy programmability requirements. Eight devices shall be submitted to programming (see 3.2.3.1). If any device fails to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(2) These eight devices shall also be submitted to the requirements of the specified tests of group A, subgroups 1 and 7. If any device fails, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(3a) Eight devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9 for binning circuit delay only. If any device fails, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(3b) If the binning circuit is tested on 100 percent of the products, then the above requirement (3A) is met.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

TABLE I. Electrical performance characteristics.

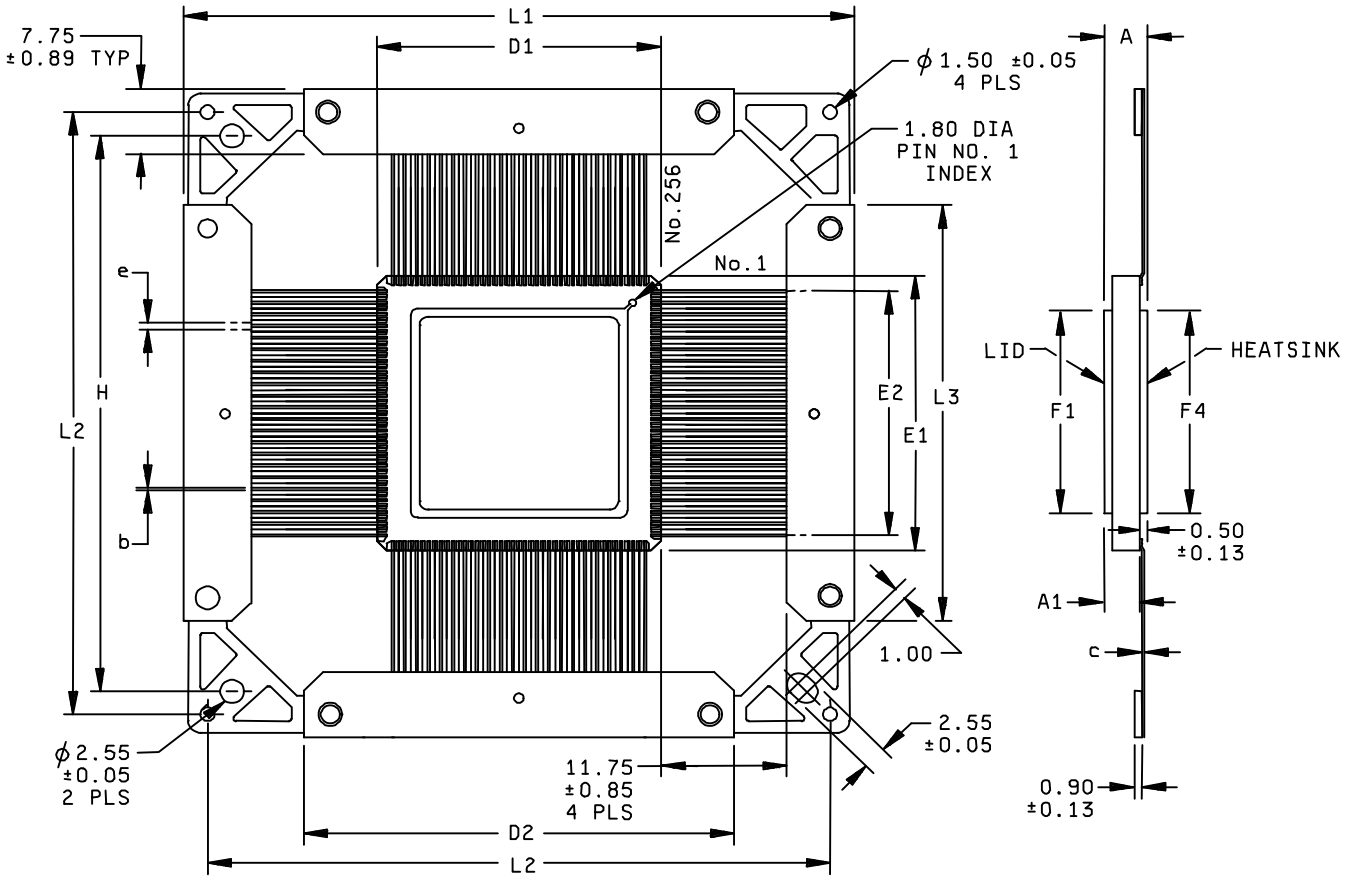
Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ $-55^{o}C \le T_C \le +125^{o}C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
High Level output voltage	V_{OH}	Test one output at a time, V_{CC} = 4.5 V, I_{OH} = -4.0 mA	1, 2, 3	All	3.7		V
Low level output voltage	V_{OL}	Test one output at a time, V_{CC} = 4.5 V, I_{OL} = 6.0 mA	1, 2, 3	All		0.4	V
Low level input voltage	V_{IL}		1, 2, 3	All	-0.3	0.8	V
High level input voltage	V_{IH}		1, 2, 3	All	2.0	V_{CC} +0.3	V
Standby supply current	I_{DD}	Outputs unloaded, V_{CC} = 5.5 V, $V_{IN} = V_{CC}$ or GND	1, 2, 3	All		25	mA
Input leakage current	I_{IL}	V_{CC} = 5.5 V, $V_{IN} = V_{CC}$ or GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, $V_O = V_{CC}$ or GND	1, 2, 3	All	-10	10	µA
I/O terminal capacitance	$C_{I/O}$	See 4.4.1c, f= 1.0 Mhz, V_{OUT} = 0 V	4	All		20	pF
Functional tests	FT 2/	See 4.4.1e, V_O = 0 V, V_{CC} = 4.5 V	7, 8A, 8B	All			
Binning circuit delay	t_{PBLH}, t_{PBHL}	See figure 3, V_{IL} = 0 V, V_{IH} = 3.0 V, V_{CC} = 4.5 V, V_{OUT} = 1.5 V 3/	9, 10, 11	01		227	ns
				02		192	

1/ All tests shall be performed under the worst case condition unless otherwise specified

2/ Devices are functionally tested using a serial scan test method. Data is shifted into the SDI pin and the DCLK pin is used as a clock. The data is used to drive the inputs of the internal logic and I/O modules, allowing a complete functional test to be performed. The outputs of the module can be read by shifting out the output response or by monitoring the PRA, PRB, or SDO pins. These tests form a part of the manufacturer's test tape and shall be maintained and available at the approved source(s) of supply upon request by preparing or acquiring activity.

3/ Binning circuit delay is defined as the input-to-output delay of a special path called the "binning circuit". The binning circuit consists of one input buffer plus 16 combinatorial logic modules plus one output buffer. The logic modules are distributed along the left side of the device. These modules are configured as non-inverting buffers and are connected through programmed antifuses with typical capacitive loading.

Case outline X

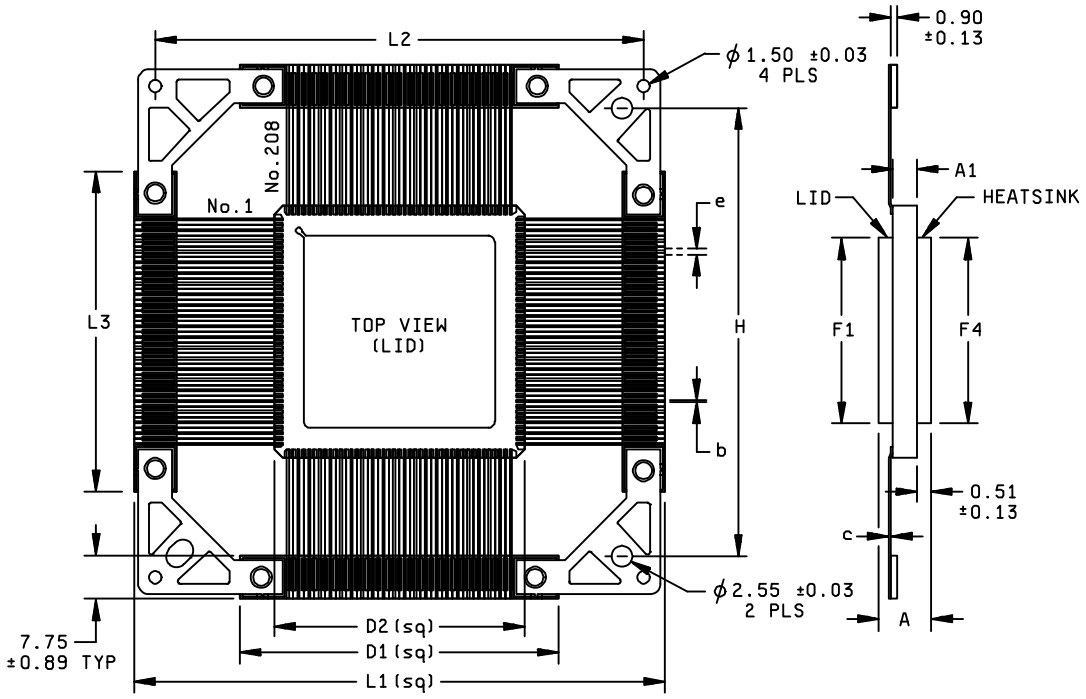


	Min.	Norm.	Max.
A	2.78	3.17	3.56
A1	2.43	2.79	3.15
b	0.18	0.20	0.22
c	0.11	0.15	0.17
D1/ E1	35.64	36.00	36.36
D2/ E2	31.5 BSC		
e	0.50 BSC		
F1	22.98	23.11	23.23
F4	22.61	22.86	23.11
L1	74.60	75.00	75.40
L2	69.87	70.00	70.13
L3	55.80	56.30	56.80
H	65.77	65.90	66.03
Weight	20gm Typ.		

Note: All dimensions are in millimeters.

Figure 1. Case outlines.

Case outline Y



	Min.	Norm.	Max.
A	2.79	3.18	3.57
A1	2.44	2.80	3.16
b	0.18	0.20	0.22
c	0.08	0.13	0.18
D1	28.96	29.21	29.46
D2	25.5 BSC		
e	0.50 BSC		
F1	22.98	23.11	23.23
F4	22.61	22.86	23.11
L1	74.60	75.00	75.40
L2	69.87	70.00	70.13
L3	55.80	56.30	56.80
H	65.77	65.90	66.03
Weight	18.5gm Typ.		

Note: All dimensions are in millimeters.

FIGURE 1. Case outline – Continued.

Case outline X

Device Types	All	Device Types	All	Device Types	All
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal number	Terminal Symbol
1	NC	44	I/O	87	WD, I/O
2	GND	45	I/O	88	WD, I/O
3	I/O	46	I/O	89	I/O
4	I/O	47	I/O	90	I/O
5	I/O	48	GND	91	I/O
6	I/O	49	I/O	92	I/O
7	I/O	50	I/O	93	I/O
8	I/O	51	I/O	94	I/O
9	I/O	52	I/O	95	VCC
10	GND	53	I/O	96	VCC
11	I/O	54	I/O	97	GND
12	I/O	55	I/O	98	GND
13	I/O	56	I/O	99	I/O
14	I/O	57	I/O	100	I/O
15	I/O	58	I/O	101	I/O
16	I/O	59	I/O	102	I/O
17	I/O	60	VCC	103	I/O
18	I/O	61	GND	104	I/O
19	I/O	62	GND	105	WD, I/O
20	I/O	63	NC	106	WD, I/O
21	I/O	64	NC	107	I/O
22	I/O	65	NC	108	I/O
23	I/O	66	I/O	109	WD, I/O
24	I/O	67	TDO,SDO, I/O	110	WD, I/O
25	I/O	68	I/O	111	I/O
26	VCC	69	WD, I/O	112	QCLKA,I/O
27	I/O	70	WD, I/O	113	I/O
28	I/O	71	I/O	114	GND
29	VSV,VCC	72	VCC	115	I/O
30	VCC	73	I/O	116	I/O
31	GND	74	I/O	117	I/O
32	VPP,VCC	75	I/O	118	I/O
33	VKS,GND	76	WD, I/O	119	VCC
34	TCK, I/O	77	GND	120	I/O
35	I/O	78	WD, I/O	121	WD, I/O
36	GND	79	I/O	122	WD, I/O
37	I/O	80	QCLKB,I/O	123	I/O
38	I/O	81	I/O	124	I/O
39	I/O	82	I/O	125	TDI, I/O
40	I/O	83	I/O	126	TMS, I/O
41	I/O	84	I/O	127	GND
42	I/O	85	I/O	128	NC
43	I/O	86	I/O	129	NC

FIGURE 2. Terminal connections.

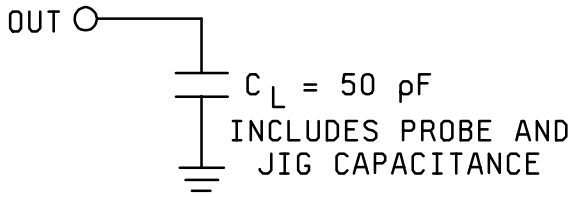
Device Types	All	Device Types	All	Device Types	All
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal number	Terminal Symbol
130	NC	173	I/O	215	WD, I/O
131	GND	174	I/O	216	WD, I/O
132	I/O	175	I/O	217	I/O
133	I/O	176	I/O	218	PRB,I/O
134	I/O	177	I/O	219	I/O
135	I/O	178	I/O	220	CLKB, I/O
136	I/O	179	I/O	221	I/O
137	I/O	180	GND	222	GND
138	I/O	181	I/O	223	GND
139	GND	182	I/O	224	VCC
140	I/O	183	I/O	225	VCC
141	I/O	184	I/O	226	I/O
142	I/O	185	I/O	227	CLKA,I/O
143	I/O	186	I/O	228	I/O
144	I/O	187	I/O	229	PRA,I/O
145	I/O	188	MODE	230	I/O
146	I/O	189	VCC	231	I/O
147	I/O	190	GND	232	WD, I/O
148	I/O	191	NC	233	WD, I/O
149	I/O	192	NC	234	I/O
150	I/O	193	NC	235	I/O
151	I/O	194	I/O	236	I/O
152	I/O	195	DCLK,I/O	237	I/O
153	I/O	196	I/O	238	I/O
154	I/O	197	I/O	239	I/O
155	VCC	198	I/O	240	QCLKD,I/O
156	I/O	199	WD, I/O	241	I/O
157	I/O	200	WD, I/O	242	WD, I/O
158	VSV,VCC	201	VCC	243	GND
159	VCC	202	I/O	244	WD, I/O
160	GND	203	I/O	245	I/O
161	I/O	204	I/O	246	I/O
162	I/O	205	I/O	247	I/O
163	I/O	206	GND	248	VCC
164	I/O	207	I/O	249	I/O
165	GND	208	I/O	250	WD, I/O
166	I/O	209	QCLKC,I/O	251	WD, I/O
167	I/O	210	I/O	252	I/O
168	I/O	211	WD, I/O	253	SDI, I/O
169	I/O	212	WD, I/O	254	I/O
170	VCC	213	I/O	255	GND
171	I/O	214	I/O	256	NC
172	I/O				

FIGURE 2. Terminal connections - Continued.

Device Types	All	Device Types	All	Device Types	All	Device Types	All
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	GND	53	GND	105	GND	157	GND
2	VCC	54	TMS, I/O	106	VCC	158	I/O
3	MODE	55	TDI, I/O	107	I/O	159	SDI, I/O
4	I/O	56	I/O	108	I/O	160	I/O
5	I/O	57	I/O (WD)	109	I/O	161	I/O (WD)
6	I/O	58	I/O (WD)	110	I/O	162	I/O (WD)
7	I/O	59	I/O	111	I/O	163	I/O
8	I/O	60	VCC	112	I/O	164	VCC
9	I/O	61	I/O	113	I/O	165	I/O
10	I/O	62	I/O	114	I/O	166	I/O
11	I/O	63	I/O	115	I/O	167	I/O
12	I/O	64	I/O	116	I/O	168	I/O (WD)
13	I/O	65	QCLKA, I/O	117	I/O	169	I/O (WD)
14	I/O	66	I/O (WD)	118	I/O	170	I/O
15	I/O	67	I/O (WD)	119	I/O	171	QCLKD, I/O
16	I/O	68	I/O	120	I/O	172	I/O
17	VCC	69	I/O	121	I/O	173	I/O
18	I/O	70	I/O (WD)	122	I/O	174	I/O
19	I/O	71	I/O (WD)	123	I/O	175	I/O
20	I/O	72	I/O	124	I/O	176	I/O (WD)
21	I/O	73	I/O	125	I/O	177	I/O (WD)
22	GND	74	I/O	126	GND	178	PRA, I/O
23	I/O	75	I/O	127	I/O	179	I/O
24	I/O	76	I/O	128	TCK, I/O	180	CLKA, I/O
25	I/O	77	I/O	129	VKS, GND	181	I/O
26	I/O	78	GND	130	VPP, VCC	182	VCC
27	GND	79	VCC	131	GND	183	VCC
28	VCC	80	VCC	132	VCC	184	GND
29	VSV, VCC	81	I/O	133	VSV, VCC	185	I/O
30	I/O	82	I/O	134	I/O	186	CLKB, I/O
31	I/O	83	I/O	135	I/O	187	I/O
32	VCC	84	I/O	136	VCC	188	PRB, I/O
33	I/O	85	I/O (WD)	137	I/O	189	I/O
34	I/O	86	I/O (WD)	138	I/O	190	I/O (WD)
35	I/O	87	I/O	139	I/O	191	I/O (WD)
36	I/O	88	I/O	140	I/O	192	I/O
37	I/O	89	I/O	141	I/O	193	I/O
38	I/O	90	I/O	142	I/O	194	I/O (WD)
39	I/O	91	QCLKB, I/O	143	I/O	195	I/O (WD)
40	I/O	92	I/O	144	I/O	196	QCLKC, I/O
41	I/O	93	I/O (WD)	145	I/O	197	I/O
42	I/O	94	I/O (WD)	146	I/O	198	I/O
43	I/O	95	I/O	147	I/O	199	I/O
44	I/O	96	I/O	148	I/O	200	I/O
45	I/O	97	I/O	149	I/O	201	I/O
46	I/O	98	VCC	150	GND	202	VCC
47	I/O	99	I/O	151	I/O	203	I/O (WD)
48	I/O	100	I/O (WD)	152	I/O	204	I/O (WD)
49	I/O	101	I/O (WD)	153	I/O	205	I/O
50	I/O	102	I/O	154	I/O	206	I/O
51	I/O	103	TDO, SDO, I/O	155	I/O	207	DCLK, I/O
52	GND	104	I/O	156	I/O	208	I/O

FIGURE 2. Terminal connections - Continued.

TEST LOAD



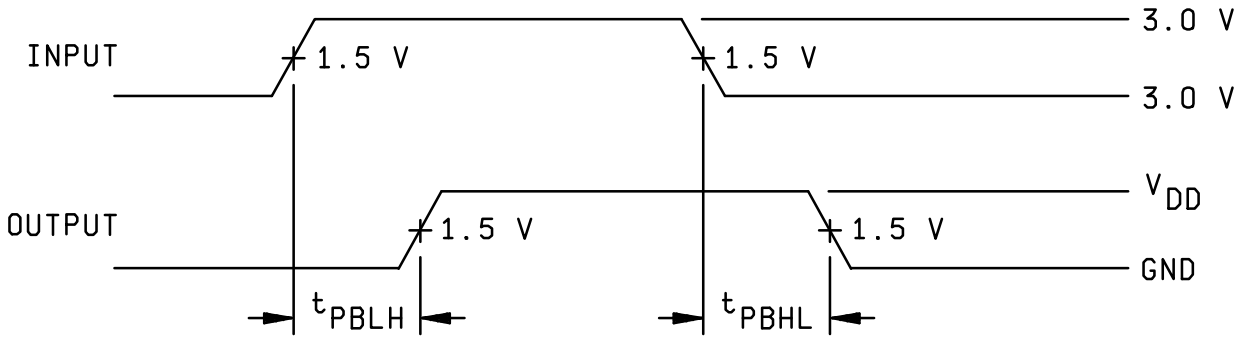


FIGURE 3. Switching test circuit and waveforms.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7*)
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7*)
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A,8B,9,10,11	1*, 2, 3, 7*, 8A,8B, 9, 10, 11	1*, 2, 3, 7*, 8A,8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11)
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the functionality for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1c.
6/) indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{DD}	±10% of specified value of table IA
I_{OZ}	±10% of specified value of table IA
t_{PBLH}, t_{PBHL}	±10 ns

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

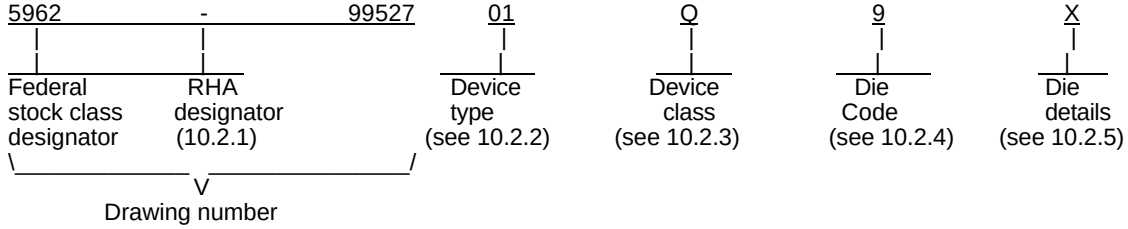
Appendix A

Appendix A forms a part of SMD 5962-99527

10. Scope

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under two high reliability class levels (class Q and M) and space application (class V). QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. When available a choice of class levels are reflected in the PIN.

10.2 PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Bin speed
01	32200DX	20,000 gate, field programmable gate array	251 ns

10.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

10.2.4 Die code. The die code designator shall be a number 9 for all devices supplied as die only with no case outline.

10.2.5 Die details. The die details designation shall be a unique which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.5.1 Die physical dimensions.

Device type	Die size (X,Y)	Die thickness	Die Detail	Figure Number
01	503mils, 474mils	19±1 mils	A	A-1

10.2.5.2 Die bonding pad locations and electrical functions.

Device type	Die Detail	Figure Number
01	A	A-1

10.2.5.3 Interface materials.

Device type	Top metalization	Backside metalization	Die Detail	Figure Number
01	Ti-cap+Al/Cu/Si,9-12kA	None (backgrind)	A	A-1

10.2.5.4 Assembly related information.

Device type	Glassivation	Die Detail	Figure Number
01	Ox/Nitride	A	A-1

10.2.5.4 Wafer fab locations

Device type	Source	Die Detail	Figure Number
01	Chartered Semiconductor, Singapore	A	A-1

10.3 Absolute maximum ratings.
See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions.
See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS.

See paragraph 2.1, 2.2 and 2.3 within the body of this drawing for details.

30. REQUIREMENTS.

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-389535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The Modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physical dimensions. The die physical dimensions shall be specified in 10.2.5.1 and on figures A-1.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.5.2 and on figures A-1.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.5.3 and on figures A.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.5.4 and figures A-1.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics are as specified in table 1 of the body of this document.

30.4 Electrical test requirements. The electrical test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table 1.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be "QML" or "Q" as required by MIL-PRF-38535 and "M" for device class M in according to MIL-PRF-38535, appendix A.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

30.8 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

30.9 Unprogrammed die delivered to the user. All testing shall be verified through wafer probe test as defined in 40.2.

30.10 Manufacturer-programmed die delivered to the user. The programming integrity test shall be performed during programming. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria within MIL-STD-883 test method 5007.
b) 100% wafer probe (see paragraph 30.4)
c) 100% internal visual inspection to the applicable class M, Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

40.3 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed including groups A, B, C, D and E inspections and as specified herein except where MIL-PRF-38535 permits alternate in-line control testing.

40.3.1 Programmability. See 4.4.1.e for packaged die.

40.3.2 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535.

a) End point electrical testing of packaged die shall be as specified in table IIA.
b) For device class M, the devices shall be subjected to radiation hardness assured testes as specified in MIL-PRF-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table I at T_A=+25°±5°C, after exposure, to the subgroups specified in table IIA herein.

50. DIE CARRIER

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

60. NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit application (original equipment), design applications and logistics purposes.

60.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

60.3 Substitutability. Device class Q devices will replace device class M devices.

60.4 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

60.5 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614)-692-0525.

60.6 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0674.

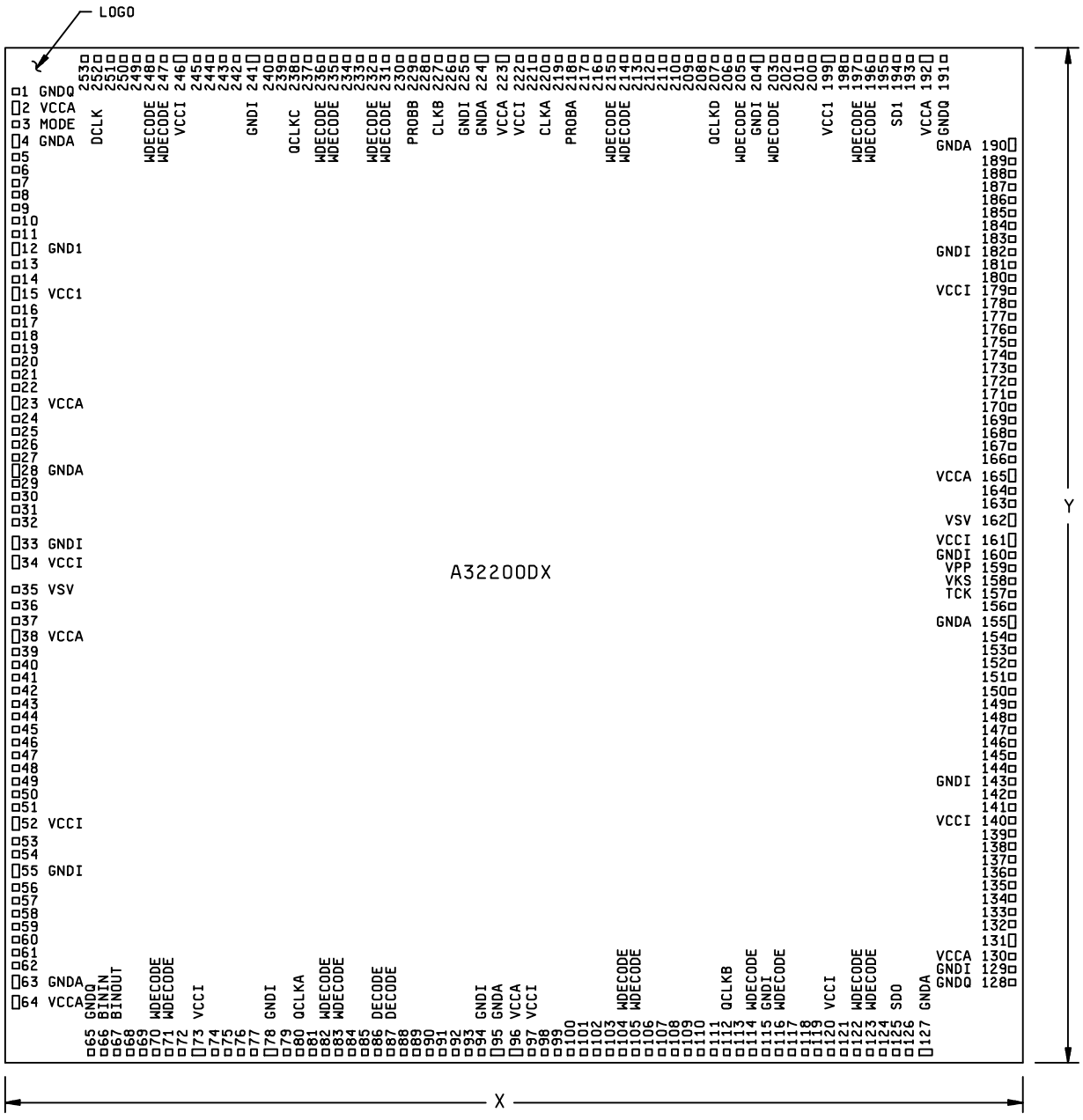


Figure A-1. Bond Pad Functions and Locations

Bond Pad Functions and Locations

Pad #	Name	Center-X	Center-Y	Pad #	Name	Center-X	Center-Y
1	GND	-6146	5540	43	I/O	-6146	-1666
2	VCC	-6146	5342	44	I/O	-6146	-1850
3	MODE	-6146	5142	45	I/O	-6146	-2033
4	GND	-6146	4968	46	I/O	-6146	-2216
5	I/O	-6146	4795	47	I/O	-6146	-2400
6	I/O	-6146	4679	48	I/O	-6146	-2583
7	I/O	-6146	4551	49	I/O	-6146	-2767
8	I/O	-6146	4404	50	I/O	-6146	-2950
9	I/O	-6146	4256	51	I/O	-6146	-3134
10	I/O	-6146	4109	52	VCC	-6146	-3345
11	I/O	-6146	3962	53	I/O	-6146	-3556
12	GND	-6146	3787	54	I/O	-6146	-3739
13	I/O	-6146	3612	55	GND	-6146	-3950
14	I/O	-6146	3465	56	I/O	-6146	-4161
15	VCC	-6146	3290	57	I/O	-6146	-4345
16	I/O	-6146	3116	58	I/O	-6146	-4528
17	I/O	-6146	2968	59	I/O	-6146	-4674
18	I/O	-6146	2821	60	I/O	-6146	-4795
19	I/O	-6146	2674	61	I/O	-6146	-4916
20	I/O	-6146	2527	62	I/O	-6146	-5037
21	I/O	-6146	2380	63	GND	-6146	-5236
22	I/O	-6146	2233	64	VCC	-6146	-5482
23	VCC	-6146	2027	65	GND	-5854	-5811
24	I/O	-6146	1846	66	TMS, BININ, I/O	-5713	-5811
25	I/O	-6146	1723	67	TDI, BINOUT,I/O	-5573	-5811
26	I/O	-6146	1600	68	I/O	-5433	-5811
27	I/O	-6146	1477	69	I/O	-5288	-5811
28	GND	-6146	1296	70	I/O(WD)	-5100	-5811
29	I/O	-6146	1115	71	I/O(WD)	-4913	-5811
30	I/O	-6146	992	72	I/O	-4725	-5811
31	I/O	-6146	869	73	VCC	-4510	-5811
32	I/O	-6146	747	74	I/O	-4294	-5811
33	GND	-6146	354	75	I/O	-4107	-5811
34	VCC	-6146	176	76	I/O	-3919	-5811
35	VSV, VCC	-6146	-262	77	I/O	-3731	-5811
36	I/O	-6146	-385	78	GND	-3516	-5811
37	I/O	-6146	-508	79	I/O	-3301	-5811
38	VCC	-6146	-689	80	QCLKA, I/O	-3113	-5811
39	I/O	-6146	-932	81	I/O	-2926	-5811
40	I/O	-6146	-1116	82	I/O(WD)	-2738	-5811
41	I/O	-6146	-1299	83	I/O(WD)	-2550	-5811
42	I/O	-6146	-1483	84	I/O	-2363	-5811

Note - All X-Y locations are in millimeters.

Figure A-1. Bond Pad Functions and Locations

Bond Pad Functions and Locations

Pad #	Name	Center-X	Center-Y
85	I/O	-2175	-5811
86	I/O(WD)	-1987	-5811
87	I/O(WD)	-1800	-5811
88	I/O	-1612	-5811
89	I/O	-1424	-5811
90	I/O	-1237	-5811
91	I/O	-1049	-5811
92	I/O	-861	-5811
93	I/O	-674	-5811
94	GND	-459	-5811
95	GND	-181	-5811
96	VCC	80	-5811
97	VCC	304	-5811
98	I/O	464	-5811
99	I/O	652	-5811
100	I/O	840	-5811
101	I/O	1027	-5811
102	I/O	1215	-5811
103	I/O	1403	-5811
104	I/O(WD)	1591	-5811
105	I/O(WD)	1779	-5811
106	I/O	1966	-5811
107	I/O	2154	-5811
108	I/O	2342	-5811
109	I/O	2530	-5811
110	I/O	2717	-5811
111	I/O	2905	-5811
112	QCLKB, I/O	3093	-5811
113	I/O	3281	-5811
114	I/O(WD)	3468	-5811
115	GND	3684	-5811
116	I/O(WD)	3899	-5811
117	I/O	4087	-5811
118	I/O	4275	-5811
119	I/O	4462	-5811
120	VCC	4678	-5811
121	I/O	4880	-5811
122	I/O(WD)	5020	-5811
123	I/O(WD)	5160	-5811
124	I/O	5301	-5811
125	TDO, SDO, I/O	5472	-5811
126	I/O	5612	-5811
127	GND	5810	-5811
128	GND	6146	-5540
129	GND	6146	-5372
130	VCC	6146	-5163
131	I/O	6146	-4984
132	I/O	6146	-4863
133	I/O	6146	-4742
134	I/O	6146	-4615
135	I/O	6146	-4468
136	I/O	6146	-4316
137	I/O	6146	-4164
138	I/O	6146	-4012
139	I/O	6146	-3860
140	VCC	6146	-3680
141	I/O	6146	-3501
142	I/O	6146	-3349
143	GND	6146	-3169
144	I/O	6146	-2989
145	I/O	6146	-2837
146	I/O	6146	-2685
147	I/O	6146	-2533
148	I/O	6146	-2381
149	I/O	6146	-2229
150	I/O	6146	-2077
151	I/O	6146	-1939
152	I/O	6146	-1801
153	I/O	6146	-1663
154	I/O	6146	-1525
155	GND	6146	-1315
156	I/O	6146	-1048
157	TCK, I/O	6146	-896
158	VKS, GND	6146	-546
159	VPP, VCC	6146	-171
160	GND	6146	179
161	VCC	6146	386
162	VSV, VCC	6146	566
163	I/O	6146	718
164	I/O	6146	870
165	VCC	6146	1080
166	I/O	6146	1290
167	I/O	6146	1442
168	I/O	6146	1594

Note - All X-Y locations are in millimeters.

Figure A-1. Bond Pad Functions and Locations continued

Bond Pad Functions and Locations

Pad #	Name	Center-X	Center-Y
169	I/O	6146	1746
170	I/O	6146	1899
171	I/O	6146	2051
172	I/O	6146	2203
173	I/O	6146	2355
174	I/O	6146	2507
175	I/O	6146	2659
176	I/O	6146	2811
177	I/O	6146	2963
178	I/O	6146	3115
179	VCC	6146	3295
180	I/O	6146	3475
181	I/O	6146	3627
182	GND	6146	3806
183	I/O	6146	3986
184	I/O	6146	4138
185	I/O	6146	4290
186	I/O	6146	4431
187	I/O	6146	4563
188	I/O	6146	4857
189	I/O	6146	5280
190	GND	6146	5482
191	GND	5874	5811
192	VCC	5560	5811
193	I/O	5358	5811
194	SDI, I/O	5228	5811
195	I/O	5098	5811
196	I/O(WD)	4951	5811
197	I/O(WD)	4775	5811
198	I/O	4600	5811
199	VCC	4397	5811
200	I/O	4195	5811
201	I/O	4019	5811
202	I/O	3844	5811
203	I/O(WD)	3669	5811
204	GND	3466	5811
205	I/O(WD)	3263	5811
206	I/O	3088	5811
207	QCLKD, I/O	2913	5811
208	I/O	2737	5811
209	I/O	2562	5811
210	I/O	2387	5811

Pad#	Name	Center-X	Center-Y
211	I/O	2212	5811
212	I/O	2037	5811
213	I/O	1861	5811
214	I/O	1686	5811
215	I/O(WD)	1539	5811
216	I/O(WD)	1393	5811
217	I/O	1246	5811
218	PRA, I/O	1099	5811
219	I/O	940	5811
220	CLKA, I/O	793	5811
221	I/O	646	5811
222	VCC	406	5811
223	VCC	90	5811
224	GND	-184	5811
225	GND	-599	5811
226	I/O	-816	5811
227	CLKB, I/O	-1005	5811
228	I/O	-1194	5811
229	PRB, I/O	-1384	5811
230	I/O	-1586	5811
231	I/O(WD)	-1775	5811
232	I/O(WD)	-1964	5811
233	I/O	-2153	5811
234	I/O	-2342	5811
235	I/O(WD)	-2531	5811
236	I/O(WD)	-2720	5811
237	I/O	-2909	5811
238	QCLKC, I/O	-3099	5811
239	I/O	-3288	5811
240	I/O	-3477	5811
241	GND	-3694	5811
242	I/O	-3910	5811
243	I/O	-4099	5811
244	I/O	-4289	5811
245	I/O	-4478	5811
246	VCC	-4694	5811
247	I/O(WD)	-4911	5811
248	I/O(WD)	-5100	5811
249	I/O	-5245	5811
250	I/O	-5370	5811
251	I/O	-5495	5811
252	DCLK, I/O	-5713	5811
253	I/O	-5854	5811

Note - All X-Y locations are in millimeters.

Figure A-1. Bond Pad Functions and Locations continued

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 99 - 01 - 22

Approved sources of supply for SMD 5962-99527 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9952701QXC	0J4Z0	A32200DX-CQ256B
5962-9952701QYC	0J4Z0	A32200DX-CQ208B
5962-9952702QXC	0J4Z0	A32200DX-1CQ256B
5962-9952702QYC	0J4Z0	A32200DX-1CQ208B
5962-9952701Q9A	0J4Z0	A32200DX-DIE

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0J4Z0	Actel Corporation 955 East Arques Ave. Sunnyvale, CA94086