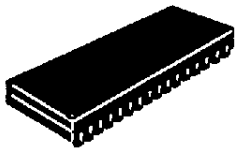
MCM6705A

32K x 9 Bit Static Random Access Memory



J PACKAGE
300 MIL SOJ
CASE 857–02

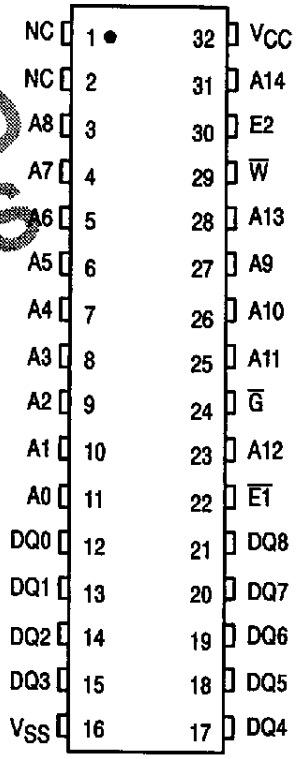
The MCM6705A is a 294,912 bit static random access memory organized as 32,768 words of 9 bits, fabricated using high performance silicon–gate BiCMOS technology. Static design eliminates the need for external clocks or timing strobes.

Output enable ($\overline{G}$) is a special control feature that provides increased system flexibility and eliminates bus contention problems.

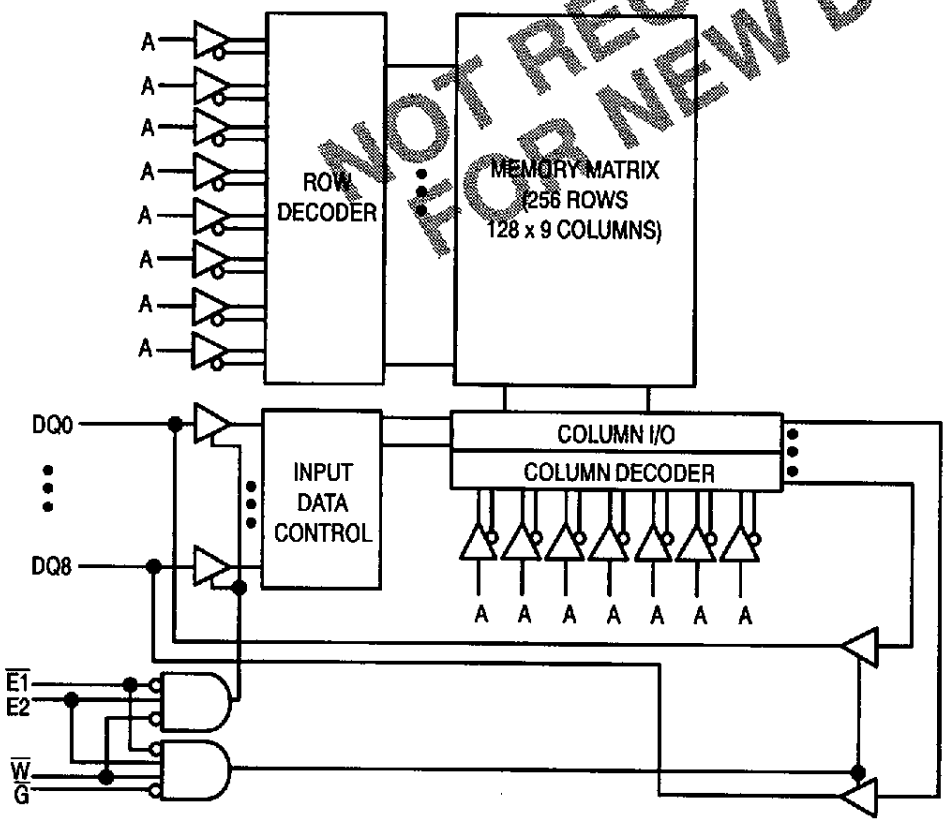
The MCM6705A is available in a 300 mil, 32 lead surface–mount SOJ package.

- Single 5.0 V ± 10% Power Supply
- Fully Static — No Clock or Timing Strobes Necessary
- All Inputs and Outputs Are TTL Compatible
- Three State Outputs
- Fast Access Times: MCM6705A–10 = 10 ns
  MCM6705A–12 = 12 ns

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0 – A14	Address
$\overline{W}$	Write Enable
$\overline{E1}$, E2	Chip Enable
$\overline{G}$	Output Enable
DQ0 – DQ8	Data Input/Output
V_{CC}	+ 5 V Power Supply
V_{SS}	Ground
NC	No Connection

TRUTH TABLE (X = Don't Care)

$\overline{E1}$	E2	$\overline{G}$	$\overline{W}$	Mode	V_{CC} Current	Output	Cycle
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High–Z	—
L	H	H	H	Output Disabled	I_{CCA}	High–Z	—
L	H	L	H	Read	I_{CCA}	D_{out}	Read Cycle
L	H	X	L	Write	I_{CCA}	High–Z	Write Cycle

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	– 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	– 0.5 to V_{CC} + 0.5	V
Output Current	I_{out}	± 30	mA
Power Dissipation	P_D	2.0	W
Temperature Under Bias	T_{bias}	– 10 to + 85	°C
Operating Temperature	T_A	0 to + 70	°C
Storage Temperature – Plastic	T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

This BiCMOS memory circuit has been designed to meet the dc and ac specifications shown in the tables, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow of at least 500 linear feet per minute is maintained.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.3*	V
Input Low Voltage	V_{IL}	– 0.5**	—	0.8	V

*V_{IH} (max) = V_{CC} + 0.3 V dc; V_{IH} (max) = V_{CC} + 2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.
**V_{IL} (min) = –0.5 V dc @ 30.0 mA; V_{IL} (min) = –2.0 V ac (pulse width ≤ 2.0 ns) or I ≤ 30.0 mA.

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit
Input Leakage Current (All Inputs, V_{in} = 0 to V_{CC})	$I_{lkg(I)}$	—	± 1.0	µA
Output Leakage Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL} or $\overline{G}$ = V_{IH}, V_{out} = 0 to V_{CC})	$I_{lkg(O)}$	—	± 1.0	µA
Output High Voltage (I_{OH} = – 4.0 mA)	V_{OH}	2.4	—	V
Output Low Voltage (I_{OL} = + 8.0 mA)	V_{OL}	—	0.4	V

POWER SUPPLY CURRENTS

Parameter	Symbol	MCM6705A–10	MCM6705A–12	Unit
AC Active Supply Current (I_{out} = 0 mA, V_{CC} = max, f = f_{max})	I_{CCA}	195	185	mA
AC Standby Current ($\overline{E1}$ = V_{IH} or E2 = V_{IL}, V_{CC} = max, f = f_{max})	I_{SB1}	125	120	mA
CMOS Standby Current (V_{CC} = max, f = 0 MHz, $\overline{E1}$ ≥ V_{CC} – 0.2 V, or E2 ≤ V_{SS} + 0.2 V, V_{in} ≤ V_{SS} + 0.2 V or ≥ V_{CC} – 0.2 V)	I_{SB2}	55	55	mA

CAPACITANCE (f = 1.0 MHz, dV = 3.0 V, T_A = 25°C, Periodically Sampled Rather Than 100% Tested)

Parameter	Symbol	Max	Unit
Address Input Capacitance	C_{in}	5	pF
Control Pin Input Capacitance ($\overline{E1}$, E2, $\overline{G}$, $\overline{W}$)	C_{in}	6	pF
I/O Capacitance	$C_{I/O}$	8	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ±10%, T_A = 0 to +70°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level ..... 1.5 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Measurement Reference Level ..... 1.5 V
Output Load ..... See Figure 1A

READ CYCLE (See Notes 1, 2, and 3)

Parameter	Symbol	MCM6705A–10		MCM6705A–12		Unit	Notes
		Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	10	—	12	—	ns	4
Address Access Time	t_{AVQV}	—	10	—	12	ns	
Chip Enable Access Time	t_{ELQV}	—	10	—	12	ns	
Output Enable Access Time	t_{GLQV}	—	5	—	6	ns	
Output Hold from Address Change	t_{AXQX}	3	—	3	—	ns	
Chip Enable Low to Output Active	t_{ELQX}	1	—	1	—	ns	5, 6, 7
Chip Enable High to Output High–Z	t_{EHQZ}	0	6	0	7	ns	5, 6, 7
Output Enable Low to Output Active	t_{GLQX}	0	—	0	—	ns	5, 6, 7
Output Enable High to Output High–Z	t_{GHQZ}	0	5	0	6	ns	5, 6, 7

NOTES:
1. $\overline{W}$ is high for read cycle.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ is represented by E in this table. E2 would require a transition opposite of $\overline{E1}$.
4. All read cycle timing is referenced from the last valid address to the first transitioning address.
5. At any given voltage and temperature, t_{EHQZ} max < t_{ELQX} min, and t_{GHQZ} max < t_{GLQX} min, both for a given device and from device to device.
6. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
7. This parameter is sampled and not 100% tested.
8. Device is continuously selected ($\overline{E1}$ = V_{IL}, E2 = V_{IH}, $\overline{G}$ = V_{IL}).
9. Addresses valid prior to or coincident with $\overline{E}$ going low.

AC TEST LOADS

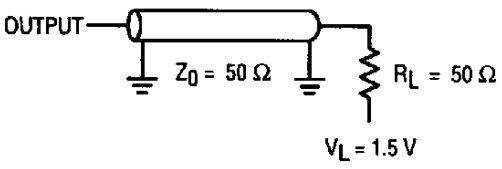


Figure 1A

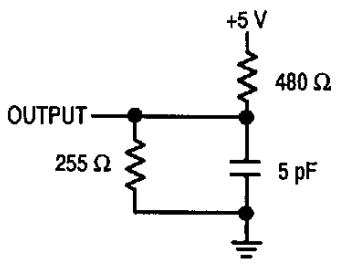
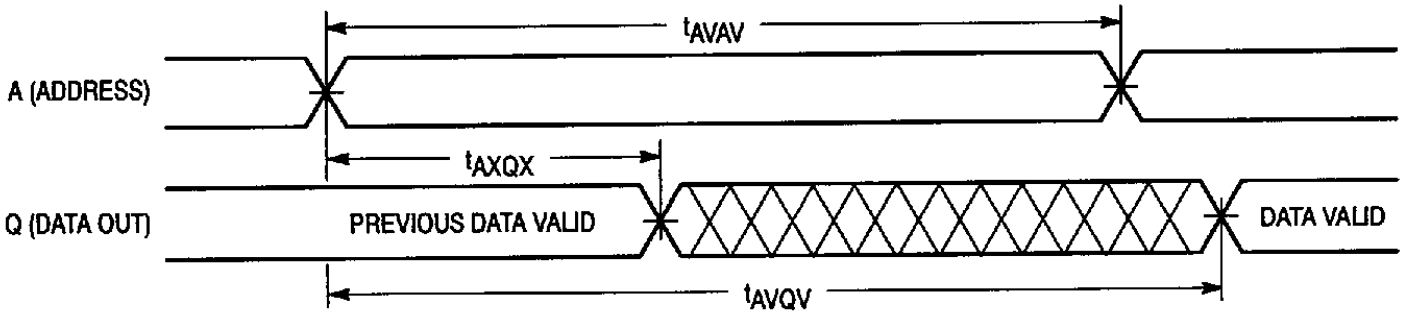


Figure 1B

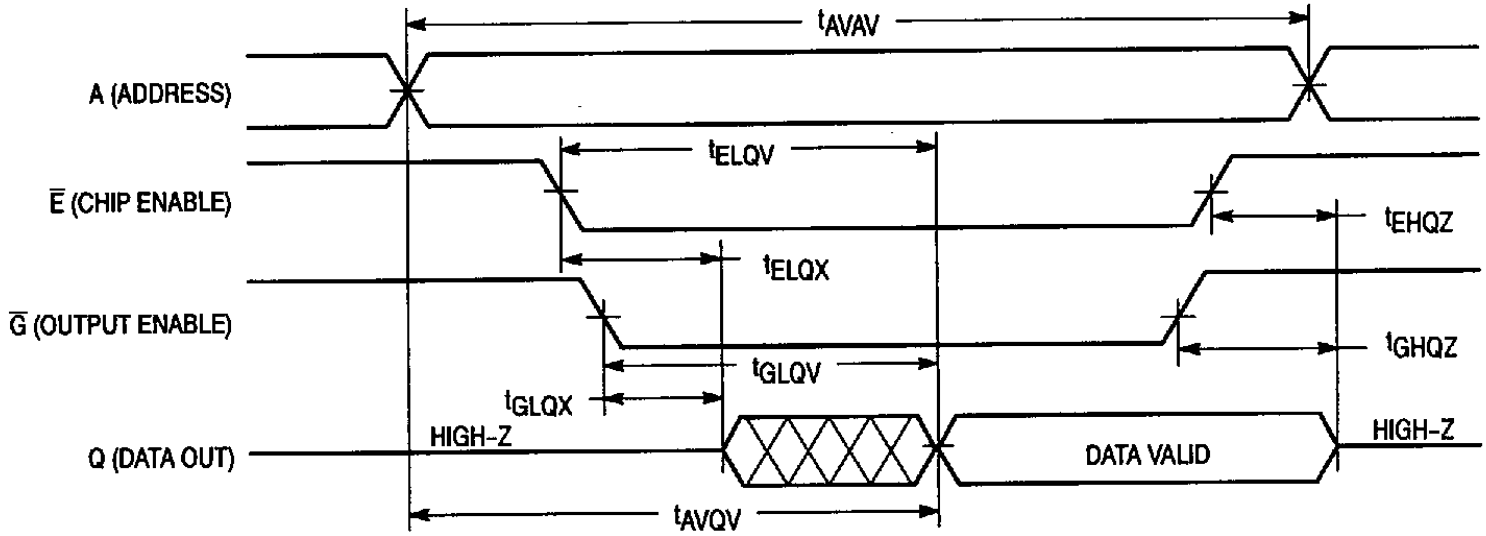
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE 1 (See Note 8)



READ CYCLE 2 (See Note 9)

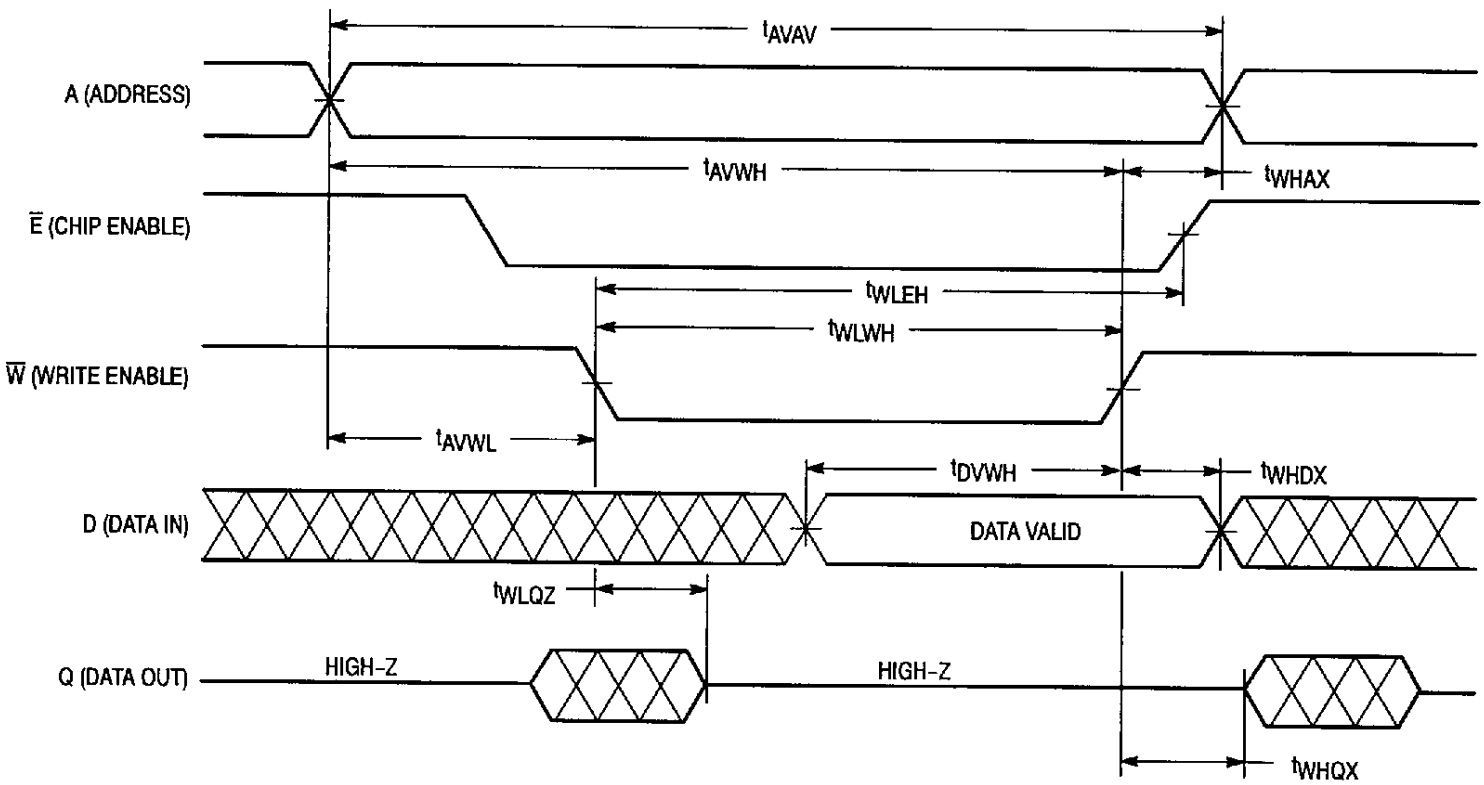


WRITE CYCLE 1 ($\overline{W}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6705A–10		MCM6705A–12		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	ns	4
Address Setup Time	t_{AVWL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVWH}	9	—	10	—	ns	
Write Pulse Width	t_{WLWH}, t_{WLEH}	9	—	10	—	ns	
Data Valid to End of Write	t_{DVWH}	5	—	6	—	ns	
Data Hold Time	t_{WHDX}	0	—	0	—	ns	
Write Low to Data High–Z	t_{WLQZ}	0	5	0	6	ns	5, 6, 7
Write High to Output Active	t_{WHQX}	3	—	3	—	ns	5, 6, 7
Write Recovery Time	t_{WHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ is represented by E in this table. E2 would require a transition opposite of $\overline{E1}$.
4. All write cycle timings are referenced from the last valid address to the first transitioning address.
5. Transition is measured 200 mV from steady–state voltage with load of Figure 1B.
6. Parameter is sampled and not 100% tested.
7. At any given voltage and temperature, t_{WLQZ} max is < t_{WHQX} min both for a given device and from device to device.

WRITE CYCLE 1

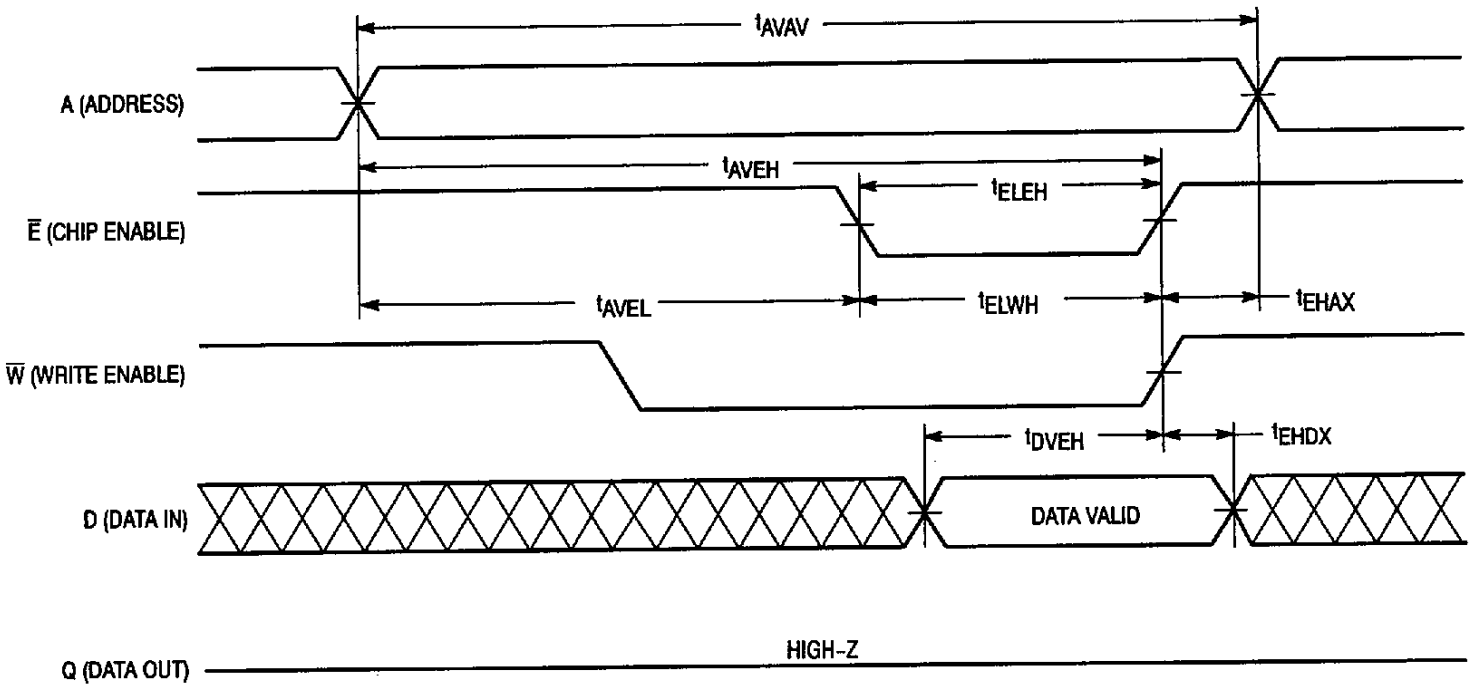


WRITE CYCLE 2 ($\overline{E}$ Controlled, See Notes 1, 2, and 3)

Parameter	Symbol	MCM6705A–10		MCM6705A–12		Unit	Notes
		Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	10	—	12	—	ns	4
Address Setup Time	t_{AVEL}	0	—	0	—	ns	
Address Valid to End of Write	t_{AVEH}	9	—	10	—	ns	
Chip Enable to End of Write	t_{ELWH}, t_{ELEH}	8	—	9	—	ns	5, 6
Data Valid to End of Write	t_{DVEH}	5	—	6	—	ns	
Data Hold Time	t_{EHDX}	0	—	0	—	ns	
Write Recovery Time	t_{EHAX}	0	—	0	—	ns	

NOTES:
1. A write occurs during the overlap of $\overline{E}$ low and $\overline{W}$ low.
2. Product sensitivites to noise require proper grounding and decoupling of power supplies as well as minimization or elimination of bus contention conditions during read and write cycles.
3. $\overline{E1}$ is represented by E in this table. E2 would require a transition opposite of $\overline{E1}$.
4. All write cycle timing is referenced from the last valid address to the first transitioning address.
5. If $\overline{E}$ goes low coincident with or after $\overline{W}$ goes low, the output will remain in a high impedance condition.
6. If $\overline{E}$ goes high coincident with or before $\overline{W}$ goes high, the output will remain in a high impedance condition.

WRITE CYCLE 2



ORDERING INFORMATION
(Order by Full Part Number)

MCM 6705A X XX XX

- Motorola Memory Prefix
- Part Number
- Package (J = 300 mil SOJ)
- Speed (10 = 10 ns, 12 = 12 ns)
- Shipping Method (R2 = Tape and Reel, Blank = Rails)

Full Part Numbers — MCM6705AJ10 MCM6705AJ10R2
MCM6705AJ12 MCM6705AJ12R2