Low Power Precision Analog Microcontroller ARM Cortex M3, with dual Sigma-Delta ADCs

Preliminary Technical Data

ADuCM360/ADuCM361

FEATURES

Analog Input/Output
- Dual (24-bit) ADCs (ADuCM360)
- Single (24-bit) ADC (ADuCM361)
- Single Ended and fully Differential inputs
- Programmable ADC output rate (4 Hz to 4 kHz)
- Simultaneous 50Hz/60Hz rejection
  - 50SPS Continuous Conversion Mode
  - 16.67SPS Single Conversion Mode

Flexible input MUX for input channel selection to both ADCs

Primary and Auxiliary (24-bit) ADC channel
- 6 differential or 11 Single-Ended input channels
- 4 internal channels for monitoring DAC, Temperature sensor, IOVDD and AVDD (ADC1 only)
- Programmable Gain (1 to 128)
- Selectable input range: ±6.64 mV to ±1.2 V
- RMS noise: 43nV @3.75Hz, 180nV @ 50Hz

Programmable sensor excitation current sources
- 10/50/100/150/200/250/300/400/500/600/800uA and 1mA current source options

On-chip precision Voltage reference (±4 ppm/°C)

Single 12-bit voltage output DAC
- NPN mode for 4-20mA loop applications

Microcontroller
- ARM Cortex™-M3 32-bit processor
- Serial Wire download and debug
- Internal Watch crystal for wakeup timer
- 16 MHz Oscillator with 8-way Programmable Divider

Memory

128k Bytes Flash/EE Memory, 8k Bytes SRAM

In-circuit debug/download via Serial Wire and UART

Power
- Operates directly from a 3.0V battery
- Supply Range: 1.8V to 3.6V (max)

Power Consumption
- MCU Active Mode: Core consumes 290µA / MHz
- Active Mode: 1.0mA (All peripherals active), core operating at 500KHz
- Power down mode: 4µA (WU Timer Active)

On-Chip Peripherals
- UART, I2C and 2 x SPI Serial I/O
- 16-bit PWM Controller
- 19-Pin Multi-Function GPIO Port
- 2 General Purpose Timers
- Wake-up Timer/Watchdog Timer
- Multi-Channel DMA and Interrupt Controller

Package and Temperature Range
- 48 lead LFCSP (7mm x 7mm) package –40°C to 125°C

Development Tools
- Low-Cost QuickStart™ Development System
- Third-Party Compiler and emulator tool Support

Multiple Functional Safety features for improved diagnostics

APPLICATIONS

- Industrial automation and process control
- Intelligent, precision sensing systems
- 4 mA to 20 mA loop-powered smart sensor systems
- Medical devices, patient monitoring

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FUNCTIONAL BLOCK DIAGRAM

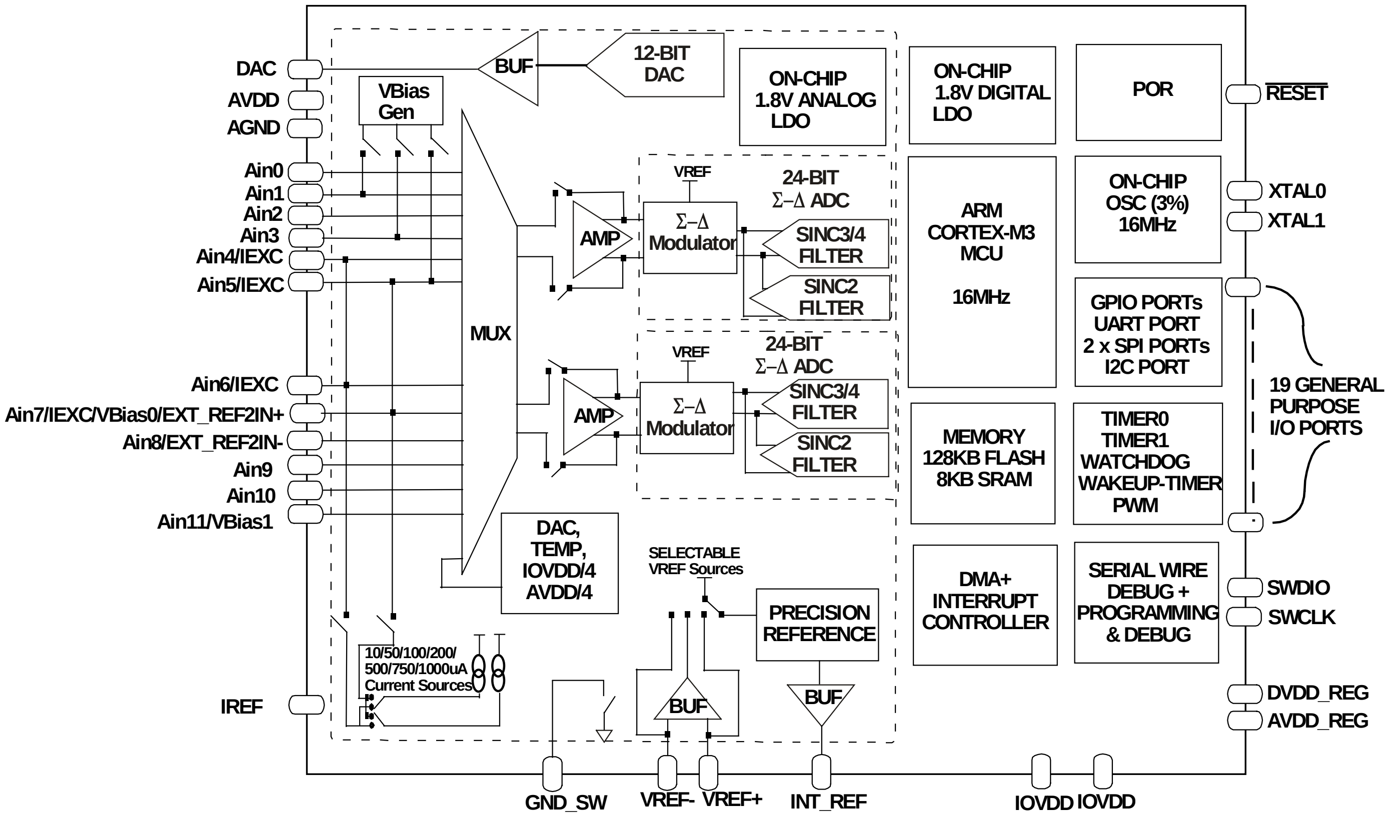

Figure 1. ADuCM360 Block Diagram

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GENERAL DESCRIPTION

The ADuCM360 is a fully integrated, 4 kSPS, 24-bit data acquisition system incorporating dual, high performance multichannel sigma-delta (Σ-Δ) analog-to-digital converters (ADCs), 32-bit ARM Cortex M3® MCU, and Flash/EE memory on a single chip. The part is designed for direct interfacing to external precision sensors in both wired and battery powered applications.

The ADuCM361 contains all the features of the ADuCM360 except the primary ADC, ADC0 is not available – only the auxiliary ADC, ADC1 is available.

The device contains an on-chip 32 KHz oscillator and an internal 16MHz high-frequency oscillator. This clock is routed through a programmable clock divider from which the MCU core clock operating frequency is generated. The maximum core clock speed is 16MHz and this is not limited by operating voltage or temperature.

The microcontroller core is a low power Cortex-M3 core from ARM. It is a 32-bit RISC machine, offering up to 20 MIPS peak performance. The Cortex-M3 MCU incorporates a flexible 11-channel DMA controller supporting all wired (SPI, UART, I^2C) communication peripherals. 128k Bytes of non-volatile Flash/EE and 8k Bytes of SRAM are also integrated on-chip.

The Analog sub-system consists of dual ADCs each connected to a flexible input MUX. Both ADCs can operate in fully differential and single ended modes. Other on-chip ADC features include dual programmable excitation current sources, burn-out current sources and a bias voltage generator of AVDD_REG/2 (900mV) to set the common-mode voltage of an input channel. A low-side internal ground switch is provided to allow powering down of a bridge between conversions. The ADCs contain two parallel filters – a Sinc3 or Sinc4 in parallel with a Sinc2. The Sinc3 or Sinc4 filter is for precision measurements. The Sinc2 filter is for fast measurements and for detection of step changes in the input signal The device also contains a low noise, low drift internal band-gap reference or can be configured to accept up to 2 external reference sources in ratiometric measurement configurations. An option to buffer the external reference inputs is also provided on-chip. A single-channel buffered voltage output DAC is also provided on chip.

The ADuCM360/ADuCM361 also integrates a range of on-chip peripherals which can be configured under microcontroller software control as required in the application. These peripherals include UART, I2C and dual SPI Serial I/O communication controllers, 19-Pin GPIO Ports, 2 General Purpose Timers, Wake-up Timer and System Watchdog Timer. A 16-bit PWM with six output channels is also provided.

The ADuCM360/ADuCM361 is specifically designed to operate in battery powered applications where low power operation is critical. The microcontroller core can be configured in a normal operating mode consuming 290µA/MHz (including Flash/SRAM Idd) resulting in an overall system current consumption of 1mA when all peripherals are active.

The part can also be configured in a number of low power operating modes under direct program control, including hibernate mode (internal wake-up timer active) consuming only 4µA. In hibernate mode, peripherals such as external interrupts or the internal wake up timer can wake up the device. This allows the part to operate in an ultra-low power operating mode and still respond to asynchronous external or periodic events.

On-chip factory firmware supports in-circuit serial download via a serial wire interface (2-pin JTAG system) and UART while non-intrusive emulation is also supported via the serial wire interface. These features are incorporated into a low-cost QuickStart Development System supporting this Precision Analog Microcontroller family.

The part operates from an external 1.8V to 3.6V voltage supply and is specified over an industrial temperature range of -40°C to 125°C.

SPECIFICATIONS

ADUCM360/ADUCM361 MICROCONTROLLER ELECTRICAL SPECIFICATIONS

AVDD/IOVDD = 1.8 V to 3.6V, Internal 1.2V reference, f_{CORE} = 16 MHz, all specifications T_A = −40°C to +125°C, unless otherwise noted.

Table 1. ADuCM360/ADuCM361 Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ADC SPECIFICATIONS					
Conversion Rate[1]	Chop off	4		4000	Hz
	Chop on	4		1333	Hz
Both Primary & Auxiliary Channels					
No Missing Codes[1]	Chop off (f_{ADC} ≤ 500 Hz)	24			Bits
	Chop on (f_{ADC} ≤ 250 Hz)	24			Bits
RMS Noise and Data Output Rates	See Noise and Resolution tables in the User Guide				
Integral Nonlinearity[1]	Gain = 1		±15		ppm of FSR
	Gain = 2, 4, 8, 16, 32, 64, 128		±25		ppm of FSR
Offset Error[,2,3]	Chop off, offset error is in the order of the noise for the programmed gain and update rate following calibration		±100/Gain		µV
Offset Error[1,2,3]	Chop on		±1.0		µV
Offset Error Drift vs. Temperature[4]	Chop off		100/ Gain		nV/°C
	Chop on		10		nV/°C
Offset Error Drift vs. Time			TBD		nV/1000 hours
Full-Scale Error[1,5,6,7]			±0.5/Gain	TBD	mV
Gain Drift vs. Temperature[4]	Gain = 1 to 16, external reference		±1		ppm/°C
	Gain = 32 to 128 external reference		±3		
Gain Error Drift vs. Time			TBD		ppm/1000 hours
PGA Gain Mismatch Error			±0.15		%
Power Supply Rejection[1,8]	Chop on, ADC = 0.25 V (Gain = 4), ext. reference	85			dB
	Chop off, ADC = 7.8 mV (Gain = 128), ext. reference	100			dB
	Chop off, ADC = 1 V (Gain = 1), ext. reference	85			dB
Absolute Input Voltage Range					
Unbuffered Mode	Gain=1	AGND		Avdd	V
Buffered Mode	Gain =1	AGND+ 100mV		Avdd-100mV	V
Unbuffered Mode:	Gain >=2	AGND		Avdd	mV
Differential Input Voltage Ranges[1]	Gain = 1			±VREF	mV
	Gain = 2			±500	mV
	Gain = 4			±250	mV
	Gain = 8			±125	mV
	Gain = 16			±62.5	mV
	Gain = 32 (AVDD >=2.0V)			±26.56	mV
	(AVDD <2.0V)			±18.75	mV
	Gain = 64 (AVDD >=2.0V)			±13.28	mV

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	(AVDD <2.0V)			±9.375	mV
	Gain = 128 (AVDD >=2.0V)			±6.64	mV
	(AVDD <2.0V)			±4.6875	mV
Common mode Voltage, Vcm[1]	Vcm=(AIN(+)+AIN(-))/2, Gain=2 to 128 Input current will be higher when Vcm <0.5V	AGND			V
Input Current[1,9]	Gain = 1, Buffered mode (excluding pins with Vbias)		1		nA
	Gain >1, Buffered mode (excluding pins with Vbias)		2-		nA
	Unbuffered mode. Input current will vary with input voltage		500		nA/V
Average Input Current Drift	Buffered mode:				
	AIN0, AIN1, AIN2, AIN3		±5		pA/°C
	AIN4, AIN5, AIN6, AIN7		±16		pA/°C
	AIN8, AIN9, AIN10, AIN11		±9		pA/°C
	Unbuffered mode		±250		pA/V/°C
Common-Mode Rejection DC[1]					
On ADC Input	ADC Gain =1	70	100		
	ADC Gain =2 to 128	80			dB
Common-Mode Rejection[1] 50 Hz/60 Hz	50 Hz/60 Hz ± 1 Hz, 16.7 Hz update rate, chop on 50 Hz update rate, chop off				
	ADC Gain =1	97			dB
	ADC Gain =2 to 128	90			dB
Normal-Mode Rejection[1] 50 Hz/60 Hz					
On ADC Input	50 Hz/60 Hz ± 1 Hz, 16.6 Hz $f_{ADC/}$ chop on, 50 Hz $f_{ADC/}$ chop off	60	80		dB
TEMPERATURE SENSOR	After user calibration				
Voltage Output at 25°C	MCU in power down or standby mode before measurement		82.1		mV
Voltage TC			250		mV/°C
Accuracy			6		°C
GROUND SWITCH					
Ron			12		Ohms
Allowable Current	With 20K resistor off – direct short to ground		20		mA
VOLTAGE REFERENCE					
ADC Precision Reference					
Internal V_{REF}			1.2		V
Initial Accuracy[1]	Measured at T_A = 25°C	-0.05		0.05	%
Reference Temperature Coefficient (Tempco)[1,8]		−15	±8	+15	ppm/°C
Power Supply Rejection[1]			100		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
External Reference Input Range	Buffered mode	0		AVDD-0.1	V
	Unbuffered mode	0		AVDD	V
	Minimum Differential voltage between VREF+ and VREF- pins is 400mV				
Input Current	Buffered mode		15		nA
	Unbuffered mode		500		nA/V
Normal Mode Rejection			80		
Common Mode Rejection			78		dB
Reference Detect Levels		-	400	-	mV
EXCITATION CURRENT SOURCES					
Output Current	Available from each current source – 10/50/200uA nominal	10	50	1000	µA
Initial Tolerance at 25°C	Iout >= 50uA		±5		%
Drift[1]	Using internal reference resistor		200		ppm/°C
	Using external 150 kΩ reference resistor between IREF pin and AGND. Resistor must have a drift spec of 5ppm/°C		75		ppm/°C
Initial Current Matching at 25°C[1]	Matching between both current sources		±0.5		%
Drift Matching[1]			50		ppm/°C
Load Regulation (AVDD) [1]	AVDD = 3.3 V		0.2		%/V
Output Compliance[1]	10uA to 210uA Iout	AGND – 30 mV		AVDD – 0.85 V	V
	Iout >210uA	AGND – 30 mV		AVDD – 1.1 V	V
DAC CHANNEL SPECIFICATIONS	R_L = 5 kΩ, C_L = 100 pF				
Voltage Range	Internal reference	0		V_{REF}	V
	External reference	0		1.8	V
DC Specifications[10]					
Resolution		12			Bits
Relative Accuracy			±3		LSB
Differential Nonlinearity	Guaranteed monotonic		±0.5	±1	LSB
Offset Error	1.2 V internal reference		±2	±15	mV
Gain Error	V_{REF} range (reference = 1.2 V)			±1	%
NPN Mode					
Resolution		12			Bits
Relative Accuracy			±1.0		LSB
Differential Nonlinearity			±0.5		LSB
Offset Error			±0.35		mA
Gain Error			±0.75		mA
Output Current Range[1]		0.008		23.6	mA
DAC AC CHARACTERISTICS					
Voltage Output Settling Time			10		µs
Digital-to-Analog Glitch Energy	1 LSB change at major carry (where maximum number of bits simultaneously change in the DAC0DAT register)		±20		nV-sec

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER-ON RESET (POR)					
POR Trip Level	Refers to voltage at DVDD pin				
	Power-on level		1.6		V
	Power-down level		1.6		V
Timeout from POR			50		ms
WATCHDOG TIMER (WDT)					
Timeout Period[1]		0.00003		8192	sec
Timeout Step Size	T3CON[3:2]=[10]		7.8125		ms
FLASH/EE MEMORY[1]					
Endurance[11]		20,000			Cycles
Data Retention[12]	Tj=85°C	10			Years
Digital Inputs	All digital inputs				
Logic 1 Input Current (leakage current)	V_{INH} =VDD or V_{INH} = 1.8V		10		nA
	Internal pull-up disabled $\overline{\text{RESET}}$, SWCLK, SWDIO		100		µA
Logic 0 Input Current (leakage current)	V_{INL} = 0V		10		nA
	Internal pull-up disabled $\overline{\text{RESET}}$, SWCLK, SWDIO		100		µA
Input Capacitance			10		pF
Logic Inputs					
VINL, Input Low Voltage				0.2 x VDD	V
VINH, Input High Voltage		0.7 x VDD			V
Logic Outputs					
VOH, Output High Voltage	I_{SOURCE} = 1mA	VDD – 400mV			V
VOL, Output Low Voltage	I_{SINK} = 1mA			0.4	V
CRYSTAL OSCILLATOR[1]					
Logic Inputs, XTALI Only[13]					
Input Low Voltage (VINL)				0.8	V
Input High Voltage (VINH)		1.7			V
XTALI Capacitance			6		pF
XTALO Capacitance			6		pF
ON-CHIP Low Power Oscillator					
Oscillator			32,768		kHz
Accuracy		–20		+20	%
ON-CHIP High Frequency Oscillator					
Oscillator		0.125	2	16	MHz
Accuracy	To be confirmed across full temperature range of -40 to +125C	-1		1	%
MCU CLOCK RATE	Eight programmable core clock selections within this range:	0.125	2	16	MHz
Using an External Clock		0.032768		16	MHz
MCU START-UP TIME					
At Power-On	Includes kernel power-on execution time		41		ms
After Reset Event	Includes kernel power-on execution time		1.44		ms

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
From MCU Power-Down (mode 1, 2 and 3)	Fclk is the Cortex-M3 core clock		3-5 x Fclk		
From TOTAL-HALT or HIBERNATE (mode 4 or mode 5) mode			30.8		μs
POWER REQUIREMENTS					
Power Supply Voltages					
VDD		1.8		3.6	V
Power Consumption					
I_{DD} (MCU Active Mode)[14,15]	MCU clock rate = 16 MHz, all peripherals on		5.5		mA
	MCU clock rate = 500 KHz, Both ADCs on (Input buffers off) with PGAs Gain = 4, 1 x SPI on, all timers on		1		mA
I_{DD} (MCU Powered Down)[1]	Full temperature range HIBERNATE (mode 5)		4	10	μA
	Reduced temperature range −40°C to +85°C		2	5	μA
I_{DD} (Primary ADC) (total)[15]	PGA enabled – total, G>=32		320		μA
PGA	G=4/8/16 – PGA only		130		μA
	G=32/64/128 – PGA only		180		
Input Buffers	2 x Input buffers is 70uA		70		μA
Digital Interface + Modulator			70		μA
I_{DD} (Auxiliary ADC)	Input buffers off, G=4/8/16 only		200		μA
External Reference Input buffers	60uA each		120		μA

[1] These numbers are not production tested but are guaranteed by design and/or characterization data at production release.
[2] Tested at gain range = 4 after initial offset calibration.
[3] Measured with an internal short. A system zero-scale calibration removes this error.
[4] A recalibration at any temperature removes these errors.
[5] These numbers do not include internal reference temperature drift.
[6] Factory calibrated at gain = 1.
[7] System calibration at a specific gain range removes the error at this gain range.
[8] Measured using the box method.
[9] Input current measured with one ADC measuring a channel. If both ADCs measure the same input channel, then the input current will increase – approximately double
[10] Reference DAC linearity is calculated using a reduced code range of 0x0AB to 0xF30.
[11] Endurance is qualified to 20,000 cycles as per JEDEC Std. 22 Method A117 and measured at −40°C, +25°C, and +125°C. Typical endurance at 25°C is 170,000 cycles.
[12] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Std. 22 Method A117. Retention lifetime derates with junction temperature.
[13] Voltage input levels only relevant if driving XTAL input from a voltage source. If a crystal is connected directly, the internal crystal interface will determine the common mode voltage.
[14] Typical additional supply current consumed during Flash/EE memory program and erase cycles is 7mA.
[15] Total I_{DD} for ADC includes figures for PGA≥32, input buffers, digital interface and the Sigma Delta modulator.

NOISE RESOLUTION OF PRIMARY AND AUXILIARY ADCS

Table 2: RMS Noise (μV) vs. Gain and Output Update Rate

(Using an Internal Reference (1.2V) Both ADCs)

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
3.75 (Chop On) ADCxFLT = 0x8D7C	1.05	0.45	0.23	0.135	0.072	0.064	0.055	0.052
30 (Chop Off) ADCxFLT = 0x007E	2.1	1.37	0.63	0.37	0.22	0.2	0.16	0.155
50 (Chop Off) ADCxFLT = 0x007D	3.7	1.6	0.83	0.47	0.29	0.24	0.21	0.2
100 (Chop Off) ADCxFLT = 0x004D	5.45	2.41	1.13	0.63	0.38	0.32	0.27	0.25
488 (Chop Off Sinc4) ADCxFLT = 0x100F	10	4.7	2.2	1.3	0.79	0.67	0.58	0.57
976 (Chop Off Sinc4) ADCxFLT = 0x1007	13.5	6.5	3.3	1.7	1.1	0.91	0.74	0.7
1953 (Chop Off Sinc4) ADCxFLT = 0x1003	19.3	10	4.7	2.6	1.55	1.3	1.15	1.0
3906 (Chop Off Sinc4) ADCxFLT = 0x1001	67.0	36	16.6	8.8	4.9	2.68	1.76	1.4

Table 3: Typical Output RMS Effective Number of Bits in Normal Mode

(Using an Internal Reference (1.2V), Both ADCs, Peak-to-Peak Bits in Parentheses)

ADC Register Status	Data Update Rate	Input Voltage Noise (mV)							
		±1.0 V (PGA = 1)	**±500 mV (PGA = 2)**	**±250 mV (PGA = 4)**	**±125 mV (PGA = 8)**	**±62.5 mV (PGA = 16)**	**±31.25 mV (PGA = 32)**	**±15.625 mV (PGA = 64)**	**±7.8125 mV (PGA = 128)**
Chop On Sinc3	3.75 Hz	21.1 (18.4p-p)	21.3 (18.6p-p)	21.3 (18.6p-p)	21.1 (18.4p-p)	21 (18.3p-p)	20.2 (17.4p-p)	19.4 (16.7p-p)	18.5 (15.7p-p)
Chop Off Sinc3	30 Hz	20.1 (17.4p-p)	19.7 (17p-p)	19.8 (17.1p-p)	19.6 (16.9p-p)	19.4 (16.7p-p)	18.5 (15.8p-p)	17.8 (15.1p-p)	16.9 (14.2p-p)
Chop Off Sinc3	50 Hz	19.3 (16.6p-p)	19.5 (16.8p-p)	19.5 (16.8p-p)	19.3 (16.6p-p)	19 (16.3p-p)	18.3 (15.5p-p)	17.4 (14.7p-p)	16.5 (13.8p-p)
Chop Off Sinc3	100 Hz	18.7 (16p-p)	18.9 (16.2p-p)	19 (16.3p-p)	18.9 (16.2p-p)	18.6 (16.1p-p)	17.8 (15.1p-p)	17.1 (14.4p-p)	16.2 (13.5p-p)
Chop Off Sinc4	488 Hz	17.9 (15.2p-p)	18 (15.2p-p)	18.1 (15.3p-p)	17.8 (15.1p-p)	17.5 (14.8p-p)	16.8 (14p-p)	16 (13.3p-p)	15 (12.3p-p)
Chop Off Sinc4	976 Hz	17.4 (14.7p-p)	17.5 (14.8p-p)	17.5 (14.8p-p)	17.4 (14.7p-p)	17.1 (14.3p-p)	16.3 (13.6p-p)	15.6 (12.9p-p)	14.7 (12p-p)
Chop Off Sinc4	1953 Hz	16.9 (14.2p-p)	16.9 (14.2p-p)	17 (14.3p-p)	16.8 (14p-p)	16.6 (13.8p-p)	15.8 (13.1p-p)	15 (13.1p-p)	14.2 (11.5p-p)
Chop Off Sinc4	3906 Hz	15.1 (12.4p-p)	15 (12.3p-p)	15.1 (12.4p-p)	15.1 (12.4p-p)	14.9 (12.2p-p)	14.8 (12p-p)	14.4 (11.7p-p)	13.7 (11p-p)

Table 4: RMS Noise (µV) vs. Gain and Output Update Rate

(Using an External Reference (2.5V) Both ADCs)

Update Rate (Hz)	Gain of 1	Gain of 2	Gain of 4	Gain of 8	Gain of 16	Gain of 32	Gain of 64	Gain of 128
4.55 (Chop On) ADCxFLT = 0x88FD	1.1	0.5	0.27	0.17	0.088	0.07	0.06	0.58
30 (Chop Off) ADCxFLT = 0x007E	3	1.4	0.85	0.44	0.27	0.22	0.19	0.17
50 (Chop Off) ADCxFLT = 0x007D	3.9	2.2	0.92	0.46	0.3	0.21	0.2	0.19
100 (Chop Off) ADCxFLT = 0x004F	5.2	2.8	1.25	0.63	0.38	0.32	0.28	0.26
488 (Chop Off Sinc4) ADCxFLT = 0x100F	9.3	5.0	2.5	1.2	0.75	0.7	0.57	0.5
976 (Chop Off Sinc4) ADCxFLT = 0x1007	12.5	7	3.5	1.75	1.2	0.83	0.77	0.75
1953 (Chop Off Sinc4) ADCxFLT = 0x1003	20.0	10	5.7	2.6	1.71	1.3	1.24	1.1
3906 (Chop Off Sinc4) ADCxFLT = 0x1001	140.0	70.0	35.0	17.2	8.9	4.8	2.65	1.88

Table 5: Typical Output RMS Effective Number of Bits in Normal Mode

(Using an External Reference (2.5V), Both ADCs, Peak-to-Peak Bits in Parentheses)

ADC Register Status	Data Update Rate		Input Voltage Noise (mV)						
		±1.0 V (PGA = 1)	**±500 mV (PGA = 2)**	**±250 mV (PGA = 4)**	**±125 mV (PGA = 8)**	**±62.5 mV (PGA = 16)**	**±31.25 mV (PGA = 32)**	**±15.625 mV (PGA = 64)**	**±7.8125 mV (PGA = 128)**
Chop On Sinc3	3.75 Hz	22.1 (19.4p-p)	22.3 (19.5p-p)	22.1 (19.4p-p)	21.8 (19.1p-p)	21.8 (19.1p-p)	21.1 (18.4p-p)	20.3 (17.6p-p)	19.4 (16.6p-p)
Chop Off Sinc3	30 Hz	20.7 (18p-p)	20.7 (18p-p)	20.5 (17.7p-p)	20.5 (17.7p-p)	20.1 (17.4p-p)	19.4 (16.7p-p)	18.6 (15.9p-p)	17.8 (15.1p-p)
Chop Off Sinc3	50 Hz	20.3 (17.6p-p)	20.1 (17.4p-p)	20.4 (17.7p-p)	20.4 (17.7p-p)	20 (17.3p-p)	19.5 (16.8p-p)	18.6 (15.9p-p)	17.6 (14.9p-p)
Chop Off Sinc3	100 Hz	19.9 (17.2p-p)	19.8 (17p-p)	19.9 (17.2p-p)	19.9 (17.2p-p)	19.6 (16.9p-p)	18.9 (16.2p-p)	18.1 (15.4p-p)	17.2 (14.5p-p)
Chop Off Sinc4	488 Hz	19 (16.3p-p)	18.9 (16.2p-p)	18.9 (16.2p-p)	19 (16.3p-p)	18.7 (15.9p-p)	17.8 (15p-p)	17.1 (14.3p-p)	16.3 (13.5p-p)
Chop Off Sinc4	976 Hz	18.6 (15.9p-p)	18.4 (15.7p-p)	18.4 (15.7p-p)	18.4 (15.7p-p)	18 (15.3p-p)	17.5 (14.8p-p)	16.6 (13.9p-p)	15.7 (12.9p-p)
Chop Off Sinc4	1953 Hz	17.9 (15.2p-p)	17.9 (15.2p-p)	17.7 (15p-p)	17.9 (15.2p-p)	17.5 (14.8p-p)	16.9 (14.2p-p)	15.9 (13.2p-p)	15.1 (12.4p-p)
Chop Off Sinc4	3906 Hz	15.1 (12.4p-p)	15.1 (12.4p-p)	15.1 (12.4p-p)	15.1 (12.4p-p)	15.1 (12.4p-p)	15 (12.3p-p)	14.8 (12.1p-p)	14.3 (11.6p-p)

I²C TIMING DIAGRAMS

Capacitive load for each of the I²C[1]-bus line, Cb = 400pF maximum as per I²C-bus specifications.

I²C timing is guaranteed by design and not production tested.

Table 6. I²C Timing in Fast Mode (400 kHz)

Parameter	Description	Min	Max	Unit
t_L	Serial Clock (SCL) low pulse width	1300	-	ns
t_H	SCL high pulse width	600	-	ns
t_{SHD}	Start condition hold time	600	-	ns
t_{DSU}	Data setup time	100	-	ns
t_{DHD}	Data hold time	0	-	ns
t_{RSU}	Setup time for repeated start	600	-	ns
t_{PSU}	Stop condition setup time	600	-	ns
t_{BUF}	Bus-free time between a stop condition and a start condition	1.3	-	µs
t_R	Rise time for both SCL and serial data (SDA)	20 + 0.1 Cb	300	ns
t_F	Fall time for both SCL and SDA	20 + 0.1 Cb	300	ns
t_{SUP}	Pulse width of spike suppressed	0	50	ns

Table 7. I²C Timing in Standard Mode (100 kHz)

Parameter	Description	Min	Max	Unit
t_L	SCL low pulse width	4.7	-	µs
t_H	SCL high pulse width	4.0	-	ns
t_{SHD}	Start condition hold time	4.7	-	µs
t_{DSU}	Data setup time	250	-	ns
t_{DHD}	Data hold time	0	-	µs
t_{RSU}	Setup time for repeated start	4.0	-	µs
t_{PSU}	Stop condition setup time	4.0	-	µs
t_{BUF}	Bus-free time between a stop condition and a start condition	4.7	-	µs
t_R	Rise time for both SCL and SDA	-	1	µs
t_F	Fall time for both SCL and SDA	-	300	ns

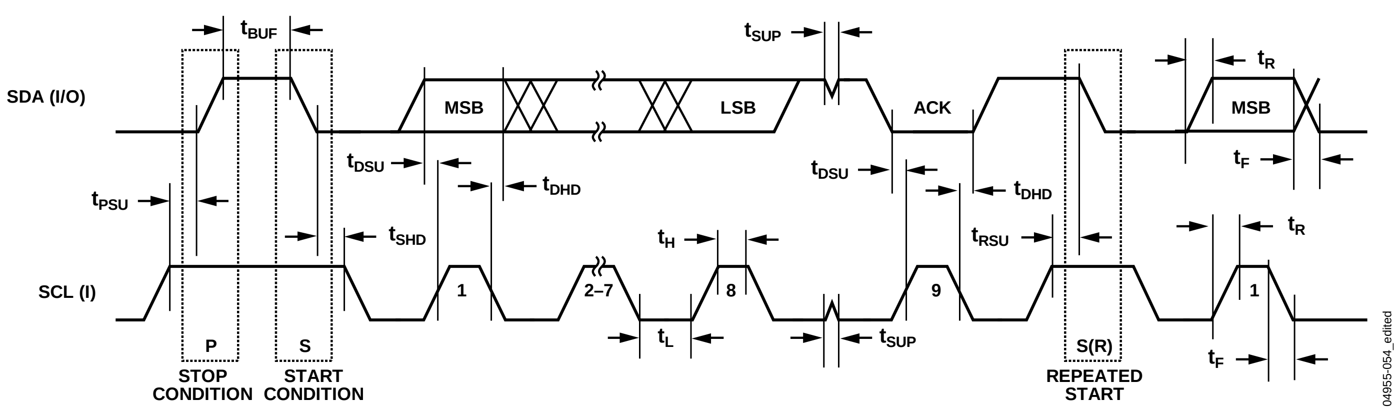


Figure 2. I²C Compatible Interface Timing

[1] I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

SPI TIMING DIAGRAMS

Table 8. SPI Master Mode Timing

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge		0	35.5	ns
t_{DOSU}	Data output setup before SCLK edge[1]	(SPIDIV + 1) × t_{UCLK}			ns
t_{DSU}	Data input setup time before SCLK edge	58.7			ns
t_{DHD}	Data input hold time after SCLK edge	16			ns
t_{DF}	Data output fall time		12	35.5	ns
t_{DR}	Data output rise time		12	35.5	ns
t_{SR}	SCLK rise time		12	35.5	ns
t_{SF}	SCLK fall time		12	35.5	ns

[1] t_{UCLK} = 62.5 ns. It corresponds to the internal 16MHz clock before the clock divider.

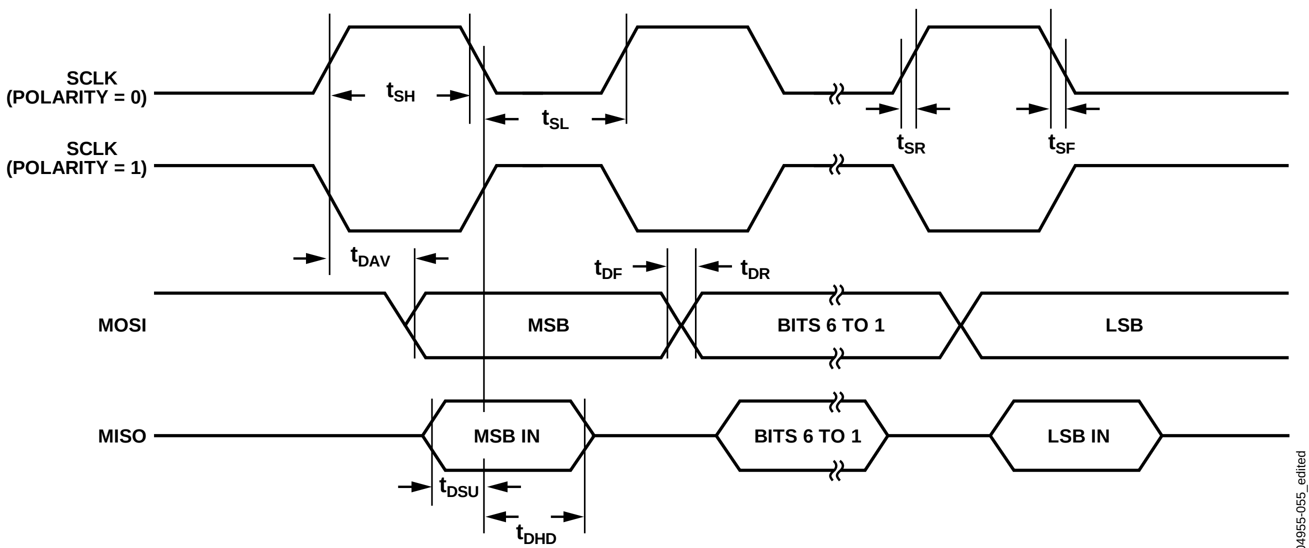


Figure 3. SPI Master Mode Timing (PHASE Mode = 1)

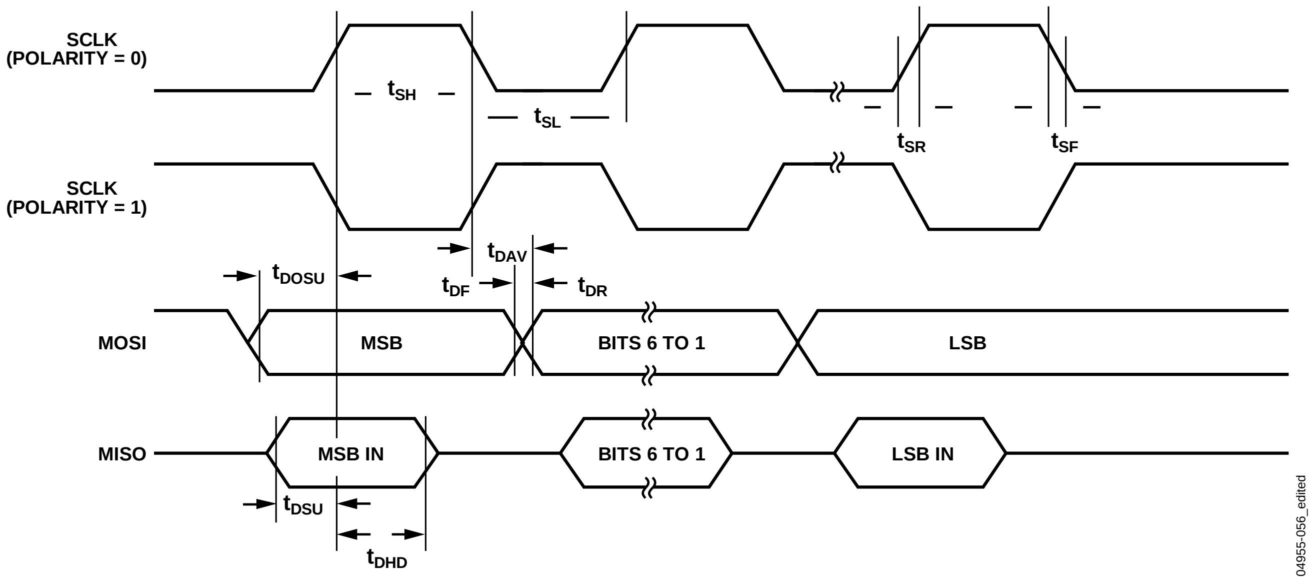


Figure 4. SPI Master Mode Timing (PHASE Mode = 0)

Table 9. SPI Slave Mode Timing

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge	38			ns
t_{SL}	SCLK low pulse width[1]		(SPIDIV + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]	62.5	(SPIDIV + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge			49.1	ns
t_{DSU}	Data input setup time before SCLK edge	20.2			ns
t_{DHD}	Data input hold time after SCLK edge	10.1			ns
t_{DF}	Data output fall time		12	35.5	ns
t_{DR}	Data output rise time		12	35.5	ns
t_{SR}	SCLK rise time		12	35.5	ns
t_{SF}	SCLK fall time		12	35.5	ns
t_{DOCS}	Data output valid after $\overline{CS}$ edge			25	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 62.5 ns. It corresponds to the internal 16MHz clock before the clock divider.

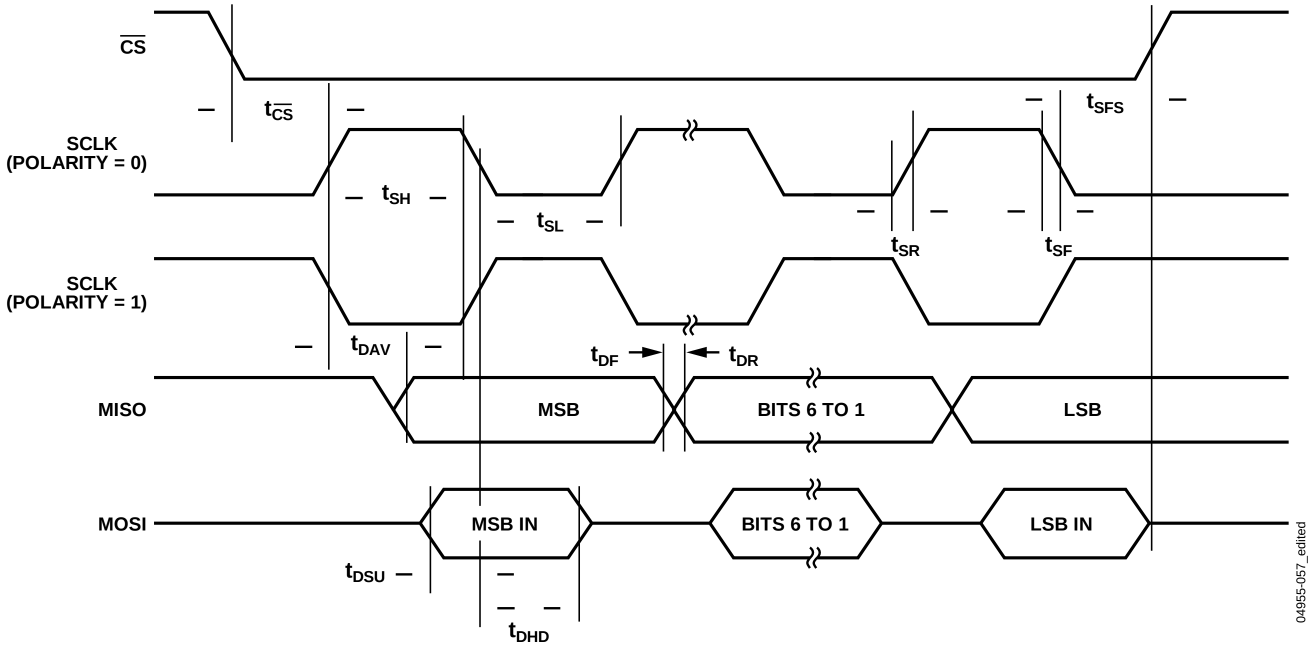


Figure 5. SPI Slave Mode Timing (PHASE Mode = 1)

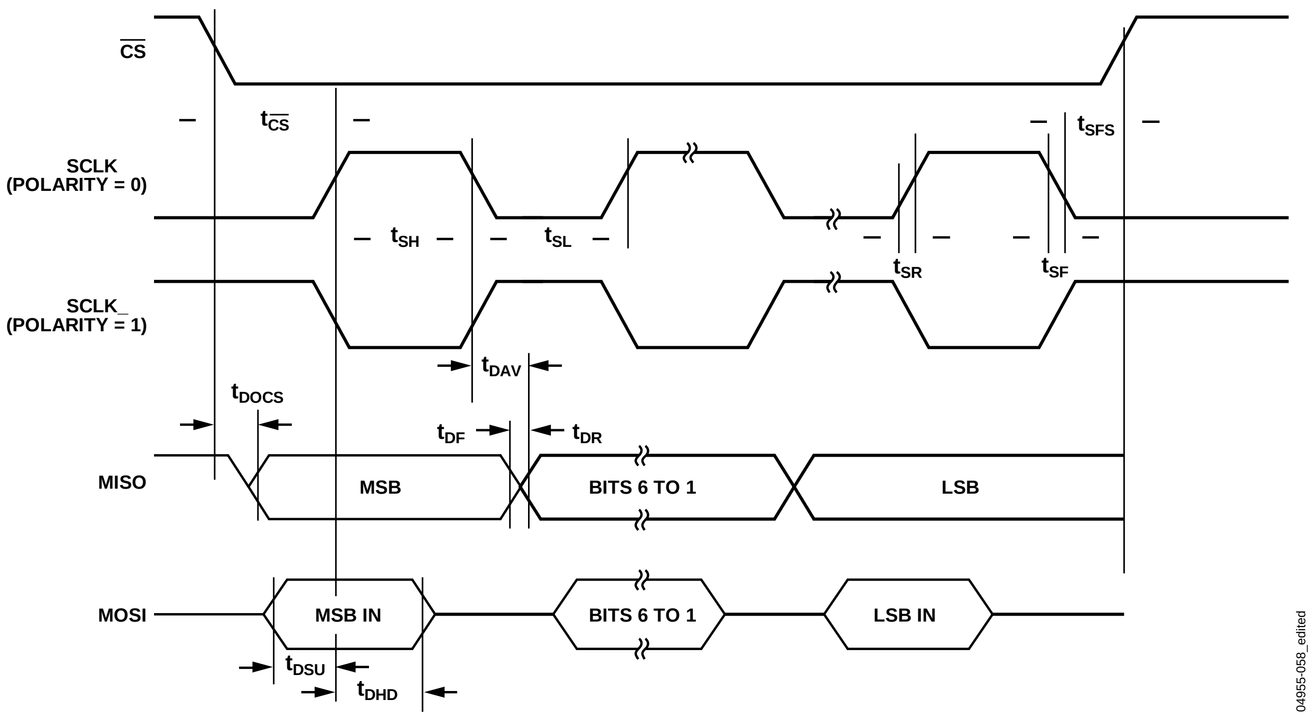


Figure 6. SPI Slave Mode Timing (PHASE Mode = 0)

ABSOLUTE MAXIMUM RATINGS

Table 10.

Parameter	Rating
AVDD/IOVDD to GND	−0.3 V to 3.96V
Digital Input Voltage to DGND	−0.3 V to 3.96V
Digital Output Voltage to DGND	−0.3 V to 3.96V
V_{REF} to AGND	−0.3 V to TBD
Analog Inputs to AGND	−0.3 V to TBD
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD (Human Body Model) rating	±2kV
All Pins	
θ_{JA} Thermal Impedance	
48-Pin LFCSP _VQ	27°C/W
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
Pb-Free Assemblies (20 sec to 40 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Pin Configuration and Function Descriptions

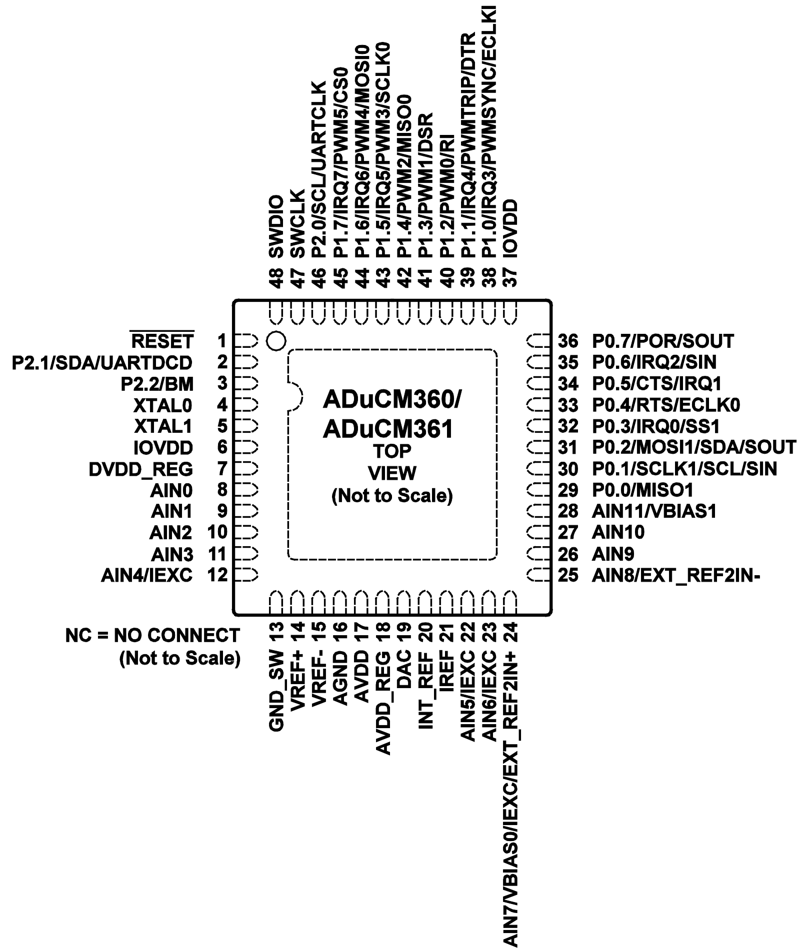


Figure 7. ADuCM360/ADuCM361 Pinout

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Reset. Input pin, active low. An internal pull-up is provided.
2	P2.1/SDA/UARTDCD	General-Purpose Input and General-Purpose Output P2.1/ I^{2}C serial data Pin/Alternatively, this pin may be the UART Data carrier Detect pin. This is a multi function input/output pin.
3	P2.2/BM	General-Purpose Input and General Purpose Output P2.2/ Boot mode input select pin. When this pin is held low during any reset sequence, the part will enter UART download mode. This is a dual function input/output pin.
4	XTAL0	External Crystal Oscillator Output Pin. Optional 32.768kHz source for Real time clock.
5	XTAL1	External Crystal Oscillator Input Pin. Optional 32.768kHz source for Real time clock.
6	IOVDD	Digital System Supply pin.
7	DVDD_REG	Internal Digital Regulator Supply Output. This pin must be connected to ground via a 470nF capacitor. ***Note: This pin must be connected to pin 18, AVDD_REG***
8	AIN0	ADC Analog Input 0. This pin can be configured as a positive or negative input to either ADC in Differential or single ended modes.
9	AIN1	ADC Analog Input 1. This pin can be configured as a positive or negative input to either ADC in Differential or single ended modes.
10	AIN2	ADC Analog Input 2. This pin can be configured as a positive or negative input to either ADC in

Pin No.	Mnemonic	Description
		Differential or single ended modes.
11	AIN3	ADC Analog Input 3. This pin can be configured as a positive or negative input to either ADC in Differential or single ended modes.
12	AIN4/IEXC	ADC Analog Input 4. This pin can be configured as a positive or negative input to either ADC in Differential or single ended modes. Or, it may be configured as the output pin for either Excitation current source 0 or 1.
13	GND_SW	Sensor Power Switch to Analog Ground Reference.
14	VREF+	External Reference Positive Input, an external reference can be applied between VREF+ and VREF-.
15	VREF−	External Reference Negative Input, an external reference can be applied between VREF+ and VREF-.
16	AGND	Analog System Ground reference pin.
17	AVDD	Analog System Supply pin.
18	AVDD_REG	Internal Analog Regulator Supply Output. This pin must be connected to ground via a 470nF capacitor. ***Note: This pin must be connected to pin 7, DVDD_REG***
19	DAC	DAC Voltage Output
20	INT_REF	This pin must be connected to ground via a 470nF decoupling capacitor.
21	IREF	Optional reference current resistor connection for the Excitation current sources. Reference current set by low drift external resistor (5ppm/C).
22	AIN5/IEXC	Multi-Function Pin: ADC Analog Input 5. This pin can be configured as a positive or negative input to either ADC in Differential or single ended modes. Alternatively, it may be configured as the output pin for either Excitation current source 0 or 1. Or, it may be configured as the output pin for either Excitation current source 0 or 1.
23	AIN6/IEXC	Multi-Function Pin: ADC Analog Input 6. This pin can be configured as a positive or negative input to either ADC in Differential or single ended modes. Or, it may be configured as the output pin for either Excitation current source 0 or 1.
24	AIN7/VBIAS0/IEXC/EXT_REF2IN+	Multi-Function Pin: ADC Analog Input 7. This pin can be configured as a positive or negative input to either ADC in differential or single ended modes. Alternatively, this pin can be configured as an analog output pin to generate a Bias Voltage, VBIAS3 of AVDD_REG/2. Or, it may be configured as the output pin for either Excitation current source 0 or 1. Alternatively, this pin can be configured as an external reference 2 positive input.
25	AIN8/EXT_REF2IN-	Multi-Function Pin: ADC Analog Input 8. This pin can be configured as a positive or negative input to either ADC in Differential or single ended modes. Alternatively, this pin can be configured as an external reference 2 negative input.
26	AIN9	ADC Analog Input 9. This pin can be configured as a positive or negative input to either ADC in Differential or single ended modes. Alternatively, this pin can be configured as the non-inverting input to the DAC output buffer when the DAC is configured for NPN mode.
27	AIN10	ADC Analog Input 10. This pin can be configured as a positive or negative input to either ADC in Differential or single ended modes.
28	AIN11/VBIAS1	Multi-Function Pin: ADC Analog Input 11. This pin can be configured as a positive or negative input to either ADC in Differential or single ended modes. Alternatively, this pin can be configured as an analog output pin to generate a Bias Voltage, VBIAS5 of AVdd/2.
29	P0.0/MISO1	General-Purpose Input and General-Purpose Output P0.0/SPI1 Master In – Slave out Pin. This is a dual function input/output pin.
30	P0.1/SCLK1/SCL/SIN	General-Purpose Input and General-Purpose Output P0.1/SPI1 Serial Clock Pin/I^{2}C Serial Clock Pin/ UART Serial Input. This is a multi function input/output pin. ***This pin will be the data input for the UART downloader.***
31	P0.2/MOSI1/SDA/SOUT	General-Purpose Input and General-Purpose Output P0.2/ SPI1 Master Out – Slave In Pin /I^{2}C Serial Data Pin/ UART Serial output. This is a multi function input/output pin. ***This pin will be the data output for the UART downloader.***
32	P0.3/IRQ0/$\overline{\text{CS1}}$	General-Purpose Input and General-Purpose Output P0.3/ External Interrupt Request 0/ SPI1 Chip Select Pin (Active Low). This is a triple function input/output pin.
33	P0.4/RTS/ECLKO	General-Purpose Input and General-Purpose Output P0.4/ Request-to-Send Signal in UART Mode/ Clock out (for test purposes) pin. This is a triple function input/output pin.
34	P0.5/CTS/IRQ1	General-Purpose Input and General-Purpose Output P0.5/ Clear-to-Send Signal in UART Mode. / External Interrupt Request 1.

Pin No.	Mnemonic	Description
		This is a dual function input/output pin.
35	P0.6/IRQ2/SIN	General-Purpose Input and General-Purpose Output P0.6/ External Interrupt Request 2/ UART Serial Input. This is a triple function input/output pin.
36	P0.7/POR/SOUT	General-Purpose Input and General-Purpose Output P0.7/ Power on Reset active high bit/ UART Serial output. This is a triple function input/output pin.
37	IOVDD	Digital System Supply pin.
38	P1.0/IRQ3/PWMSYNC/ECLKI	General-Purpose Input and General Purpose Output P1.0/ External Interrupt Request 3/ PWM external Sync input/External clock input pin. This is a Quad function input/output pin.
39	P1.1/IRQ4/PWMTRIP/DTR	General-Purpose Input and General Purpose Output P1.1/ External Interrupt Request 4/ PWM external trip input/UART Data terminal Ready pin. This is a multi function input/output pin.
40	P1.2/PWM0/RI	General-Purpose Input and General-Purpose Output P1.2/PWM0 Output/UART Ring Indicator pin. This is a triple function input/output pin.
41	P1.3/PWM1/DSR	General-Purpose Input and General-Purpose Output P1.3/PWM1 Output/UARTData Set Ready pin. This is a triple function input/output pin.
42	P1.4/PWM2/MISO0	General-Purpose Input and General-Purpose Output P1.4/PWM2 Output/ SPI0 Master In – Slave out Pin. This is a triple function input/output pin.
43	P1.5/IRQ5/PWM3/SCLK0	General-Purpose Input and General-Purpose Output P1.5/ External Interrupt Request 5/ PWM3 Output/ SPI0 Serial Clock Pin. This is a Quad function input/output pin.
44	P1.6/IRQ6/PWM4/MOSI0	General-Purpose Input and General-Purpose Output P1.6/ External Interrupt Request 6/ PWM4 Output/ SPI0 Master out, Slave in Pin. This is a Quad function input/output pin.
45	P1.7/IRQ7/PWM5/$\overline{\text{CS0}}$	General-Purpose Input and General-Purpose Output P1.7/ External Interrupt Request 7/ PWM5 Output/ SPI0 Chip Select Pin (Active Low). This is a Quad function input/output pin.
46	P2.0/SCL/UARTCLK	General-Purpose Input and General Purpose Output P2.0/ I^2C Serial Clock Pin. Alternatively, this pin may be an optional input clock pin for the UART block only. This is a Triple function input/output pin.
47	SWCLK	Serial Wire debug clock input pin.
48	SWDIO	Serial Wire debug data input/output pin.
	EP	**Exposed Paddle. The LFCSP_VQ has an exposed paddle that MUST BE connected to digital ground.

TYPICAL PERFORMANCE CHARACTERISTICS

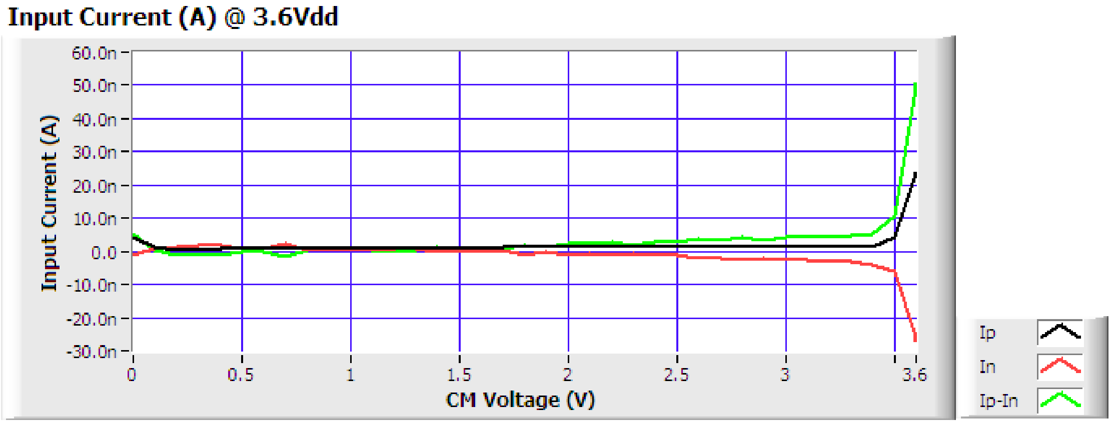


Figure 8. Common Mode Voltage (Vcm) in Volts vs Input Current in nA, Gain=4, ADC input 250mV, AVdd=3.6V, T=25C

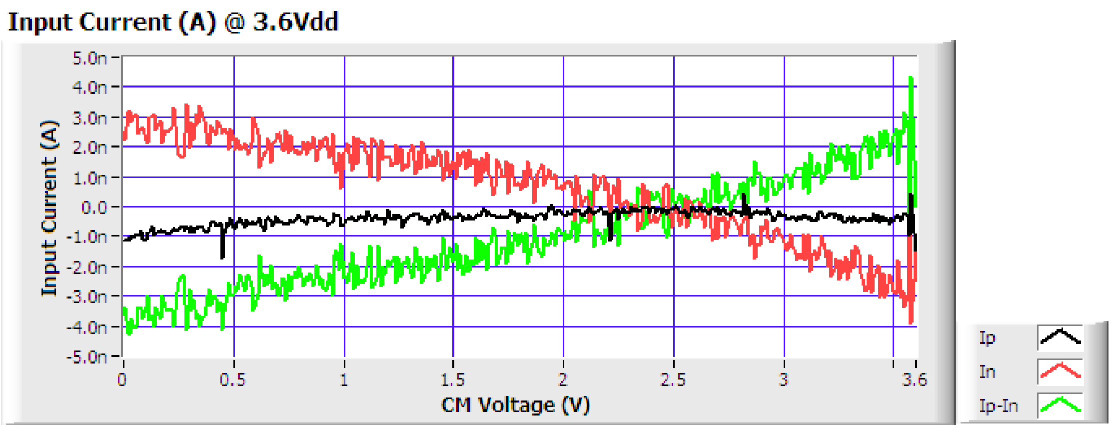


Figure 9. Common Mode Voltage (Vcm) in Volts vs Input Current in nA, Gain=128, ADC input 7.8125mV, AVdd=3.6V, T=25C

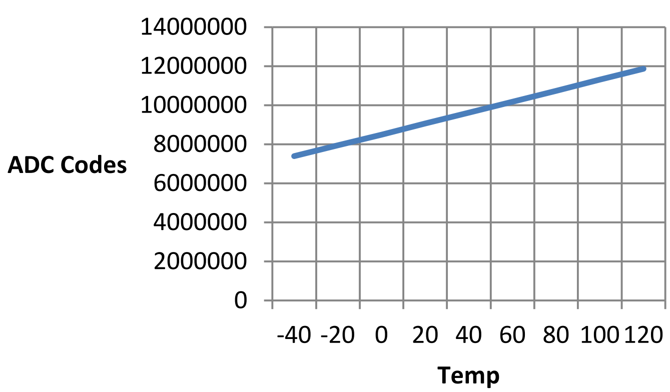
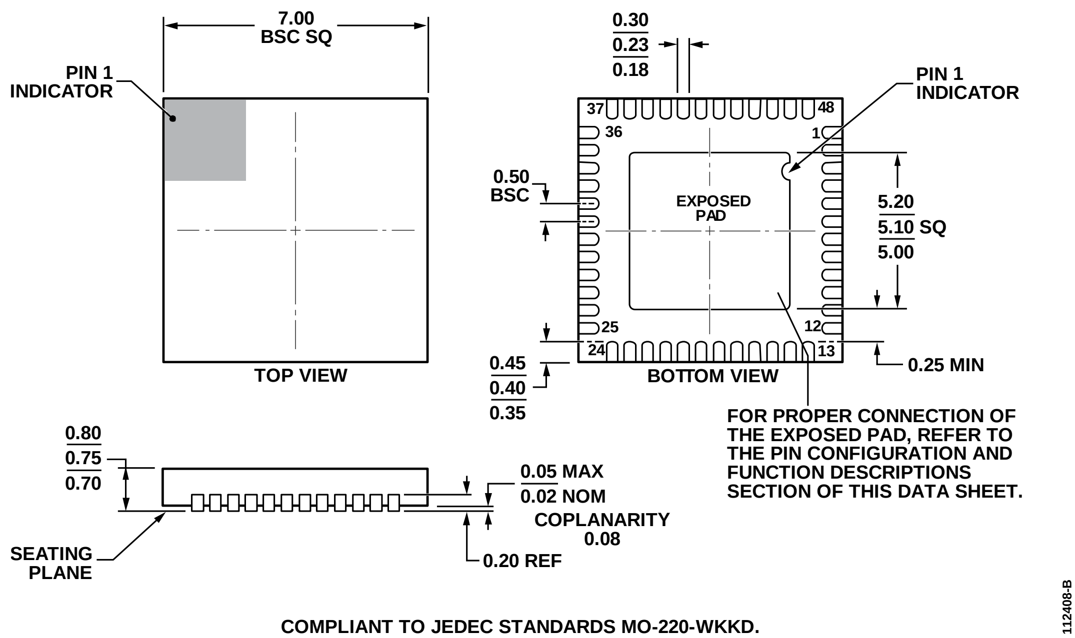


Figure 10. ADC Codes (decimal values) v Die temperature

OUTLINE DIMENSIONS



(CP-48-4)

Figure 11. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad
Dimensions shown in millimeters