Integrated Device Technology, Inc.

16K x 16 CMOS STATIC RAM MODULE

IDT7MC4005

FEATURES:

- High-density 256K CMOS static RAM module
- Fast access time: 15ns (max.)
- Low profile 36-pin sidebraze ceramic DSIP (Dual Single In-line Package)
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible
- Multiple GND pins for maximum noise immunity

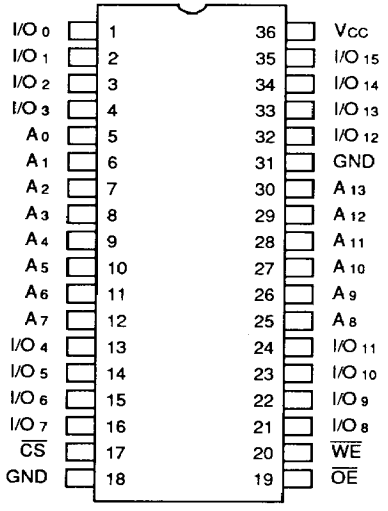
DESCRIPTION:

The IDT7MC4005 is a 16K x 16 CMOS static RAM module constructed on a co-fired ceramic substrate using four 16K x 4 static RAMs in leadless chip carriers. Extremely fast speeds can be achieved due to the use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS™ technology. The IDT7MC4005 is available with access times as fast as 15ns, with minimal power consumption.

The IDT7MC family of ceramic DSIPs offers the optimum in packing density and profile height. The IDT7MC4005 is packaged in a 36-pin ceramic DSIP (Dual Single In-line Package). The dual row configuration allows 36 pins to be placed on a package 1.8 inches long and .27 inches wide. At only .500 inches high, this low profile package is ideal for systems with minimum board spacing.

All inputs and outputs of the IDT7MC4005 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

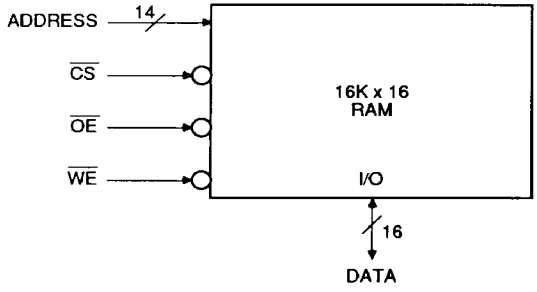
PIN CONFIGURATION(1)



2706 Drw 01

NOTE:
1. For module dimensions, please refer to module drawing M42 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



2706 drw 02

PIN NAMES

I/O0-15	Data Inputs/Outputs
A0-13	Address Inputs
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
VCC	Power
GND	Ground

2706 tbl 01

CEMOS is a trademark of Integrated Device Technology, Inc.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–10 to +85	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

2706 tbl 02

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	—	0.8	V

2706 tbl 03

NOTE:
1. V_{IL} (min.) = –3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND VOLTAGE SUPPLY

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 10%

2706 tbl 04

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address and Control)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	20	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max., V_{IN} = GND to V_{CC}	—	5	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	—	5	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	—	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4mA	2.4	—	V

2706 tbl 05

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Test Conditions	IDT7MC4005 Max.(1)	IDT7MC4005 Max.(2)	Unit
I_{CC1}	Operating Current	f = 0, $\overline{CS}$ = V_{IL} V_{CC} = Max., Output Open	480	400	mA
I_{CC2}	Dynamic Operating Current	f = f_{MAX}, $\overline{CS}$ = V_{IL} V_{CC} = Max., Outputs Open	600	500	mA
I_{SB}	Standby Supply Current	f = f_{MAX}, $\overline{CS}$ ≥ V_{IH} V_{CC} = Max., Outputs Open	240	200	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} - 0.2V V_{IN} ≥ V_{CC} - 0.2V or ≤ 0.2V	80	60	mA

2706 tbl 06

NOTE:
1. For tAA = 15, 20, 25ns versions.
2. For tAA = 30, 35ns versions.

8

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2706 tbl 08

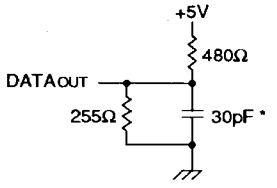
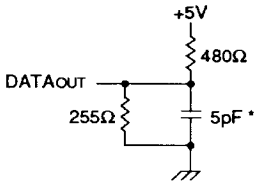


Figure 1. Output Load



2706 drw 03

Figure 2. Output Load (for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

* Including scope and jig

AC ELECTRICAL CHARACTERISTICS

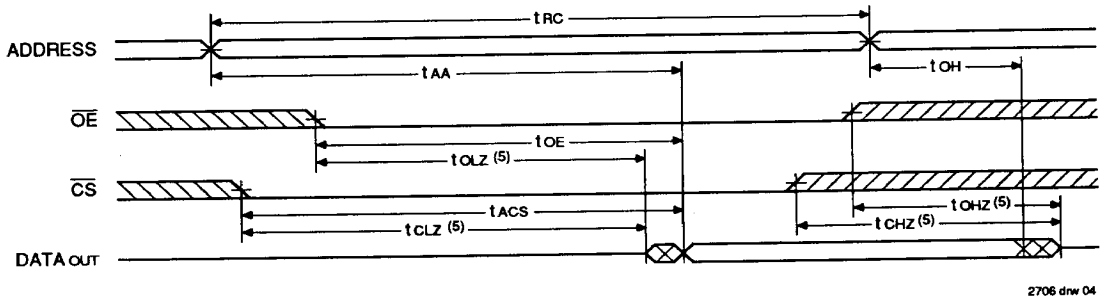
(V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameters	7MC4005S15 Min.	7MC4005S15 Max.	7MC4005S20 Min.	7MC4005S20 Max.	7MC4005S25 Min.	7MC4005S25 Max.	7MC4005S30 Min.	7MC4005S30 Max.	7MC4005S35 Min.	7MC4005S35 Max.	Unit
Read Cycle												
t_{RC}	Read Cycle Time	15	—	20	—	25	—	30	—	35	—	ns
t_{AA}	Address Access Time	—	15	—	20	—	25	—	30	—	35	ns
t_{ACS}	Chip Select Access Time	—	15	—	20	—	25	—	30	—	35	ns
t_{CLZ} (1)	Chip Select to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{OE}	Output Enable to Output Valid	—	12	—	15	—	15	—	20	—	20	ns
t_{OLZ} (1)	Output Enable to Output in Low Z	5	—	5	—	5	—	5	—	5	—	ns
t_{CHZ} (1)	Chip Select to Output in High Z	—	8	—	8	—	10	—	13	—	15	ns
t_{OHZ} (1)	Output Disable to Output in High Z	—	8	—	8	—	15	—	15	—	15	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
t_{PU} (1)	Chip Select to Power Up Time	0	—	0	—	0	—	0	—	0	—	ns
t_{PD} (1)	Chip Deselect to Power Down Time	—	15	—	20	—	25	—	30	—	35	ns
Write Cycle												
t_{WC}	Write Cycle Time	13	—	17	—	20	—	25	—	30	—	ns
t_{CW}	Chip Select to End of Write	13	—	17	—	20	—	25	—	25	—	ns
t_{AW}	Address Valid to End of Write	13	—	17	—	20	—	25	—	27	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	12	—	17	—	20	—	25	—	25	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
t_{WHZ} (1)	Write Enable to Output in High Z	—	6	—	7	—	7	—	10	—	10	ns
t_{DW}	Data to Write Time Overlap	8	—	10	—	13	—	15	—	15	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	0	—	0	—	ns
t_{OW} (1)	Output Active from End of Write	5	—	5	—	5	—	5	—	5	—	ns

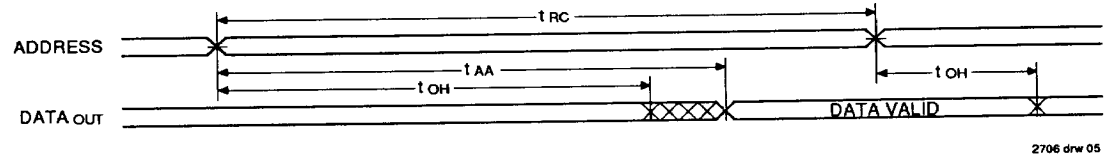
2706 tbl 07

NOTE:
1. This parameter is guaranteed by design but not tested.

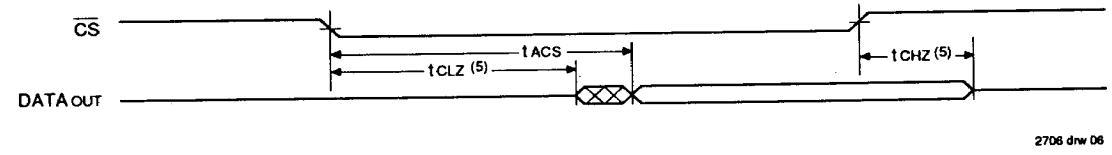
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)



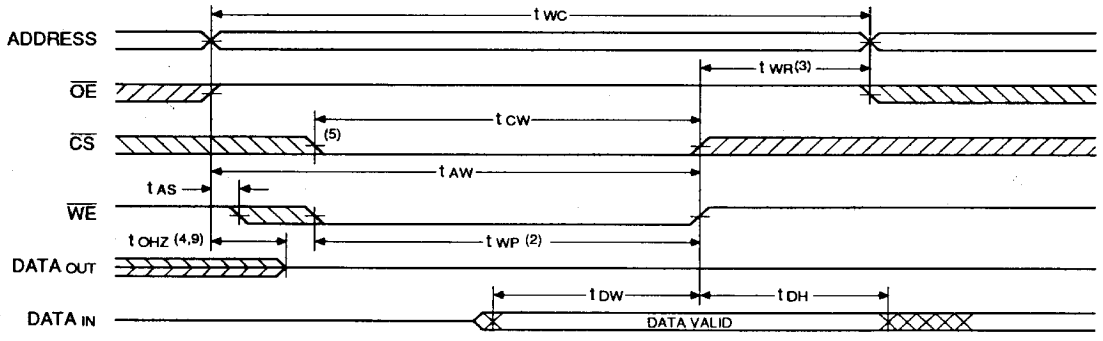
TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)



NOTES:
1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = VIL.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = VIL.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

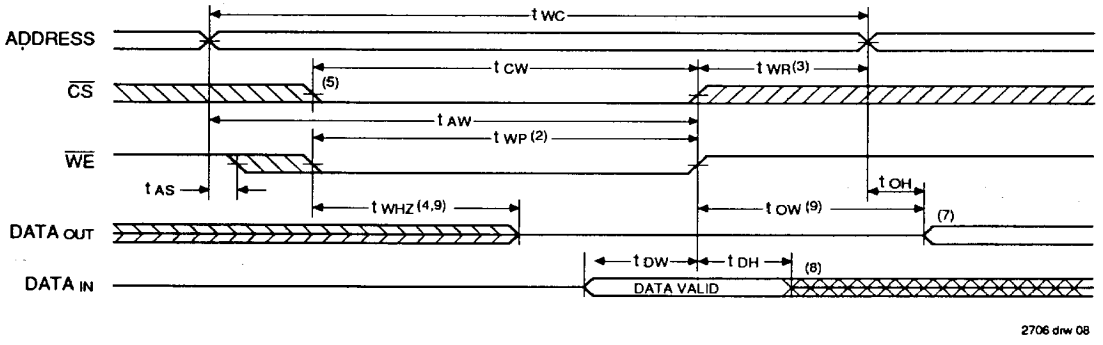
8

TIMING WAVEFORM OF WRITE CYCLE NO. 1(1)



2706 drw 07

TIMING WAVEFORM OF WRITE CYCLE NO. 2(1, 6)



2706 drw 08

NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tWP) of a low $\overline{CS}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the output must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = VIL).
7. DOUT is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is guaranteed by design but not tested.

TRUTH TABLE

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Standby	H	X	X	High Z	Standby
Read	L	L	H	DOUT	Active
Write	L	X	L	DIN	Active
Read	L	H	H	High Z	Active

2706 tbl 09

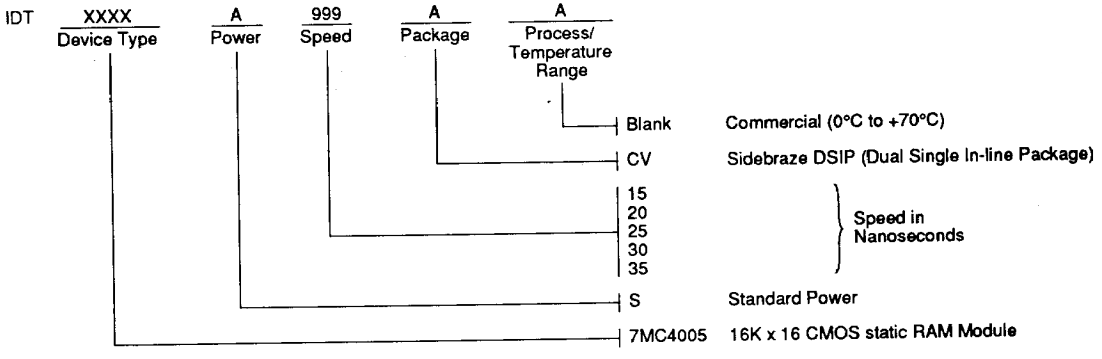
CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Typ.	Unit
CIN (D)	Input Capacitance (Data)	VIN = 0V	20	pF
CIN (A)	Input Capacitance Address and Control	VIN = 0V	50	pF
COUT	Output Capacitance	VOUT = 0V	20	pF

2706 tbl 10

NOTE:
1. This parameter is guaranteed by design but not tested.

ORDERING INFORMATION



2706 drw 10

8