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PRODUCT PROFILE

FUJITSU

MB85410-30/40**CMOS STATIC RAM MODULE****65536 Words x 8-Bit**

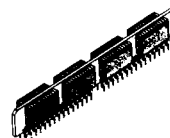
The Fujitsu MB85410 is a fully decoded, CMOS static random access memory module (SRAM) with eight MB81C71A devices mounted on a 60-pin Epoxy module. Two ENABLE pins permit expansion to 128K four bit words. Additionally, these modules incorporate a presence detect feature that permits system level memory density verification for those applications with multiple modules. Organized as eight 64K x 1 devices, the MB85410 is optimized for memory applications where low power, high performance, large memory storage, and high density are required.

- Organized as 65536 x 8-Bit Words
- Access Time/Cycle Time
–30: 30 ns Max.
–40: 40 ns Max.
- Low Power Dissipation
Active: 3520 mW max
Standby: 440 mW
CMOS Level
880 mW
TTL Level
- Static Operation
- Single +5 V \pm 10% Power Supply
- Dual ENABLE Pins (x4, x8)
- Input/Output Pins TTL Compatible
- 60-pin Epoxy Module (ZIP)
- Presence Detect: PD0 = GND;
PD1 = Open
- Temperature Range: 0°C to 70°C
- Separate Data Inputs and Outputs

ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Value	Rating
Supply Voltage	V _{CC}	-0.5 to +7.0	V
Input Voltage	V _{IN}	-3.5 to +7.0	V
Output Voltage	V _{OUT}	-0.5 to +7.0	V
Short Circuit Output Current	I _{OUT}	\pm 50	mA
Power Dissipation	P _D	8.0	W
Temperature under Bias	T _{BIAS}	-10 to +85	°C
Storage Temperature	T _{STG}	-45 to +125	°C

NOTE: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operational section of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PRELIMINARY

PLASTIC PACKAGE
MZP-60P-P02

PIN ASSIGNMENT

PD0	2	1	VSS
NC	4	3	PD1
VCC	6	5	NC
D0	8	7	D1
Q0	10	9	Q1
A0	12	11	NC
A2	14	13	A1
A4	16	15	A3
A6	18	17	A5
VSS	20	19	A7
D2	22	21	D3
Q2	24	23	Q3
WE	26	25	VCC
NC	28	27	NC
CS1	30	29	NC
NC	32	31	CS2
NC	34	33	NC
VCC	36	35	NC
D4	38	37	D5
Q4	40	39	Q5
A8	42	41	VSS
A10	44	43	A9
A12	46	45	A11
A14	48	47	A13
NC	50	49	A15
D6	52	51	D7
Q6	54	53	Q7
NC	56	55	VCC
NC	58	57	NC
VSS	60	59	NC

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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MB85410-30/-40**CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$)**

PARAMETER	SYMBOL	VALUE		UNIT
		Typ	Max	
Input Capacitance, Address and WE	C_{IN1}		80	pF
Input Capacitance, \overline{CS}_1 and \overline{CS}_2	C_{IN2}		40	pF
Input Capacitance, D_{IN}	C_{IN3}		10	pF
Output Capacitance, D_{OUT}	C_{OUT}		10	pF

DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted)

PARAMETER	SYMBOL	VALUE			UNIT
		Min	Typ	Max	
Input Leakage Current ($V_{IN} = 0\text{V to }V_{CC}$)	I_{LI}	-80		80	μA
Output Leakage Current ($\overline{CS} = V_{IH}$, $V_{OUT} = 0\text{V to }V_{CC}$)	I_{LO}	-10		10	μA
Standby Power Supply Current	CMOS level			80	mA
	TTL level			160	mA
Active Power Supply Current ($\overline{CS} = V_{IL}$, $I_{OUT} = 0\text{ mA}$)	I_{CC}			640	mA
Peak Power on Supply Current ($\overline{CS} = \text{Lower of }V_{CC}\text{ or }V_{IH}$)	I_{PO}			240	mA
Input High Level	V_{IH}	2.2		6.0	V
Input Low Level ¹	V_{IL}	-0.5		0.8	V
Output High Level ($I_{OH} = -4\text{ mA}$)	V_{OH}	2.4			V
Output Low Level ($I_{OL} = 16\text{ mA}$)	V_{OL}			0.4	V

Note: ¹-2.0V level with a maximum pulse width of 20 ns.

MB85410-30/-40**AC CHARACTERISTICS**

(At recommended operating conditions unless otherwise noted)*

READ CYCLE

PARAMETER	SYM	MB85410-30		MB85410-40		UNIT	NOTE
		Min	Max	Min	Max		
Read Cycle Time	t_{RC}	30		40		ns	1
Address Access Time	t_{AA}		30		40	ns	
\overline{CS} Access Time	t_{ACS}		30		40	ns	2
Output Hold from Address Change	t_{OH}	5		5		ns	
\overline{CS} to Output Low-Z	t_{LZ}	5		5		ns	3,4
\overline{CS} to Output High-Z	t_{HZ}	0	10	0	15	ns	3,4
Power Up from \overline{CS}	t_{PU}	0		0		ns	
Power Down from \overline{CS}	t_{PD}		20		30	ns	

WRITE CYCLE

PARAMETER	SYM	MB85410-30		MB85410-40		UNIT	NOTE
		Min	Max	Min	Max		
Write Cycle Time	t_{WC}	30		40		ns	2
Address Valid to End of Write	t_{AW}	25		35		ns	
\overline{CS} to End of Write	t_{CW}	25		35		ns	
Data Hold Time	t_{DH}	2		2		ns	
Write Pulse Width	t_{WP}	20		30		ns	
Data Valid to End of Write	t_{DW}	15		20		ns	
Address Setup Time	t_{AS1}	0		0		ns	
	t_{AS2}	0		0		ns	
Write Recovery Time	t_{WR}	2		2		ns	
Output High-Z from \overline{WE}	t_{WZ}	0	10	0	15	ns	3,4
Output Low-Z from \overline{WE}	t_{OW}	0		0		ns	3,4

Notes: * Refer to MB81C71A data sheet electricals for an explanation of the notes.

