VITELIC

V62C256 FAMILY
HIGH PERFORMANCE LOW POWER
32K x 8 BIT
CMOS STATIC RAM

Features

- High speed
  - Maximum access time of 100 ns to 150 ns
  - Equal access and cycle times
- Low power
  - 200 mW typical operating
  - 10 μW typical standby
- Battery backup
  - 2 volt data retention
- Output enable and chip enable input for ease in application
- Fully static operation
  - No clock or refresh required

Description

The V62C256 is a high speed, low power, 32,768-word by 8-bit CMOS static RAM fabricated using high-performance MIX-MOS technology. This high reliability process coupled with innovative circuit design techniques, yields access times of 100 ns. maximum.

When the chip is deselected, the device assumes a standby mode in which the device power dissipation is reduced to 10 μW (typically). The V62C256 has a data retention mode which guarantees that data will remain valid at a minimum power supply voltage of 2.0 volts.

The V62C256 is packaged in standard 28 pin DIP and mini flat (SOIC) packages.

Device Usage Chart

Operating Temperature Range	Package Outline				Access Time (ns)			Power		Temperature Mark
	P	D	F	G	100	120	150	Low	Std.	
0°C to 70°C	•	•	•	•	•	•	•	•		Blank
−40°C to +85°C	•	•	•	•	•	•	•	•		I

Package	Std.	Pin Count
Plastic DIP	P	28
SOIC (Mini Flat Pack)	F	28
CERDIP	D	28
Ceramic LCC	G	32

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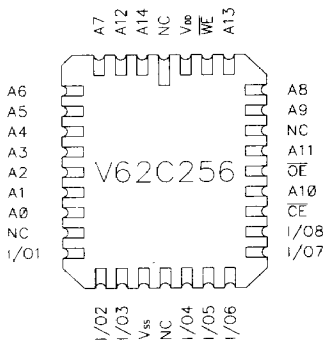
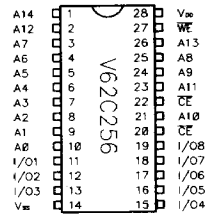
Family Device Package Speed Power Temp

LCC PIN CONFIGURATION
Top View



DIP/SOIC PIN CONFIGURATION
Top View



Truth Table

Mode	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	I/O	I_{DD}
Not Selected	X	H	X	High-Z	Standby
D_{OUT} Disable	H	L	H	High-Z	Active
Read	L	L	H	D_{OUT}	Active
Write	X	L	L	D_{IN}	Active

Absolute Maximum Ratings (1)

Symbol	Parameter	Rating	Unit
V_{TERM}	Terminal Voltage with Respect to V_{SS}	−0.5* to +7.0	V
P_T	Power Dissipation	1.0	W
T_{OPR}	Operating Temperature	−40 to +85	°C
T_{STG}	Storage Temperature	−55 to +150	°C

NOTE:

1. Operation at or near absolute maximum ratings can affect device reliability.

Capacitance

T_A = 25°C, f = 1 MHz

Symbol	Parameter	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	—	7	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	—	10	pF

NOTE:
This parameter is sampled and not 100% tested.

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}		0	0	0	V
V_{IH}	Input Voltage	2.2	—	V_{DD} + 0.3	V
V_{IL}		−0.5*	—	0.8	V

*V_{DD}, V_{IN}, $V_{I/O}$ for pulse width less than 50 ns is −3.0V.

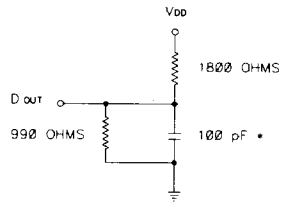


Fig 1.

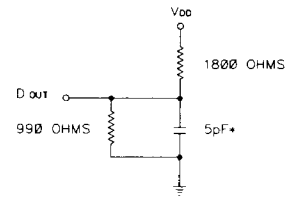
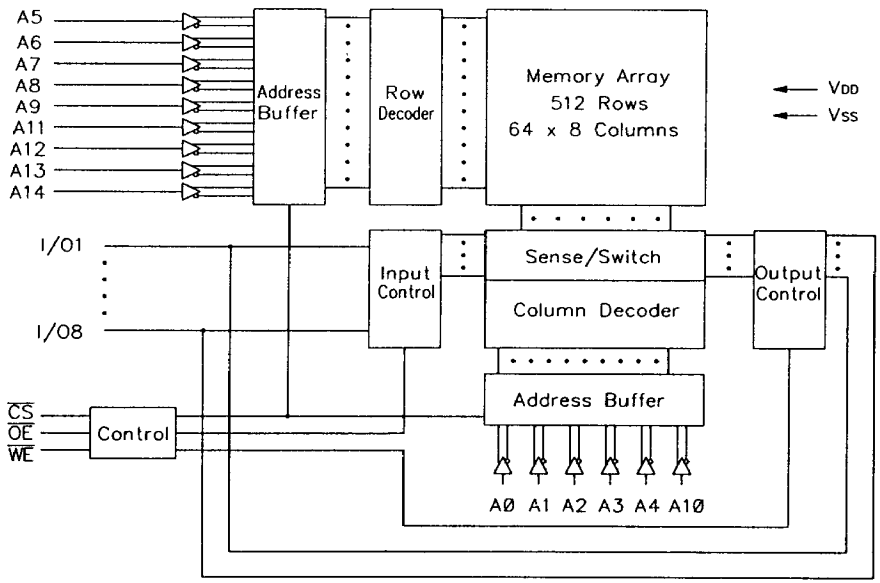


Fig 2.

*Includes test fixture and scope capacitance

BLOCK DIAGRAM



DC Characteristics

For operating characteristics, refer to Temperature Range Marking

Symbol	Parameter	Test Conditions	Range	100, 120, 150			Unit
				Min.	Typ. (1)	Max.	
$\|I_{LI}\|$	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{DD}	*—	—	—	1	µA
			**I	—	—	5	
$\|I_{LO}\|$	I/O Leakage Current	$V_{IO} = V_{SS}$ to V_{DD} $\overline{CE} \geq V_{IH}$ or $OE \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$	—	—	—	1	µA
			I	-	—	5	
I_{DD}	Dynamic Operating Current	$\overline{CE} \geq V_{IL}$, $V_{IH} \leq V_{IN} \leq V_{IL}$ Outputs Open Cycle = min, Duty Cycle = 100%	—	—	30	70	mA
			I	—	30	85	
I_{SB1}	CMOS Standby Current	$\overline{CE} \geq V_{DD} - 0.2V$	—	—	2	100	µA
			I	—	2	250	
I_{SB2}	TTL Standby Current	$\overline{CE} \geq V_{IH}$	—	—	0.3	3	mA
			I	—	0.3	6	
V_{OH}	Output High Voltage	$I_{OUT} = 2.1$ mA		2.4	—	—	V
V_{OL}	Output Low Voltage			—	—	0.4	

Low V_{DD} Data Retention Characteristics

Symbol	Parameter	Test Conditions	Range	100, 120, 150			Unit
				Min.	Typ. (1)	Max.	
V_{DDDR}	V_{DD} for Data Retention	$\overline{CE} \geq V_{DD} - 0.2V$ $V_{IN} = V_{SS}$ to V_{DD} $V_D = 3.0V$		2.0	—	5.5	V
I_{DDDR}	Data Retention Current		—	—	2.0	50	µA
			I	—	2.0	200	
t_{CDR}	Chip Deselect to Data Retention Time			0	—	—	ns
t_R	Operation Recovery Time			t_{RC} (2)	—	—	ns

NOTES:

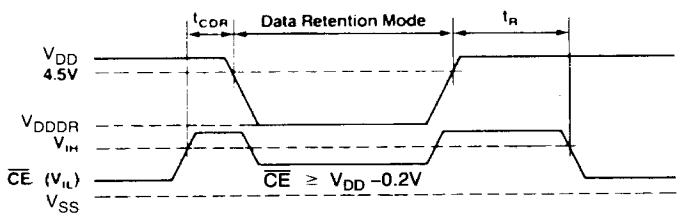
1. $V_{DD} = 5.0V$, $T_A = 25°C$
2. t_{RC} = Read Cycle Time

* (—) $T_A = 0°C$ to $70°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$

** (I) $T_A = 40°C$ to $+85°C$, $V_{DD} = 5V \pm 10\%$, $V_{SS} = 0V$

For availability in a particular temperature range, refer to Device Usage Chart, Page 53

Data Retention Timing Waveform



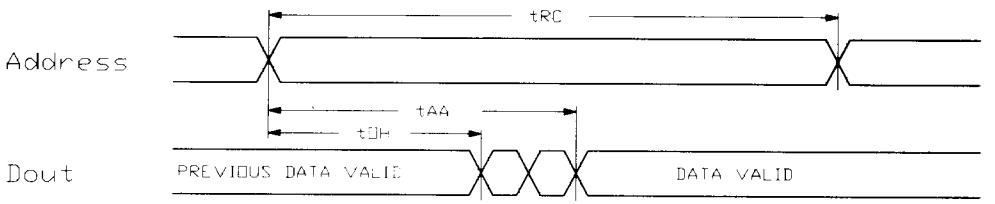
AC Characteristics

At recommended operating conditions, unless otherwise specified.

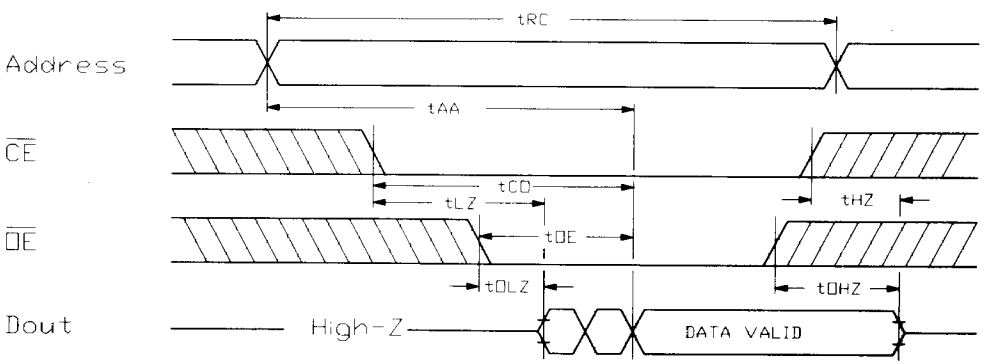
Read Cycle

Symbol	Parameter	-10L		-12L		-15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read Cycle Time	100	—	120	—	150	—	ns
t_{AA}	Address Access Time	—	100	—	120	—	150	ns
t_{CO}	Chip Enable Access Time	—	100	—	120	—	150	ns
t_{OE}	Output Enable to Output Valid	—	50	—	60	—	70	ns
t_{OH}	Output Hold from Address Change	10	—	10	—	10	—	ns
t_{LZ}	Chip Enable to Output in Low-Z	10	—	10	—	10	—	ns
t_{OLZ}	Output Enable to Output in Low-Z ($\overline{OE}$)	5	—	5	—	5	—	ns
t_{HZ}	Chip Deselection to Output in High-Z	—	35	—	40	—	50	ns
t_{OHZ}	Chip Disable to Output in High-Z ($\overline{OE}$)	—	35	—	40	—	50	ns

Read Cycle No. 1 (Address Access) (1, 2)



Read Cycle No. 2 (Chip Enable Access) (1, 2, 3)

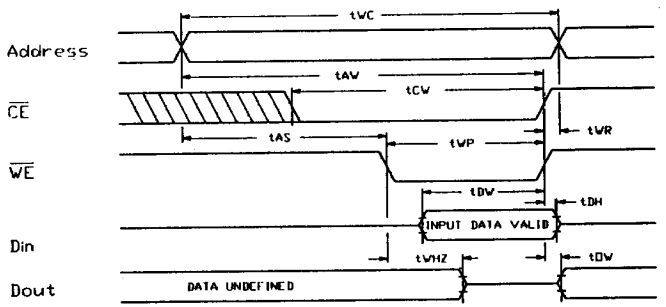


AC Characteristics

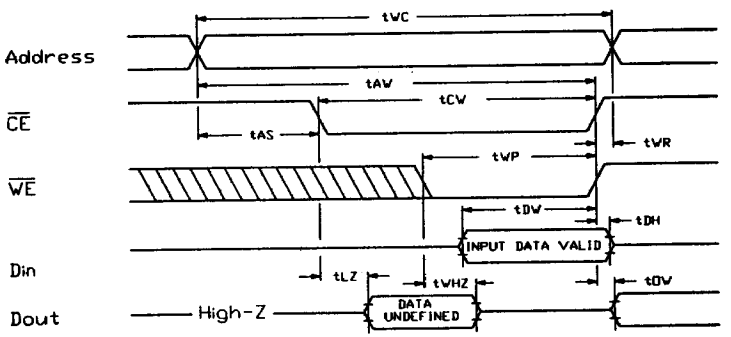
Write Cycle

Symbol	Parameter	-10L		-12L		-15L		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{WC}	Write Cycle Time	100	—	120	—	150	—	ns
t_{AW}	Address Valid to End of Write	80	—	85	—	100	—	ns
t_{CW}	Chip Enable to End of Write	80	—	85	—	100	—	ns
t_{DW}	Data to Write Overlap	40	—	50	—	60	—	ns
t_{DH}	Data Hold from Write Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	70	—	70	—	90	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time $\overline{WE}$	5	—	5	—	5	—	ns
t_{OW}	Output Active from End of Write	10	—	10	—	10	—	ns
t_{WHZ}	Write to Output in High-Z	—	35	—	40	—	50	ns

Write Cycle No. 1 ($\overline{WE}$ Controlled) (1, 2, 3)



Write Cycle No. 2 ($\overline{CE}$ Controlled) (1, 2)



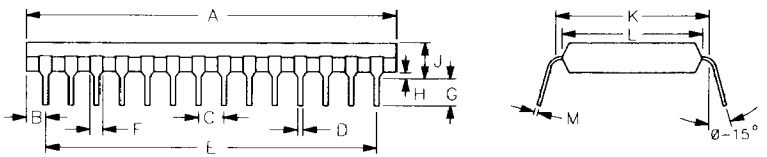
NOTES:

1. A write occurs during the overlap of a low $\overline{CE}_1$ and a high CE_2 and a low $\overline{WE}$.
2. $\overline{CE}_1$ or $\overline{WE}$ or (CE_2) must be high (low) during address transition.
3. If $\overline{OE}$ is high, I/O pins remain in a high impedance state.
4. During this period, I/O pins are in the output state, therefore the input signals of the opposite phase to the outputs must not be applied.

Package Outline

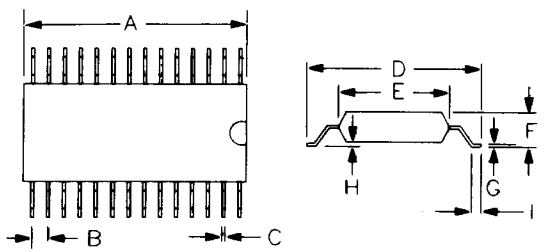
28 Pin Plastic

Item	Inches	Millimeters
A	1.46 max.	37.2 max.
B	.082	2.09
C	.10	2.54
D	.015/.020	.381/.508
E	1.3	33.02
F	.040/.065	1.016/1.651
G	.125/.160	3.175/4.064
H	.015/.065	.381/1.651
J	.170/.220	4.318/5.588
K	.590/.610	14.986/15.494
L	.530/.550	13.462/13.970
M	.009/.012	229/.305



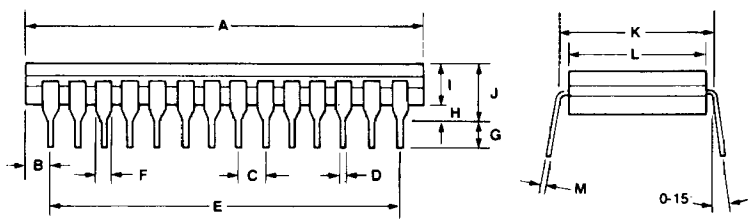
28 Pin SOIC

Dimension	Inches	Millimeters
A	.700	17.78
B	.05	1.27
C	.011/.019	0.279/.483
D	0.48 max.	12.192 max.
E	0.33 max.	8.38 max.
F	.100	2.54
G	.004/.010	.102/.254
H	.004	.102
I	.035	.889



28 Pin Cer DIP

Dimension	Inches	Millimeters
A	1.5 max.	38.10 max.
B	.110	2.76
C	.100	2.54
D	.014/.023	0.36/0.58
E	1.3	33.02
F	.030/.070	0.76/1.78
G	.10 min.	2.54 min.
H	.015/.060	0.38/1.52
J	.200	5.08
L	.520/.610	13.208/15.494
M	.008/.015	.20/.38



32 LCC

Dimension	Inches	Millimeters
A	.544/.556	13.818/14.122
B	.045/.055	1.143/1.397
C	.045/.055	1.143/1.397
D	.022/.028	.559/.711
E	.3	7.62
F	.445/.455	11.303/11.557
J	.054/.066	1.372/1.676