System Power Supply ICs for CCD Camera of Mobile Phones

Power Supply for CCD Camera Module

BD6039GU

No.10033EAT02

●Description

BD6039GU is system power supply LSI for CCD camera that supplies all voltage sources for CCD camera.
This IC has Step up DC/DC converter and LDO for CCD sensor, Inverted DC/DC converter for CCD sensor, and LDO (7ch).
REGA, REG1, REG8, REG5 can be connected the power supply independent from VBAT.
Each output voltage has an adjustable by the register, and this IC can correspond to various CCD modules.
A necessary power supply for CCD camera system is integrated into 1chip, and it contributes to space saving.
BD6039GU achieves compact size with the chip size package.

●Features

1) The BD6039GU is equipped with all voltage sources for CCD camera system.
2) Each output has an adjustable voltage; hence this IC can correspond to various CCD modules.
3) The BD6039GU is controlled by I^2C BUS format.
4) The BD6039GU employs 4.8mm^2 chip size package, so this IC achieves compact size.

●Functions

1) Step up DC/DC converter and LDO for CCD sensor (+15V/+14.5V/+13V)
2) Inverted DC/DC converter for CCD sensor (-8V/-7.5V/-7V)
3) 7ch Series Regulator
   REG1 : 1.2V, Iomax=210mA
   REG2 : 3.0V, Iomax=50mA
   REG5 : 1.5V/1.8V, Iomax=100mA
   REG6 : 3.2V/3.3V, Iomax=260mA
   REG7 : 3.0V/3.3V, Iomax=50mA
   REG8 : 1.5V/1.8V, Iomax=100mA
   REGA : 1.5V/1.8V, Iomax=100mA
4) Correspondence to I^2C BUS format
5) Thermal shutdown (Auto-return type)
6) VCSP85H4 chip size package (1.0mm max)

●Absolute Maximum Ratings(Ta=25℃)

Parameter		Symbol	Ratings	Unit
Maximum Applied voltage 1	(Note 1)	VMAX1	20	V
Maximum Applied voltage 2	(Note 2)	VMAX2	18	V
Maximum Applied voltage 3	(Note 3)	VMAX3	-13.5	V
Maximum Applied voltage 4	(Note 4)	VMAX4	6	V
Power Dissipation	(Note 5)	Pd	2110	mW
Operating Temperature Range		Topr	-30 ～ +85	℃
Storage Temperature Range		Tstg	-55 ～ +150	℃

(Note 1) SWP, VPLUS1, VPLUS2 pin
(Note 2) VDD3 pin
(Note 3) VDD4, SWN pin
(Note 4) Except Note1~Note3 pin
(Note 5) Power dissipation deleting is 16.9mW/ ℃, when it's used in over 25℃.
(It's deleting is on the board that is ROHM's standard)

●Recommended Operating Conditions (VBAT≥VIO, Ta=-30~85 ℃)

Parameter	Symbol	Limits	Unit
VBAT input voltage	VBAT	2.7 ～ 5.5	V
VIO pin voltage	VIO	1.65 ～ 3.3	V

●**Electrical Characteristics(Unless otherwise specified, Ta=25℃, VBAT=3.6V, VIO=1.8V)**

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
【Circuit Current】						
VBAT Circuit current 1	IBAT1	-	0.1	3.0	μA	RST=0V, VIO=0V
VBAT Circuit current 2	IBAT2	-	0.5	3.0	μA	RST=0V, VIO=1.8V
VBAT Circuit current 3	IBAT3	-	115	175	μA	REG1:ON, Io=0mA
VBAT Circuit current 4	IBAT4	-	115	175	μA	REG2:ON, Io=0mA
VBAT Circuit current 5	IBAT5	-	127	195	μA	REG5:ON, Io=0mA
VBAT Circuit current 6	IBAT6	-	145	220	μA	REG6:ON, Io=0mA
VBAT Circuit current 7	IBAT7	-	115	175	μA	REG7:ON, Io=0mA
VBAT Circuit current 8	IBAT8	-	127	195	μA	REG8:ON, Io=0mA
VBAT Circuit current 9	IBAT9	-	127	195	μA	REGA:ON, Io=0mA
VBAT Circuit current 10	IBAT10	-	9	14	mA	SWREG3:ON,REG3:ON, SWREG4:ON, Io=0mA
UVLO detect voltage	UVLO	2.15	2.4	2.65	V	VBAT falling
【SWREG3(Step up DC/DC)】						
Output voltage 1	VoPD1	-	16.5	-	V	Io=40mA
Output voltage 1	VoPD2	-	16.0	-	V	Io=40mA
Output voltage 1	VoPD3	-	14.5	-	V	Io=40mA
Output current	IoPD	-	-	40	mA	(Note 6)
Efficiency	EffPD	-	(80)	-	%	Io=40mA(Note 6)
Oscillator frequency	foscPD	0.8	1.0	1.2	MHz	
SW saturation voltage	VsatPD	-	100	200	mV	Iin=100mA
Over voltage protection	OvPD	18.0	18.5	19.0	V	
Over current protection	OcPD	-	0.77	1	A	
Soft start current	SftPD	-	300	-	mA	
【SWREG4(Inverted DC/DC)】						
Output voltage 1	VoND1	-8.4	-8.0	-7.6	V	Io=40mA
Output voltage 2	VoND2	-7.9	-7.5	-7.1	V	Io=40mA
Output voltage 2	VoND3	-7.4	-7.0	-6.6	V	Io=40mA
Output current	IoND	-	-	40	mA	VBAT > 3.0V(Note 6)
Efficiency	EffND	-	(70)	-	%	Io=40mA(Note 6)
Oscillator frequency	foscND	0.8	1.0	1.2	MHz	
SW saturation voltage	VsatND	-	100	200	mV	Iin=100mA
Over voltage protection	OvND	-10.5	-10.0	-9.5	V	
Over current protection	OcND	-	0.77	1	A	
Soft start current	SftND	-	300	-	mA	
Discharge resister at OFF	ROFFN	0.5	1.0	1.5	kΩ	

(Note 6) The power efficiency changes with the fluctuation of external parts and the board mounting condition.

●**Electrical Characteristics(Unless otherwise specified, Ta=25℃, VBAT=3.6V, VIO=1.8V)**

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
【REG1 (1.2V LDO)】						
Output voltage	Vo1	1.140	1.20	1.260	V	Io=210mA
Load stability	ΔVo11	-	10	60	mV	Io=1~210mA, VIN1=1.8V
Input stability	ΔVo12	-	10	60	mV	VBAT=3.2~4.5V, Io=210mA, VIN1=1.8V
Ripple rejection ratio	RR1	-	50	-	dB	f=100Hz, VBAT(AC)=200mVp-p, VIN1=1.8V, Io=50mA, BW=20Hz~20kHz
Short circuit current limit	Ilim01	-	200	400	mA	Vo=0V
Discharge resister at OFF	ROFF1	-	1.0	1.5	kΩ	
【REG2 (3.0V LDO)】						
Output voltage	Vo2	2.910	3.00	3.090	V	Io=50mA
Output voltage	Vsat2	-	0.2	0.3	V	VBAT=2.5V, Io=50mA
Load stability	ΔVo21	-	10	60	mV	Io=1~50mA
Input stability	ΔVo22	-	10	60	mV	VBAT=3.4~4.5V, Io=50mA
Ripple rejection ratio	RR2	-	60	-	dB	f=100Hz, VBAT(AC)=200mVp-p Io=50mA, BW=20Hz~20kHz
Short circuit current limit	Ilim02	-	50	100	mA	Vo=0V
Discharge resister at OFF	ROFF2	-	1.0	1.5	kΩ	
【REG3 (15V/14.5V/13V LDO)】						
Output voltage1	Vo31	14.55	15.0	15.45	V	Io=40mA
Output voltage2	Vo32	14.05	14.5	14.95	V	Io=40mA
Output voltage3	Vo33	12.55	13.0	13.45	V	Io=40mA
Output voltage	Vsat3	-	0.32	0.5	V	VPLUS2=11V, Io=40mA
Load stability	ΔVo31	-	20	80	mV	Io=1～40mA
Input stability	ΔVo32	-	10	60	mV	VPLUS2=16.5～17.5V, Io=40mA
Output voltage temperature fluctuation rate	ΔVo33	-	±100	-	ppm/℃	Ta=-30℃～85℃, Io=40mA
Output ripple voltage	RR3	-	-	3	mVp-p	Io=40mA, BW=20Hz～80kHz(Note 7)
Short circuit current limit	Ilim03	-	100	-	mA	Vo=0V
Discharge resister at OFF	ROFF3	0.5	1.0	1.5	kΩ	
【REG5 (1.5V/1.8V LDO)】						
Output voltage1	Vo51	1.440	1.50	1.560	V	Io=100mA
Output voltage2	Vo52	1.746	1.80	1.854	V	Io=100mA
Output voltage	Vsat5	-	0.09	0.14	V	VIN5=1.7V, Io=100mA, Vo=1.8V
Load stability	ΔVo51	-	10	60	mV	Io=1~100mA, Vo=1.8V, VIN5=2.8V
Input stability	ΔVo52	-	10	60	mV	VBAT=3.3~4.5V, Io=100mA, Vo=1.8V VIN5=2.8V
Ripple rejection ratio	RR5	-	50	-	dB	f=100Hz, VBAT(AC)=200mVp-p, Vo=1.8V VIN5=2.8V, Io=50mA, BW=20Hz~20kHz
Short circuit current limit	Ilim05	-	200	400	mA	Vo=0V
Discharge resister at OFF	ROFF5	-	1.0	1.5	kΩ	
【REG6 (3.2V/3.3V LDO)】						
Output voltage1	Vo61	3.104	3.20	3.296	V	Io=260mA
Output voltage2	Vo62	3.201	3.30	3.399	V	Io=260mA
Output voltage	Vsat6	-	0.07	0.13	V	VIN6=3.2V, Io=260mA, Vo=3.3V
Load stability	ΔVo61	-	10	60	mV	Io=1~260mA, Vo=3.3V, VIN6=3.6V
Input stability	ΔVo62	-	10	60	mV	VBAT=3.4~4.5V, Io=260mA, Vo=3.3V VIN6=3.6V
Ripple rejection ratio	RR6	-	60	-	dB	f=100Hz, VBAT(AC)=200mVp-p, Vo=3.3V VIN6=3.8V, Io=50mA, BW=20Hz~20kHz
Short circuit current limit	Ilim06	-	250	500	mA	Vo=0V
Discharge resister at OFF	ROFF6	-	1.0	1.5	kΩ	

(Note 7) BW: Band width

●**Electrical Characteristics(Unless otherwise specified, Ta=25℃, VBAT=3.6V, VIO=1.8V)**

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
【REG7 (3.0V/3.3V LDO)】						
Output voltage1	Vo71	2.910	3.00	3.090	V	Io=50mA
Output voltage2	Vo72	3.201	3.30	3.399	V	Io=50mA
Output voltage	Vsat7	-	0.2	0.3	V	VBAT=2.5V, Io=50mA, Vo=3.0V
Load stability	Δvo71	-	10	60	mV	Io=1~50mA, Vo=3.0V
Input stability	Δvo72	-	10	60	mV	VBAT=3.4~4.5V, Io=50mA, Vo=3.0V
Ripple rejection ratio	RR7	-	60	-	dB	f=100Hz, VBAT(AC)=200mVp-p, Vo=3.0V Io=50mA, BW=20Hz~20kHz
Short circuit current limit	Ilim07	-	50	100	mA	Vo=0V
Discharge resister at OFF	ROFF7	-	1.0	1.5	kΩ	
【REG8 (1.5V/1.8V LDO)】						
Output voltage1	Vo81	1.440	1.50	1.560	V	Io=100mA
Output voltage2	Vo82	1.746	1.80	1.854	V	Io=100mA
Output voltage	Vsat8	-	0.09	0.14	V	VIN8=1.7V, Io=100mA, Vo=1.8V
Load stability	Δvo81	-	10	60	mV	Io=1~100mA, Vo=1.8V, VIN8=2.8V
Input stability	Δvo82	-	10	60	mV	VBAT=3.3~4.5V, Io=100mA, Vo=1.8V VIN8=2.8V
Ripple rejection ratio	RR8	-	50	-	dB	f=100Hz, VBAT(AC)=200mVp-p, Vo=1.8V VIN8=2.8V, Io=50mA, BW=20Hz~20kHz
Short circuit current limit	Ilim08	-	200	400	mA	Vo=0V
Discharge resister at OFF	ROFF8	-	1.0	1.5	kΩ	
【REGA (1.5V/1.8V LDO)】						
Output voltage1	VoA1	1.440	1.50	1.560	V	Io=100mA
Output voltage2	VoA2	1.746	1.80	1.854	V	Io=100mA
Output voltage	VsatA	-	0.09	0.14	V	VINA=1.7V, Io=100mA, Vo=1.8V
Load stability	ΔVoA1	-	10	60	mV	Io=1~100mA, Vo=1.8V, VINA=2.8V
Input stability	ΔVoA2	-	10	60	mV	VBAT=3.3~4.5V, Io=100mA, Vo=1.8V VINA=2.8V
Ripple rejection ratio	RRA	-	50	-	dB	f=100Hz, VBAT(AC)=200mVp-p, Vo=1.8V VINA=2.8V, Io=50mA, BW=20Hz~20kHz
Short circuit current limit	Ilim0A	-	200	400	mA	Vo=0V
Discharge resister at OFF	ROFFA	-	1.0	1.5	kΩ	
【I2C Input (RST, SDA, SCL)】						
LOW level input voltage	VIL	-0.3	-	0.25VIO	V	
HIGH level input voltage	VIH	0.75VIO	-	VBAT+0.3	V	
Hysteresis of Schmitt trigger input	Vhys	0.05VIO	-	-	V	
LOW level output voltage (SDA) at 3mA sink current	VOL	0	-	0.30	V	
Input current each I/O pin	Ii	-10	-	10	μA	input voltage from (0.1 x VIO) to (0.9 x VIO)

●Power Dissipation (On the ROHM's standard board)

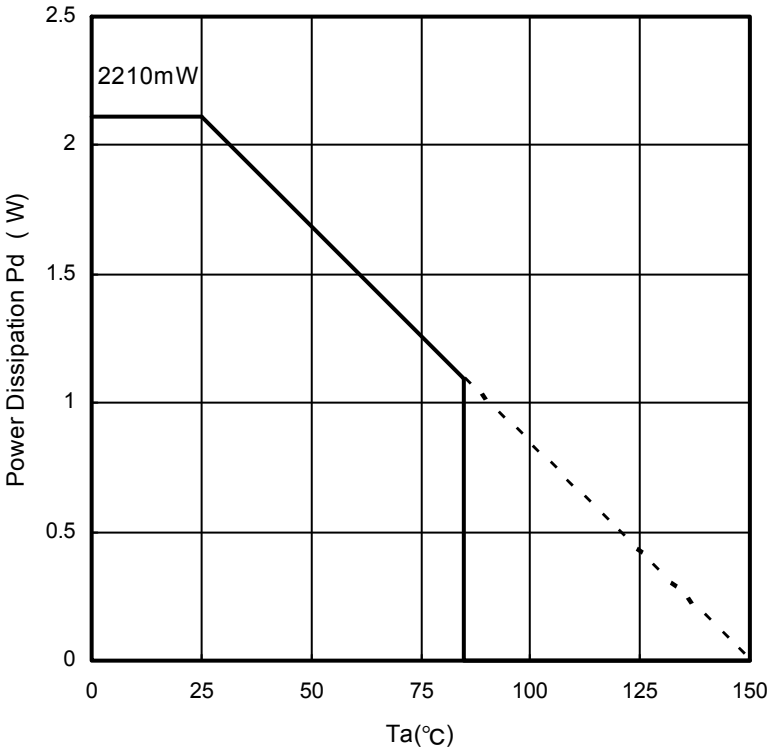


Fig.1 Power Dissipation

Information of the ROHM's standard board

Material	:	glass-epoxy
Size	:	50mm × 58mm × 1.75mm (8 Layer)
Pattern of the board		Refer to after page

●Block Diagram / Application Circuit Example

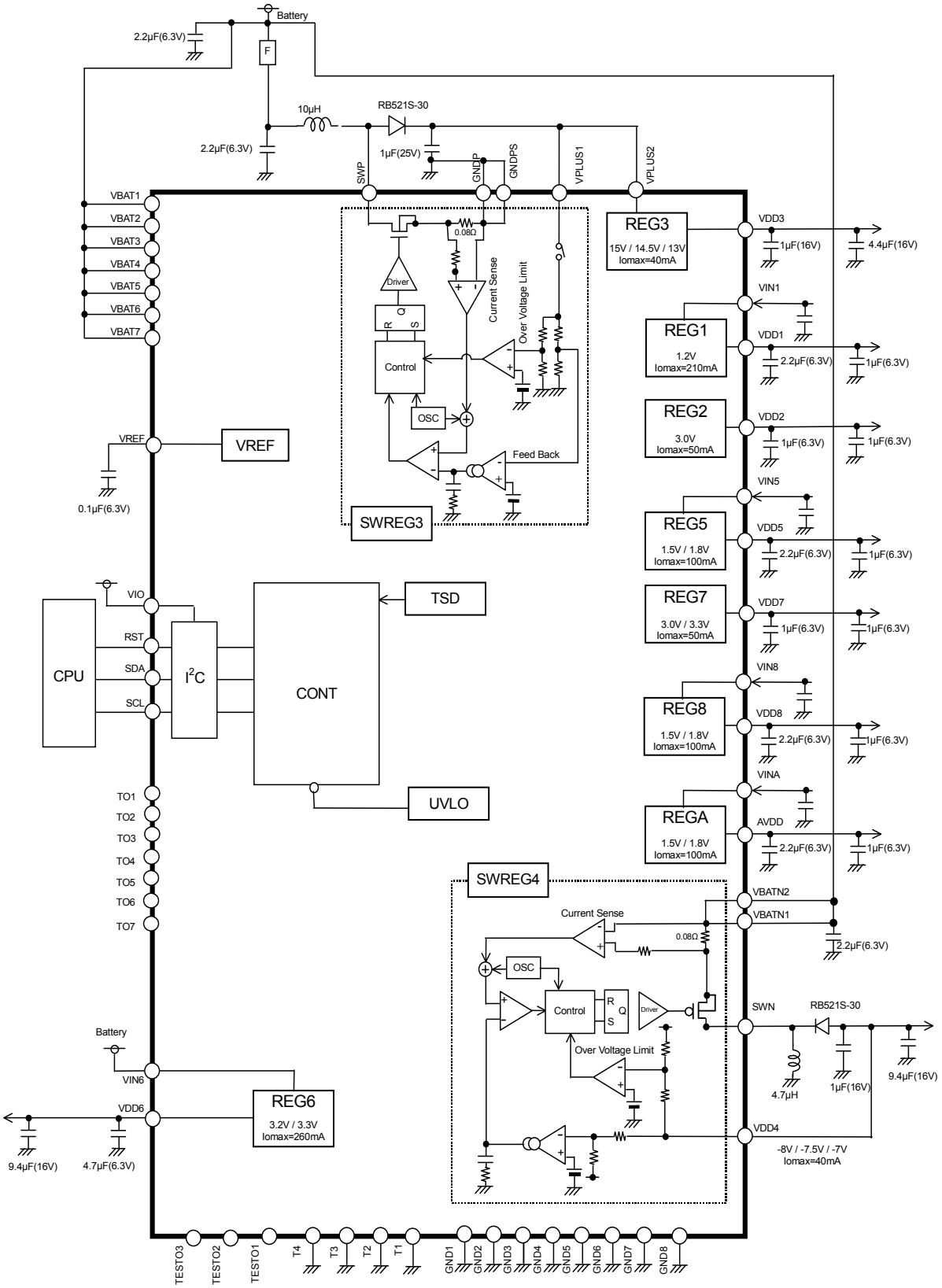


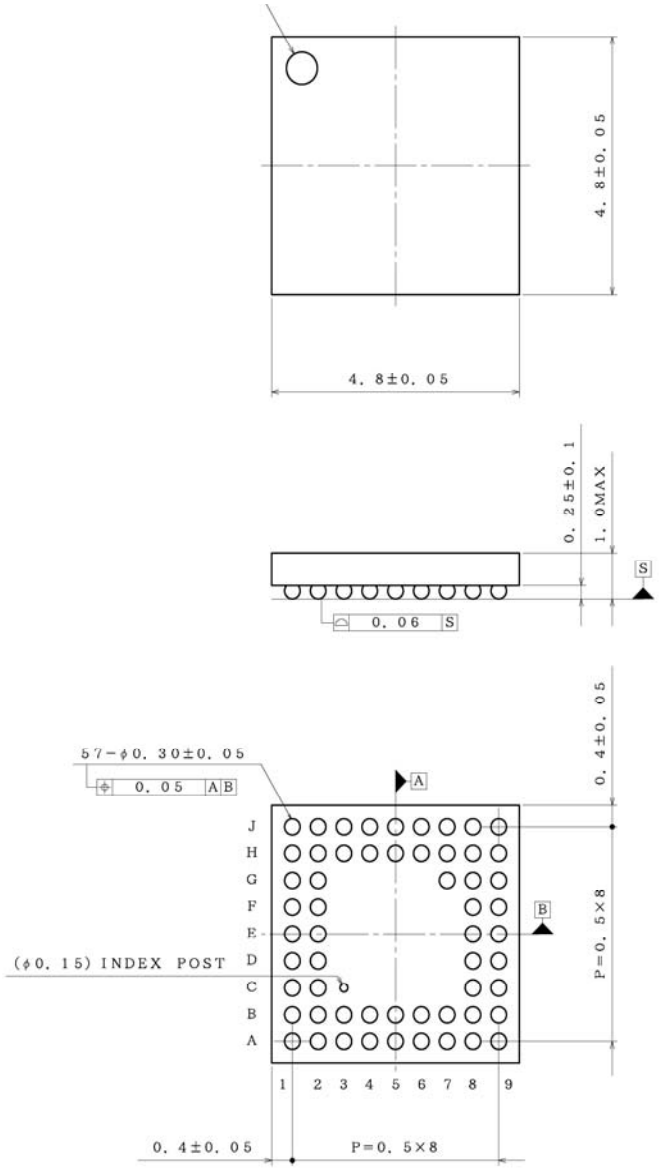
Fig.2 Block Diagram / Application Circuit example

●**Pin Configuration ［Bottom View］**

	1	2	3	4	5	6	7	8	9
J	T4	VDD3	VPLUS1	VBAT5	GND6	GNDP	SWP	AVDD	T3
H	VDD2	VBAT6	VPLUS2	TESTO3	TESTO1	GNDPS	VBAT4	VINA	VIN5
G	VDD7	TESTO2					NC	VDD5	VIN1
F	GND7	SDA						VDD1	VIN8
E	SCL	VIO						VDD8	VDD6
D	TO7	RST						VREF	VIN6
C	TO5	TO6	○					VBAT3	GND5
B	TO3	VBAT7	TO4	GND1	VBAT1	VBATN1	GND3	VBAT2	GND4
A	T1	TO1	TO2	GND8	SWN	VBATN2	GND2	VDD4	T2

●Package Outline

VCSP85H4 : CSP small package
SIZE : 4.8mm^2(A difference in public : X,Y Both ±0.05mm) Height 1.0mm max
A ball pitch : 0.5 mm

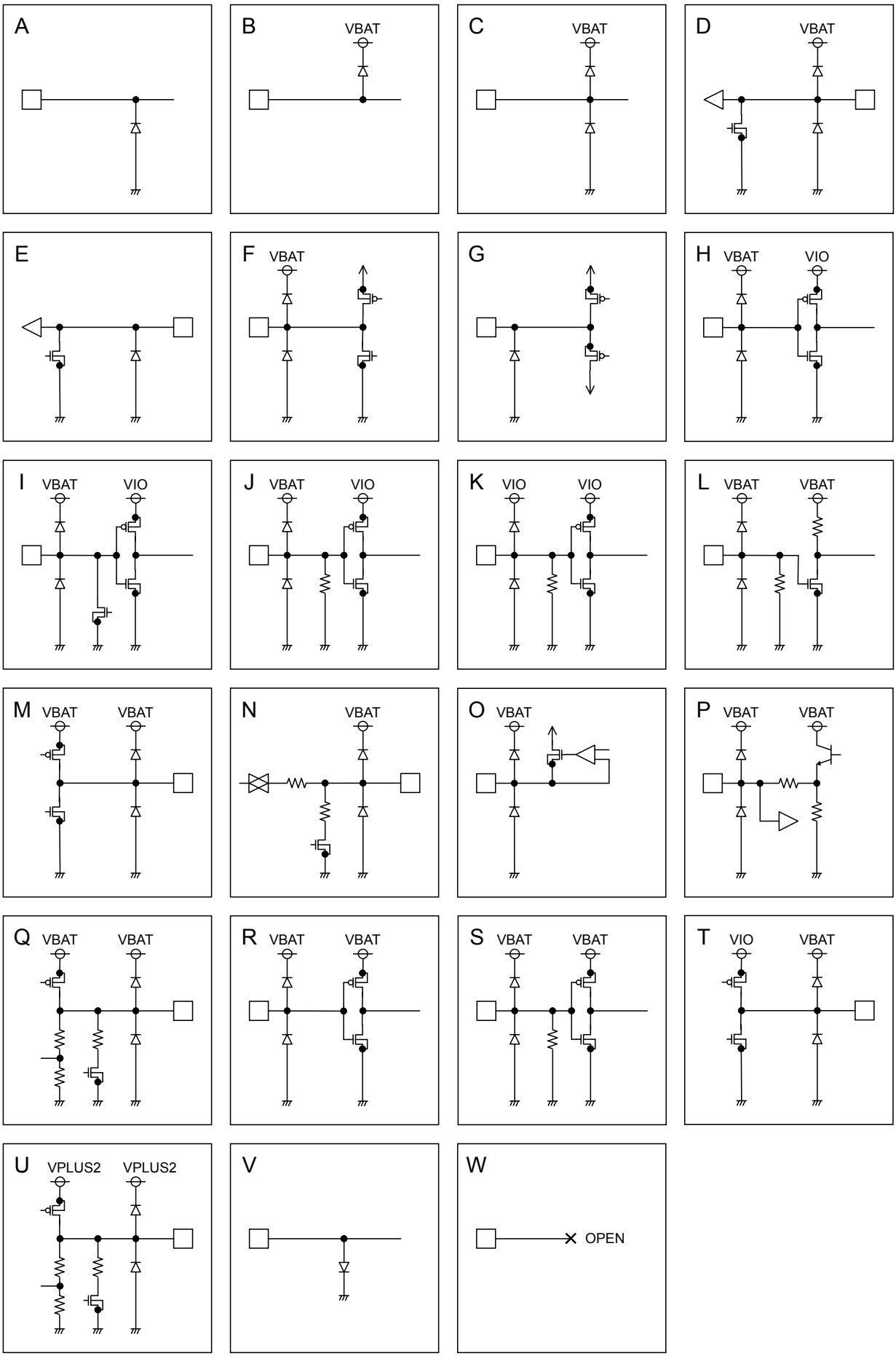


(Unit: mm)

●**Pin Functions(total 57Pins)**

No	Pin No.	Pin Name	I/O	ESD Diode		Functions	Initial conditions
				For Power	For GND		
1	B5	VBAT1	-	-	GND	Battery is connected	A
2	B8	VBAT2	-	-	GND	Battery is connected	A
3	C8	VBAT3	-	-	GND	Battery is connected	A
4	H7	VBAT4	-	-	GND	Battery is connected	A
5	J4	VBAT5	-	-	GND	Battery is connected	A
6	H2	VBAT6	-	-	GND	Battery is connected	A
7	B2	VBAT7	-	-	GND	Battery is connected	A
8	D8	VREF	O	VBAT	GND	Reference voltage output	P
9	E2	VIO	-	VBAT	GND	Power supply for logic	C
10	D2	RST	I	VBAT	GND	Reset input (L: reset, H: reset cancel)	H
11	F2	SDA	I	VBAT	GND	I2C data input	I
12	E1	SCL	I	VBAT	GND	I2C clock input	H
13	D1	TO7	-	VBAT	GND	Test pin (Open)	F
14	C2	TO6	-	-	GND	Test pin (Open)	G
15	C1	TO5	-	VBAT	GND	Test pin (Open)	F
16	B1	TO3	-	-	GND	Test pin Open)	G
17	A3	TO2	-	VBAT	GND	Test pin (Open)	F
18	A2	TO1	-	-	GND	Test pin (Open)	G
19	B3	TO4	-	-	GND	Test pin (Open)	A
20	D9	VIN6	I	-	GND	Input voltage for REG6 (connect to VBAT)	A
21	E9	VDD6	O	-	GND	REG6 output pin	Q
22	J7	SWP	O	-	GND	SWREG3 coil switching pin	A
23	J6	GNDP	-	VBAT	-	SWREG3 Power ground	B
24	H6	GNDPS	-	VBAT	-	SWREG3 Power ground	B
25	J3	VPLUS1	I	-	GND	SWREG3 boost voltage feedback pin	A
26	H3	VPLUS2	I	-	GND	Input voltage forREG3	A
27	J2	VDD3	O	VPLUS2	GND	REG3 output pin	U
28	G9	VIN1	I	VBAT	GND	Input voltage for REG	C
29	F8	VDD1	O	VBAT	GND	REG1 output pin	Q
30	H1	VDD2	O	VBAT	GND	REG2 output pin	Q
31	H9	VIN5	I	VBAT	GND	Input voltage for REG5	C
32	G8	VDD5	O	VBAT	GND	REG5 output pin	Q
33	G1	VDD7	O	VBAT	GND	REG7 output pin	Q
34	F9	VIN8	I	VBAT	GND	Input voltage for REG8	C
35	E8	VDD8	O	VBAT	GND	REG8 output pin	Q
36	H8	VINA	I	VBAT	GND	Input voltage for REGA	C
37	J8	AVDD	O	VBAT	GND	REGA output pin	Q
38	A6	VBATN2	I	-	GND	SWREG4 current sense pin	A
39	B6	VBATN1	I	-	GND	SWREG4 current sense pin	A
40	A5	SWN	O	VBAT	-	SWREG4 coil switching pin	B
41	A8	VDD4	I	GND	-	SWREG4 boost voltage feedback pin	V
42	A1	T1	I	VBAT	GND	Test pin	S
43	A9	T2	I	VBAT	GND	Test pin	S
44	J9	T3	I	VBAT	GND	Test pin	S
45	J1	T4	I	VBAT	GND	Test pin	S
46	H5	TESTO1	O	-	GND	Test pin	N
47	G2	TESTO2	O	VBAT	GND	Test pin	M
48	H4	TESTO3	O	-	GND	Test pin	N
49	B4	GND1	-	VBAT	-	Ground	B
50	A7	GND2	-	VBAT	-	Ground	B
51	B7	GND3	-	VBAT	-	Ground	B
52	B9	GND4	-	VBAT	-	Ground	B
53	C9	GND5	-	VBAT	-	Ground	B
54	J5	GND6	-	VBAT	-	Ground	B
55	F1	GND7	-	VBAT	-	Ground	B
56	A4	GND8	-	VBAT	-	Ground	B
57	G7	NC	-	-	-	NC pin	W

●Equivalent Circuit



●I²C BUS format

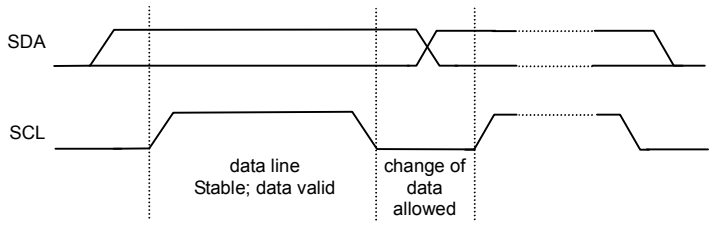
The writing/reading operation is based on the I2C slave standard.

◦Slave address

A7	A6	A5	A4	A3	A2	A1	R/W
0	0	0	1	0	0	1	1/0

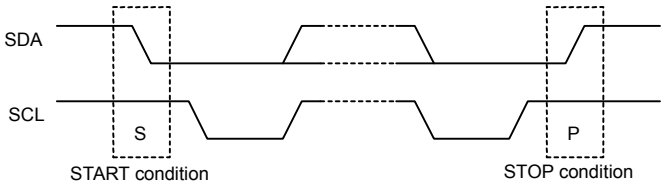
◦Bit Transfer

SCL transfers 1-bit data during H. SCL cannot change signal of SDA during H at the time of bit transfer. If SDA changes while SCL is H, START conditions or STOP conditions will occur and it will be interpreted as a control signal.



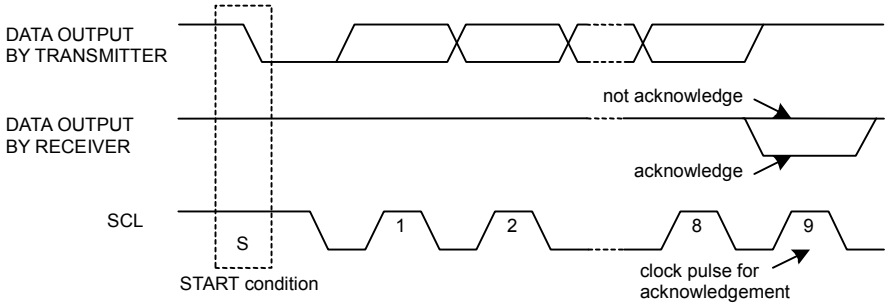
◦START and STOP condition

When SDA and SCL are H, data is not transferred on the I2C- bus. This condition indicates, if SDA changes from H to L while SCL has been H, it will become START (S) conditions, and an access start, if SDA changes from L to H while SCL has been H, it will become STOP (P) conditions and an access end.



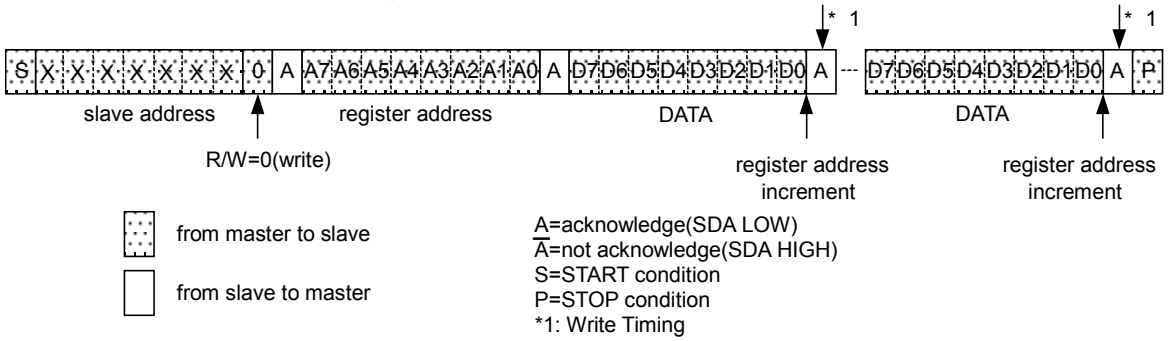
◦Acknowledge

It transfers data 8 bits each after the occurrence of START condition. A transmitter opens SDA after transfer 8bits data, and a receiver returns the acknowledge signal by setting SDA to L.



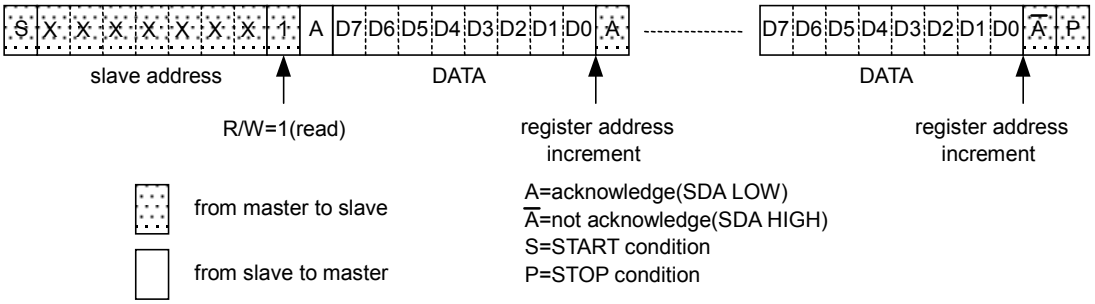
◦Writing protocol

A register address is transferred by the next 1 byte that transferred the slave address and the write-in command. The 3rd byte writes data in the internal register written in by the 2nd byte, and after 4th byte or, the increment of register address is carried out automatically. However, when a register address turns into the last address(07h), it is set to 00h by the next transmission. After the transmission end, the increment of the address is carried out.



◦Reading protocol

It reads from the next byte after writing a slave address and R/W bit. The register to read considers as the following address accessed at the end, and the data of the address that carried out the increment is read after it. If an address turns into the last address(07h), the next byte will read out 00h. After the transmission end, the increment of the address is carried out.

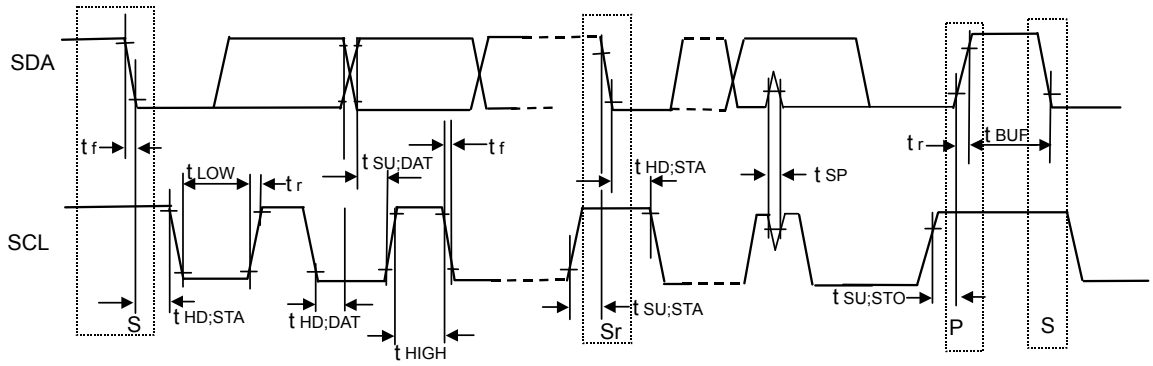


◦Multiple reading protocols

After specifying an internal address, it reads by repeated START condition and changing the data transfer direction. The data of the address that carried out the increment is read after it. If an address turns into the last address, the next byte will read out 00h. After the transmission end, the increment of the address is carried out.

As for reading protocol and multiple reading protocols, please do Ā(not acknowledge) after doing the final reading operation. It stops with read when ending by A(acknowledge), and SDA stops in the state of Low when the reading data of that time is 0. However, this state returns usually when SCL is moved, data is read, and Ā(not acknowledge) is done.

●**Timing diagram**



●**Electrical Characteristics (Unless otherwise specified, Ta=25°C, VBAT=3.6V, VIO=1.8V/3.0V)**

Parameter	Symbol	Standard-mode			Fast-mode			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
I²C BUS format								
SCL clock frequency	fSCL	0	-	100	0	-	400	kHz
LOW period of the SCL clock	tLOW	4.7	-	-	1.3	-	-	µs
HIGH period of the SCL clock	tHIGH	4.0	-	-	0.6	-	-	µs
Hold time (repeated) START condition After this period, the first clock is generated	tHD;STA	4.0	-	-	0.6	-	-	µs
Set-up time for a repeated START condition	tSU;STA	4.7	-	-	0.6	-	-	µs
Data hold time	tHD;DAT	0	-	3.45	0	-	0.9	µs
Data set-up time	tSU;DAT	250	-	-	100	-	-	ns
Set-up time for STOP condition	tSU;STO	4.0	-	-	0.6	-	-	µs
Bus free time between a STOP and START condition	tBUF	4.7	-	-	1.3	-	-	µs

●**Register List**

Address	Register data								Function
	D7	D6	D5	D4	D3	D2	D1	D0	
00h	VER［2:0］		-		-	-	-	SFTRST	Software reset
01h	-	AVDDEN	VDD6EN	VDD5EN	VDD4EN	VDD3EN	VDD2EN	VDD1EN	Power down 1
02h	VDD4SEL1	VDD4SEL0	VDD3SEL1	VDD3SEL0	Reserved				Output voltage Setting1
03h	AVDDSEL	VDD8SEL	VDD7SEL	Reserved	Reserved	VDD6SEL	Reserved	VDD5SEL	Output voltage Setting2
04h	-	-	-	-	VDD8EN	VDD7EN	Reserved	SWREG3EN	Power down 2
05h	Reserved	-	-	-	-	Reserved	Reserved	Reserved	for TEST
06h	Reserved								for TEST
07h	Reserved								for TEST
08h	Reserved								for TEST
09h	Reserved								for TEST
0Ah	Reserved								for TEST
0Bh	Reserved								for TEST

Input "0" for "-".
Input “0” for “Reserved”
Access to the register for the test and the undefined register is prohibited.

●Register Map

Address00h < Software reset >

Address	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00h	R/W	VER[2:0]		-	-	-	-	SFTRST	00h
Initial Value	20h	-	-	-	-	-	-	Initial Value	20h

Bit [7:5] : VER[2:0]
Reading the version information
"001" : DS1

This register is "Read Only"

Bit [4:1] : Not used

Bit 0 : SFTRST
"0" : Reset cancel
"1" : Reset (All register initializing)

Address01h < Power down 1 >

Address	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
01h	R/W	-	AVDDEN	VDD6EN	VDD5EN	VDD4EN	VDD3EN	VDD2EN	VDD1EN
Initial Value	00h	-	0	0	0	0	0	0	0

Bit 7 : Not used

Bit 6 : AVDDEN
AVDD Control (ON/OFF)
"0" : OFF
"1" : ON

Bit 5 : VDD6EN
VDD6 Control (ON/OFF)
"0" : OFF
"1" : ON

Bit 4 : VDD5EN
VDD5 Control (ON/OFF)
"0" : OFF
"1" : ON

Bit 3 : VDD4EN
VDD4 Control (ON/OFF)
"0" : OFF
"1" : ON

Bit 2 : VDD3EN
VDD3 Control (ON/OFF)
"0" : OFF
"1" : ON

Bit 1 : VDD2EN
VDD2 Control (ON/OFF)
"0" : OFF
"1" : ON

Bit 0 : VDD1EN
VDD1 Control (ON/OFF)
"0" : OFF
"1" : ON

Address02h < Output voltage Setting1 >

Address	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
02h	R/W	VDD4SEL1	VDD4SEL0	VDD3SEL1	VDD3SEL0	Reserved			
Initial Value	00h	0	0	0	0	0	Initial Value	00h	0

Bit [7:6] : VDD4SEL[1:0]

	VDD4 Output voltage
“00” :	-8V
“01” :	-7.5V
“10” :	-7V
“11” :	-7V

Bit [5:4] : VDD3SEL[1:0]

	VDD3 Output voltage
“00” :	14.5V
“01” :	15V
“10” :	13V
“11” :	13V

Bit [3:0] : Not used

Address03h < Output voltageSetting2 >

Address	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
03h	R/W	AVDDSEL	VDD8SEL	VDD7SEL	Reserved	Reserved	VDD6SEL	Reserved	VDD5SEL
Initial Value	00h	0	0	0	0	0	0	0	0

Bit 7 : AVDDSEL

	AVDD Output voltage Setting
“0” :	1.5V
“1” :	1.8V

Bit 6 : VDD8SEL

	VDD8 Output voltage Setting
“0” :	1.5V
“1” :	1.8V

Bit 5 : VDD7SEL

	VDD7 Output voltage Setting
“0” :	3.3V
“1” :	3.0V

Bit [4:3] : Not used

Bit 2 : VDD6SEL

	VDD6 Output voltage Setting
“0” :	3.3V
“1” :	3.2V

Bit 1 : Not used

Bit 0 : VDD5SEL

	VDD5 Output voltage Setting
“0” :	1.8V
“1” :	1.5V

Address04h < Power down 2 >

Address	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
04h	R/W	-	-	-	-	VDD8EN	VDD7EN	Reserved	SWREG3EN
Initial Value	00h	-	-	-	-	0	0	0	0

Bit [7:4] : Not used

Bit 3 : VDD8EN
VDD8 Control (ON/OFF)
"0" : OFF
"1" : ON

Bit 2 : VDD7EN
VDD7 Control (ON/OFF)
"0" : OFF
"1" : ON

Bit 1 : Not used (must be "0")

Bit 0 : SWREG3EN
SWREG3 Control (ON/OFF)
"0" : OFF
"1" : ON

●Explanation for Operate

1. Reset
   There are two kinds of reset, Software reset and Hardware reset.
   (1) Software reset
   - ◦It shifts to software reset with changing a register (SFTRST) setting “0” → “1”.
   - ◦The register is returned to the initials value under the state of Soft Reset, and it stops accepting all address except for SFTRST.
   - ◦It’s possible to release from a state of Soft Reset by setting register “1” → “0”.

   (2) Hardware reset
   - ◦It shifts to hard reset by changing RST pin “H” → “L”.
   - ◦The condition of all registers under Hardware Reset pin is returned to the initial value, and it stops accepting all address.
   - ◦It’s possible to release from a state of hardware reset by setting register “L” → “H”.

   (3) Reset Sequence
   - ◦When hardware reset was done during software reset, Software reset is canceled when hard reset is canceled. (Because the initial value of Soft Reset is “0”)

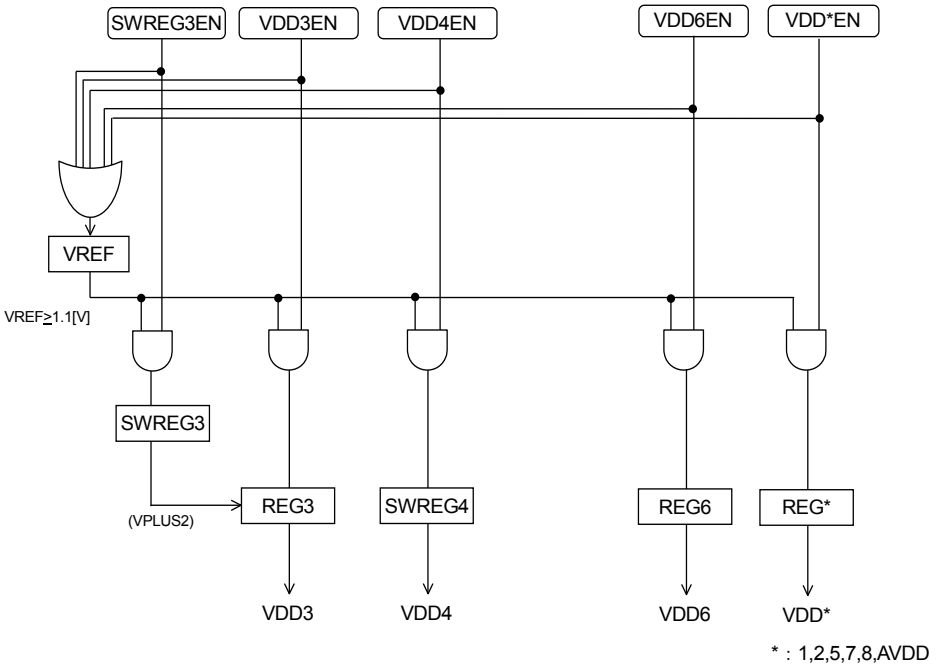
2. Thermal shutdown
   The blocks which thermal shutdown function is effective in
   SWREG3
   SWREG4
   REG1
   REG2
   REG3
   REG5
   REG6
   REG7
   REG8
   REGA

   A thermal shutdown function works in about 175 ^{o}C. (Design reference value)
   When returns to undetected condition from detected condition, each block will start up simultaneously. So, if there are some problems, (for example rush current) please work out a countermeasure on system (for example sequence on start up)

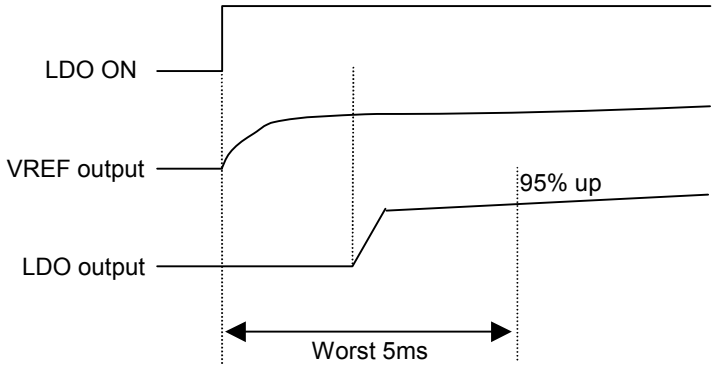
3. UVLO(Under voltage detection of VBAT)
   When UVLO works, all register (except for Address=00h, SFTRST) will return to initial value.
   Please set the register again after VBAT comes to normal value.

4. ON/OFF control

This IC controls each blocks by register setting after start up VREF (internal reference voltage).
Detection voltage of VREF's rise-up is 1.1V when static output is 1.2V.
The output of SWREG3 is power supply for REG3, but there is no internal sequencer about these 2-blocks.
Please be careful about ON/OFF timing.



VREF receives a turning on instruction blocked either each and begins rise up. Therefore, it is necessary to consider the block started up first at the rise time of VREF

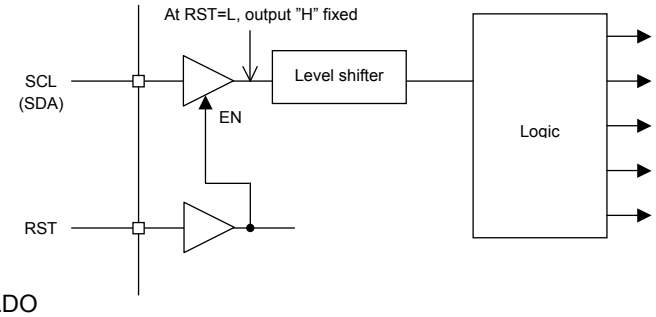


5. I^2C BUS

Operation when a signal beyond f_{SCL}=400kHz is input cannot be guaranteed, because this LSI doesn't correspond to the H/S(High Speed) mode of the I^2C BUS format.

When it uses on the serial-bus-system which the F/S(Fast Speed) mode was mixed in with the H/S mode, please connect it and remove a connection by using the mutual connection bridge from the H/S mode section to F/S mode section or in that reverse direction.

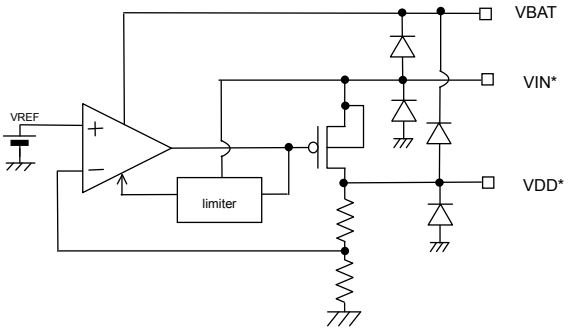
However, an optional input signal never spreads to the logic part of IC, because it stops the operation of the input buffer of SDA and SCL at RST pin=L.



6. Low input voltage LDO

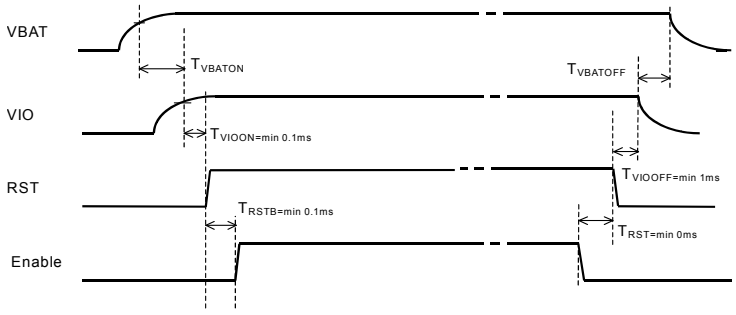
This is the system of LDO that can be input low voltage.

Please start up LDO after input VIN*, and please input VIN* after input VBAT.



7. Power up sequence

Input of VBAT, VIO and control of each block should be done by the sequence below.

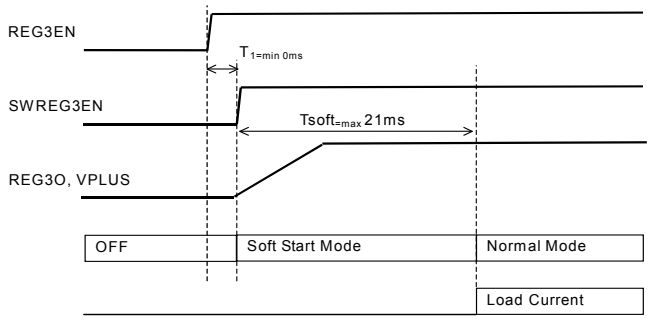


Please take enough time for each wait time

8. Start up for DC/DC
   DC/DC has soft start function to prevent rush current at starting up (both SWREG3, SWREG4)
   Soft start time is 21ms(max) based from internal OSC frequency. So, please take load current after this soft start time.

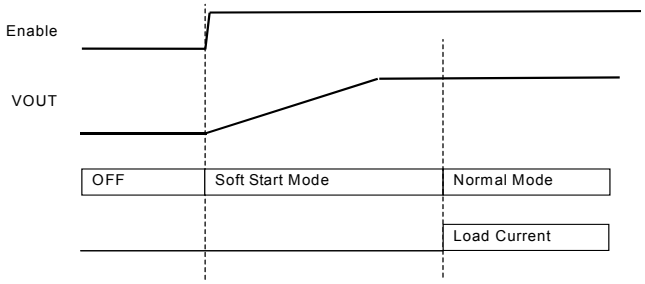
   SWREG3 is power supply for REG3. Please input the command SWREG3 on after input REG3 on, to prevent rush current at start up REG3. (REG3's rush current is prevented by SWREG3's soft start function.)

   At the unusual case the value of Cout (capacitor connected to Vout) is very large, soft start time will finish before SWREG3 rise up. So, there is a possibility to appear large rush current.

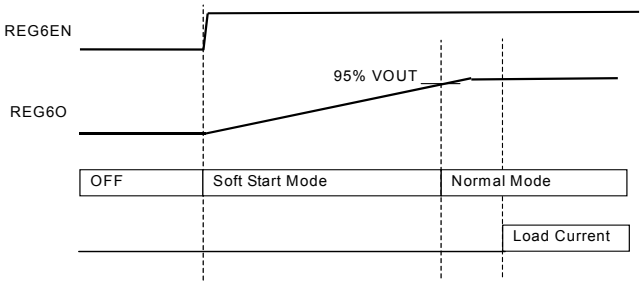


9. Start up for LDO
   LDO has soft start function to prevent rush current at starting up. This IC doesn't consider the start up with the load current. Please add the load current after LDO's output voltage rise up completely.

   ＜REG1, REG2, REG5, REG7, REG8, REGA＞

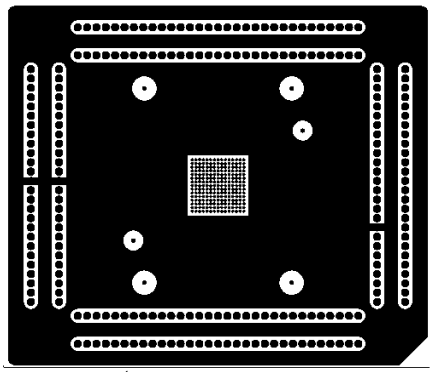


   ＜REG6＞

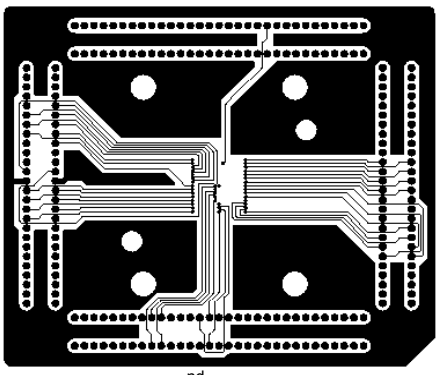


10. Input capacitor for LDO
    Regarding REG1,REG5,REG8,REGA (can be connect with different power supply from VBAT), please connect capacitor with VIN* to prevent the influence ripple of VIN* to Vout.
    The required Value of input capacitor is changes from conditions of input voltage, output voltage, output capacitor, output impedance of power supply, wire impedance of power line, etc. So, please decide it after evaluation with real application, and with an enough margin.

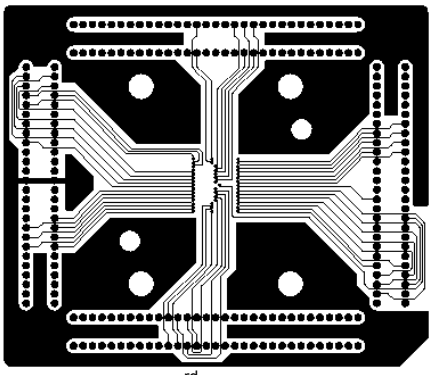
●PCB pattern of the Power Dissipation Measuring Board



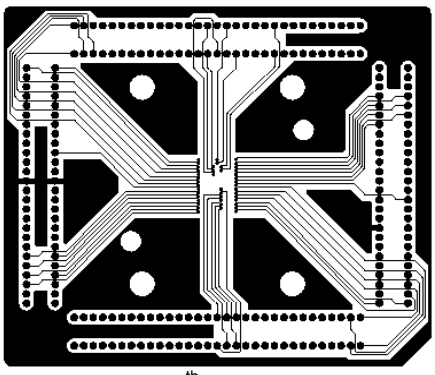
1st layer(component)



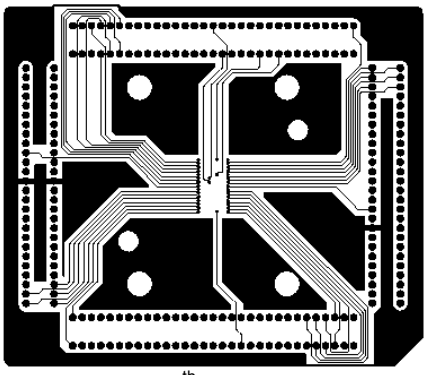
2nd layer



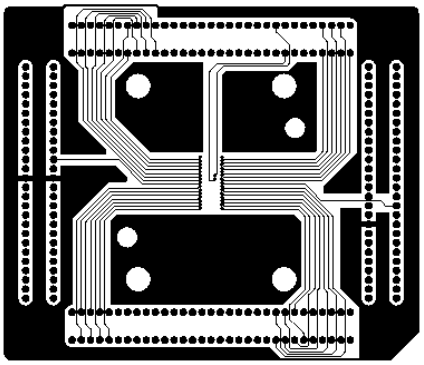
3rd layer



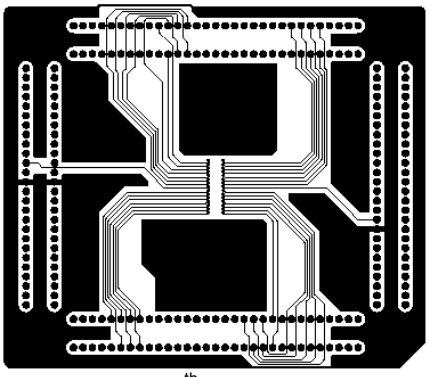
4th layer



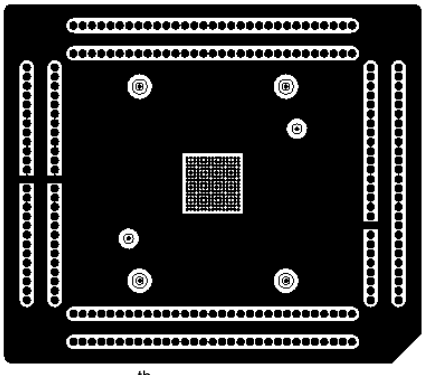
5th layer



6th layer



7th layer



8th layer(solder)

●**Notes for use**

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Power supply and ground line
Design PCB pattern to provide low impedance for the wiring between the power supply and the ground lines. Pay attention to the interference by common impedance of layout pattern when there are plural power supplies and ground lines. Especially, when there are ground pattern for small signal and ground pattern for large current included the external circuits, please separate each ground pattern. Furthermore, for all power supply pins to ICs, mount a capacitor between the power supply and the ground pin. At the same time, in order to use a capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(3) Ground voltage
Make setting of the potential of the ground pin so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no pins are at a potential lower than the ground voltage including an actual electric transient. (except for VDD4,SWN)

(4) Short circuit between pins and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between pins or between the pin and the power supply or the ground pin, the ICs can break down.

(5) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(6) Input pins
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input pin. Therefore, pay thorough attention not to handle the input pins, such as to apply to the input pins a voltage lower than the ground respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input pins a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(7) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(8) Thermal shutdown circuit (TSD)
This LSI builds in a thermal shutdown (TSD) circuit. When junction temperatures become detection temperature or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(9) Thermal design
Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

(10) LDO
Use each output of LDO by the independence. Don’t use under the condition that each output is short-circuited because it has the possibility that an operation becomes unstable.

(11) About the pin for the test, the un-use pin
Prevent a problem from being in the pin for the test and the un-use pin under the state of actual use. Please refer to a function manual and an application notebook. And, as for the pin that doesn't specially have an explanation, ask our company person in charge.

(12) About the rush current
For ICs with more than one power supply, it is possible that rush current may flow instantaneously due to the internal powering sequence and delays. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of wiring.

(13) About the function description or application note or more.
The function description and the application notebook are the design materials to design a set. So, the contents of the materials aren't always guaranteed. Please design application by having fully examination and evaluation include the external elements

●Ordering part number

B	D	6	0	3	9	G	U	-	E	2

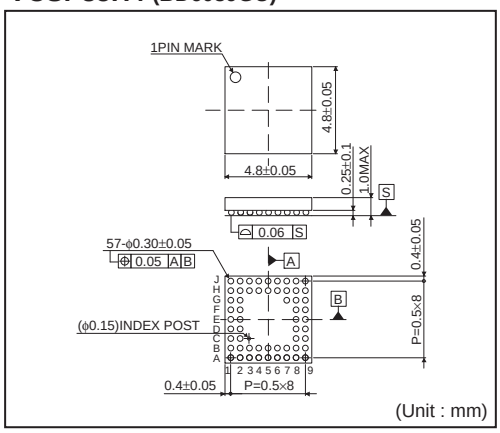
Part No. (BD)

Part No. (6039)

Package
GU: VCSP85H4

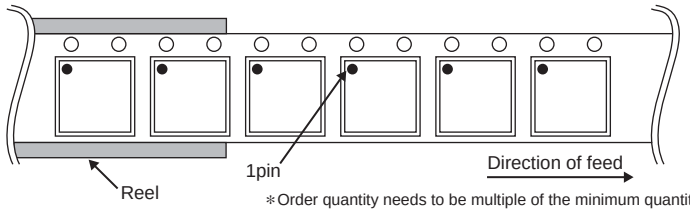
Packaging and forming specification
E2: Embossed tape and reel

VCSP85H4 (BD6039GU)



<Tape and Reel information>

Tape	Embossed carrier tape (heat sealing method)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

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